PHILIPS

Data handbook

Philips Electronic Components and Materials

Integrated circuits

Part 2 May 1980

Bipolar ICs for video equipment

INTEGRATED CIRCUITS

PART 2 - MAY 1980

BIPOLAR ICs FOR VIDEO EQUIPMENT

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

May 1980

ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**February 1980**	**T1 02-80 (ET1a 12-75)**	**Tubes for r.f. heating**
Part 2	**April 1980**	**T2 04-80 (ET1b 08-77)**	**Transmitting tubes for communications**
Part 2a	**November 1977**	**ET2a 11-77**	**Microwave tubes** Communication magnetrons, magnetrons for microwave heating, klystrons, travelling-wave tubes, diodes, triodes T-R switches
Part 2b	**May 1978**	**ET2b 05-78**	**Microwave semiconductors and components** Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators
Part 3	**January 1975**	**ET3 01-75**	**Special Quality tubes, miscellaneous devices**
Part 5a	**October 1979**	**ET5a 10-79**	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
Part 5b	**December 1978**	**ET5b 12-78**	**Camera tubes and accessories, image intensifiers**
Part 6	**January 1977**	**ET6 01-77**	**Products for nuclear technology** Channel electron multipliers, neutron tubes, Geiger-Müller tubes
Part 7a	**March 1977**	**ET7a 03-77**	**Gas-filled tubes** Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes
Part 7b	**May 1979**	**ET7b 05-79**	**Gas-filled tubes** Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units
Part 8	**July 1979**	**ET8 07-79**	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, monitor tubes, components for colour television, components for black and white television.
Part 9	**March 1978**	**ET9 03-78**	**Photomultiplier tubes; phototubes**

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**March 1980**	**S1 03-80** **(SC1b 05-77)**	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	**May 1980**	**S2 05-80** **(SC1a 08-78)**	**Power diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
Part 2	**June 1979**	**SC2 06-79**	**Low-frequency power transistors**
Part 3	**January 1978**	**SC3 01-78**	**High-frequency, switching and field-effect transistors***
Part 3	**April 1980**	**S3 04-80** **(SC2 11-77, partly)** **(SC3 01-78, partly)**	**Small-signal transistors**
Part 4a	**December 1978**	**SC4a 12-78**	**Transmitting transistors and modules**
Part 4b	**September 1978**	**SC4b 09-78**	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, photocouplers, infrared sensitive devices, photoconductive devices
Part 4c	**July 1978**	**SC4c 07-78**	**Discrete semiconductors for hybrid thick and thin-film circuits**

* Field-effect transistors and wideband transistors will be transferred to S5 and SC3c respectively. The old book SC3 01-78 should be kept until then.

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	**May 1980**	**IC1 04-80 (SC5b 03-77)**	**Bipolar ICs for radio and audio equipment**
Part 2	**May 1980**	**IC2 04-80 (SC5b 03-77)**	**Bipolar ICs for video equipment**
Part 5a	**November 1976**	**SC5a 11-76**	**Professional analogue integrated circuits**
Part 6	**October 1977**	**SC6 10-77**	**Digital integrated circuits** LOCMOS HE4000B family
Part 6b	**August 1979**	**SC6b 08-79**	**ICs for digital systems in radio and television receivers**
Signetics integrated circuits			Bipolar and MOS memories 1979 Bipolar and MOS microprocessors 1978 Analogue circuits 1979 Logic - TTL 1978

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**July 1979**	**CM1 07-79**	**Assemblies for industrial use** PLC modules, high noise immunity logic FZ/30 series, NORbits 60-series, 61-series, 90-series, input devices, hybrid integrated circuits, peripheral devices
Part 3a	**September 1978**	**CM3a 09-78**	**FM tuners, television tuners, surface acoustic wave filters**
Part 3b	**October 1978**	**CM3b 10-78**	**Loudspeakers**
Part 4a	**November 1978**	**CM4a 11-78**	**Soft Ferrites** Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube transformer cores
Part 4b	**February 1979**	**CM4b 02-79**	**Piezoelectric ceramics, permanent magnet materials**
Part 6	**April 1977**	**CM6 04-77**	**Electric motors and accessories** Small synchronous motors, stepper motors, miniature direct current motors
Part 7	**September 1971**	**CM7 09-71**	**Circuit blocks** Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
Part 7a	**January 1979**	**CM7a 01-79**	**Assemblies** Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	**June 1979**	**CM8 06-79**	**Variable mains transformers**
Part 9	**August 1979**	**CM9 08-79**	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators
Part 10	**April 1978**	**CM10 04-78**	**Connectors**
Part 11	**December 1979**	**CM11 12-79**	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	**November 1979**	**CM12 11-79**	**Variable resistors and test switches**
Part 13	**December 1979**	**CM13 12-79**	**Fixed resistors**
Part 14	**April 1980**	**C14 04-80 (CM2b 02-78)**	**Electrolytic and solid capacitors**
Part 15	**May 1980**	**C15 05-80 (CM2b 02-78)**	**Film capacitors, ceramic capacitors, variable capacitors**

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

SELECTION GUIDE BY FUNCTION

VISION I.F. CIRCUITS

Economical circuits

TCA270S; SQ	i.f. amplifier and demodulator; n-p-n tuners
TDA2540; Q	i.f. amplifier and demodulator; n-p-n tuners
TDA2541; Q	i.f. amplifier and demodulator; n-p-n tuners
TDA2542; Q	i.f. amplifier and demodulator; for E and L standards; p-n-p tuners
TDA2544	i.f. amplifier and demodulator; MOS tuners

High-performance circuits

TDA3540; Q	i.f. amplifier and demodulator; n-p-n tuners
TDA3541; Q	i.f. amplifier and demodulator; n-p-n tuners

COLOUR DECODING CIRCUITS

TBA530; Q	RGB matrix preamplifier
TBA540; Q	reference combination
TBA560C; CQ	luminance and chrominance control combination
TCA640	chrominance amplifier for SECAM or PAL/SECAM decoders
TCA650	chrominance demodulator for SECAM or PAL/SECAM decoders
TCA660B	contrast, saturation and brightness control circuit for colour difference and luminance signals
TDA2510; Q	chrominance combination
TDA2520; Q	colour demodulator combination
TDA2522; Q	colour demodulator combination
TDA2523; Q	colour demodulator combination
TDA2530; Q	RGB matrix preamplifier
TDA2532; Q	RGB matrix preamplifier
TDA2560; Q	luminance and chrominance control combination
TDA3500	video control of combination
TDA3501	video control combination
TDA3510	PAL decoder
TDA3520	SECAM decoder
TDA3560	PAL decoder
TDA3570	NTSC decoder

SYNC PROCESSORS; HORIZONTAL; VERTICAL

TBA720A; AQ	horizontal oscillator circuit
TBA890; Q	signal processing circuit
TBA920; Q; S	horizontal combination
TDA2571A; AQ	horizontal synchronization and vertical 625 divider system
TDA2573A	horizontal oscillator combination with vertical 525 divider system
TDA2575A; AQ	horizontal synchronization and vertical 525 divider system
TDA2576	horizontal oscillator combination with vertical divider
TDA2576A	horizontal oscillator combination with vertical 625 divider system
TDA2593	horizontal combination

SELECTION GUIDE BY FUNCTION (continued)

VERTICAL DEFLECTION CIRCUITS

TDA2652	vertical deflection circuit ((20 AX; 30 AX systems)
TDA2653	vertical deflection circuit (large screen; 30 AX systems)
TDA2654	vertical deflection circuit (monochrome, 110°; tiny-vision colour, 90°)
TDA3650	vertical deflection circuit (large screen; 30 AX systems)

SOUND CIRCUITS

TBA750C; CQ	limiter/amplifier
TCA420A	hi-fi FM/IF amplifier
TDA1512	12 to 20 W hi-fi audio power amplifier
TDA2610; A	4 to 7 W audio power amplifier
TDA2611A	5 W audio power amplifier
TDA2612	10 W hi-fi audio power amplifier
TDA2790	television sound combination (volume, treble, bass)
TDA2791	television sound combination (volume, treble, bass)

VIDEO RECORDER CIRCUITS

TDA2700	562,5 kHz oscillator
TDA2710	chrominance signal/mixer
TDA2720	colour sub-carrier oscillator
TDA2730	FM limiter/demodulator

MISCELLANEOUS

TAA550	voltage stabilizer for electronic tuning
TCA530	voltage stabilizer for electronic tuning
TCA750	multi-stabilizer for electronic tuning
TDA0820	double balanced modulator/demodulator
TDA2581	control circuit for SMPS
TDA2582	control circuit for PPS
TDA2640; Q	SMPS drive circuit

NUMERICAL INDEX

NUMERICAL INDEX (continued)

TDA2582; Q	control circuit for PPS
TDA2593	horizontal combination
TDA2610; A	4 to 7 W audio power amplifier
TDA2611A	5 W audio power amplifier
TDA2612	10 W hi-fi audio power amplifier
TDA2640; Q	SMPS drive circuit
TDA2652	vertical deflection circuit (20 AX; 30 AX system)
TDA2653	vertical deflection circuit (large screen; 30 AX systems)
TDA2654	vertical deflection circuit (monochrome, 110°; tiny-vision colour, 90°)
TDA2700	562,5 kHz oscillator (video recorders)
TDA2710	chrominance signal/mixer (video recorders)
TDA2720	colour sub-carrier oscillator (video recorders)
TDA2730	FM limiter/demodulator (video recorders)
TDA2790	television sound combination (volume, treble, bass)
TDA2791	television sound combination (volume, treble, bass)
TDA3500	video control combination
TDA3501	video control combination
TDA3510	PAL decoder
TDA3520	SECAM decoder
TDA3540; Q	i.f. amplifier and demodulator; n-p-n tuners
TDA3541; Q	i.f. amplifier and demodulator; p-n-p tuners
TDA3560	PAL decoder
TDA3570	NTSC decoder
TDA3650	vertical deflection system (large screen; 30 AX system)

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook.
Detailed information will be supplied on request.

TAA630S
TAA630T
TBA510; Q
TBA520; Q
TBA550; Q

TBA750A; AQ (successor type: TBA750C; CQ)
TBA900; Q
TBA990; Q
TCA290A
TCA540; Q

TCA800
TCA820 (successor type: TDA0820)
TDA2500; Q
TDA2571; Q (successor type: TDA2571A; AQ)
TDA2590; Q

TDA2591 (successor type: TDA2593)
TDA2600; Q
TDA2620; Q
TDA2630; Q
TDA2631; Q

TDA2670
TDA2680
TDA2690

GENERAL

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

The FIRST LETTER divides the solitary circuits into:

S : Solitary digital circuits
T : Analogue circuits
U : Mixed analogue/digital circuits

The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

MA : { Microcomputer / Central processing unit
MB : Slice processor (see note 2)
MD : Correlated memories
ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
P : for plastic DIL
Q : for QIL
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

   Examples: i, v, p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

   Examples: I, V, P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.
A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2, i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.
Where there is no possibility of confusion the second subscript may be omitted.

Examples: $V_{2\text{-}12}$, $v_{14\text{-}2}$, V_5, v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values : M or m
For average values : AV or av
For root-mean-square values: (RMS) or (rms)
For d.c. values : no additional subscripts

The upper case subscripts indicate total values.
The lower case subscripts indicate values of varying components:

Examples: I_2, I_{2AV}, $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO}, V_{be}, V_{CES}, I_C

V_{DSS}, V_{GS}, I_D

List of subscripts:

E, e	=	Emitter terminal
B, b	=	Base terminal for bipolar transistors, Substrate for MOS devices
C, c	=	Collector terminal
D, d	=	Drain terminal
G, g	=	Gate terminal
S, s	=	Source terminal for MOS devices Substrate for bipolar transistor circuits
(BR)	=	Break-down
M, m	=	Maximum (peak) value
AV, av	=	Average value
(RMS), (rms)	=	R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i, z_f, y_o, k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE}, h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i, z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

   i (for 11) = input
   o (for 22) = output
   f (for 21) = forward transfer
   r (for 12) = reverse transfer

Examples: $V_1 = h_i I_1 + h_r V_2$

$I_2 = h_f I_1 + h_o V_2$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.
The subscript 1 = input; the subscript 2 = output.
The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

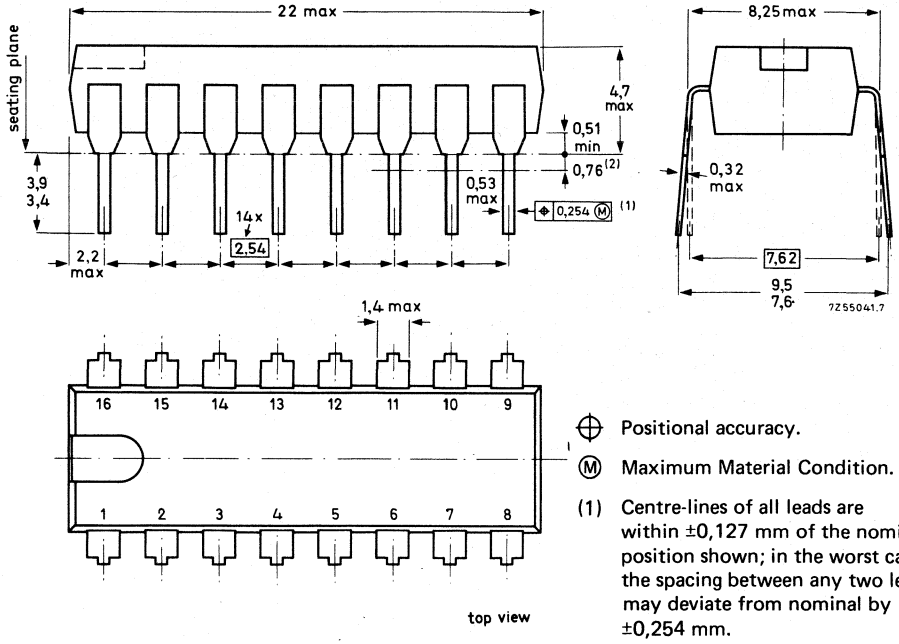
   e = common emitter
   b = common base
   c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

   R_e (h_i) etc. ... for the real part
   I_m (h_i) etc. ... for the imaginary part

PACKAGE OUTLINES

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

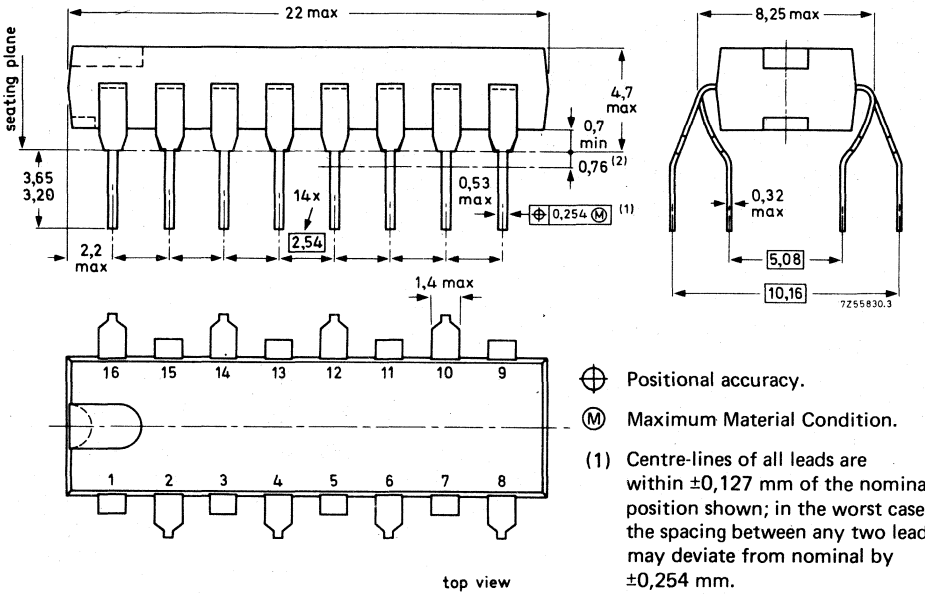
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)



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Ⓜ Maximum Material Condition.

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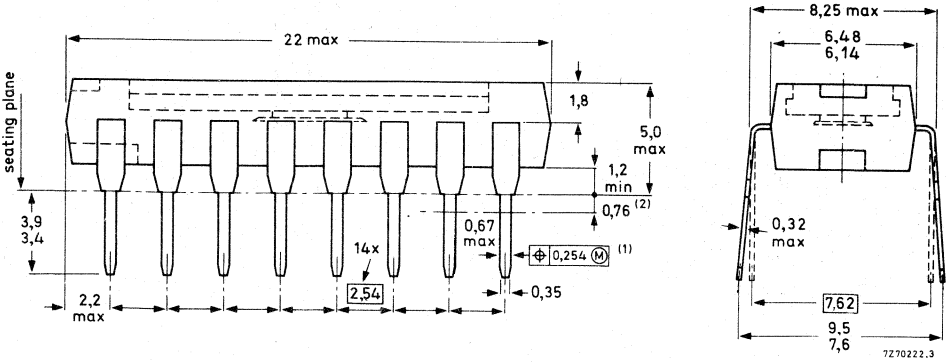
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-69B, D)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

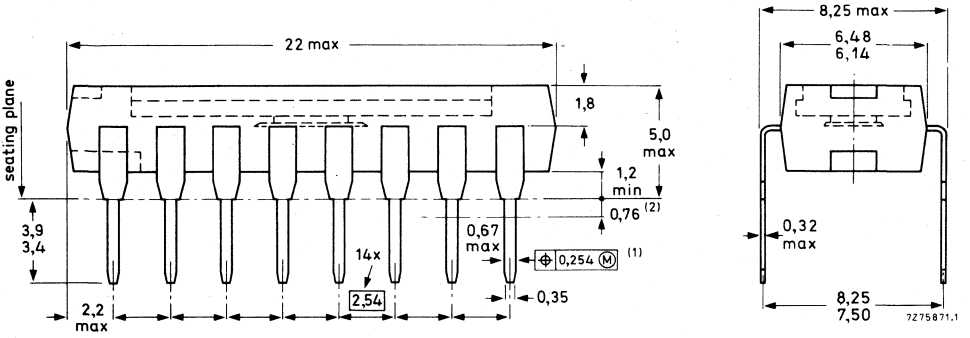
2. By dip or wave

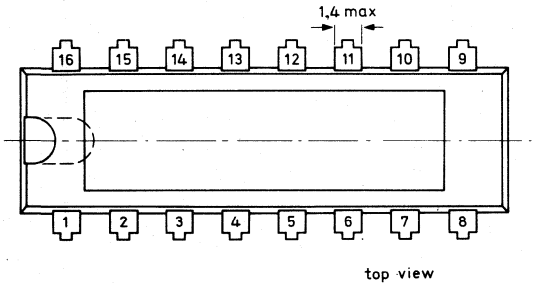
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-69C)





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

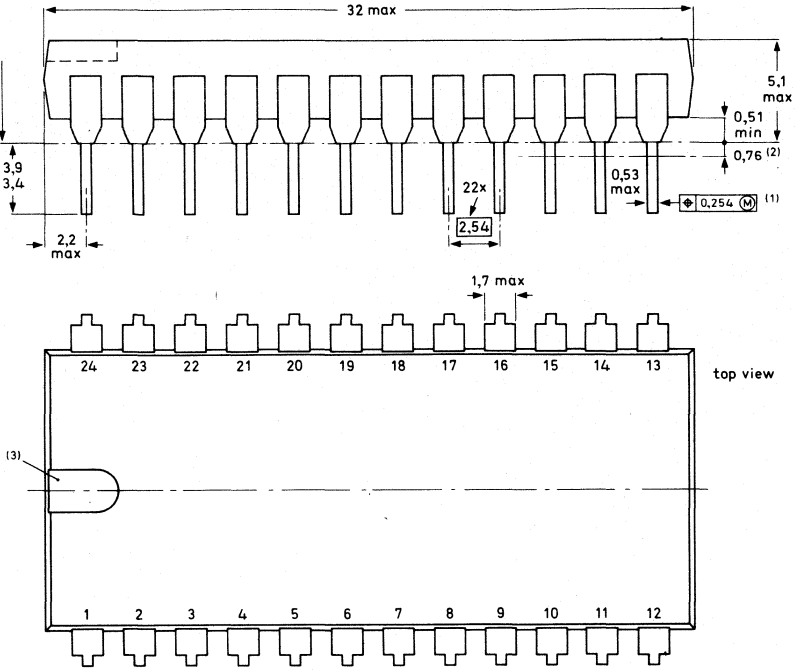
2. By dip or wave

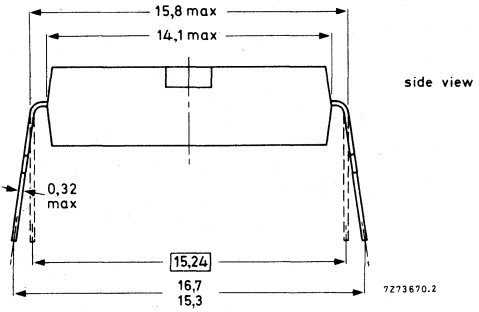
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

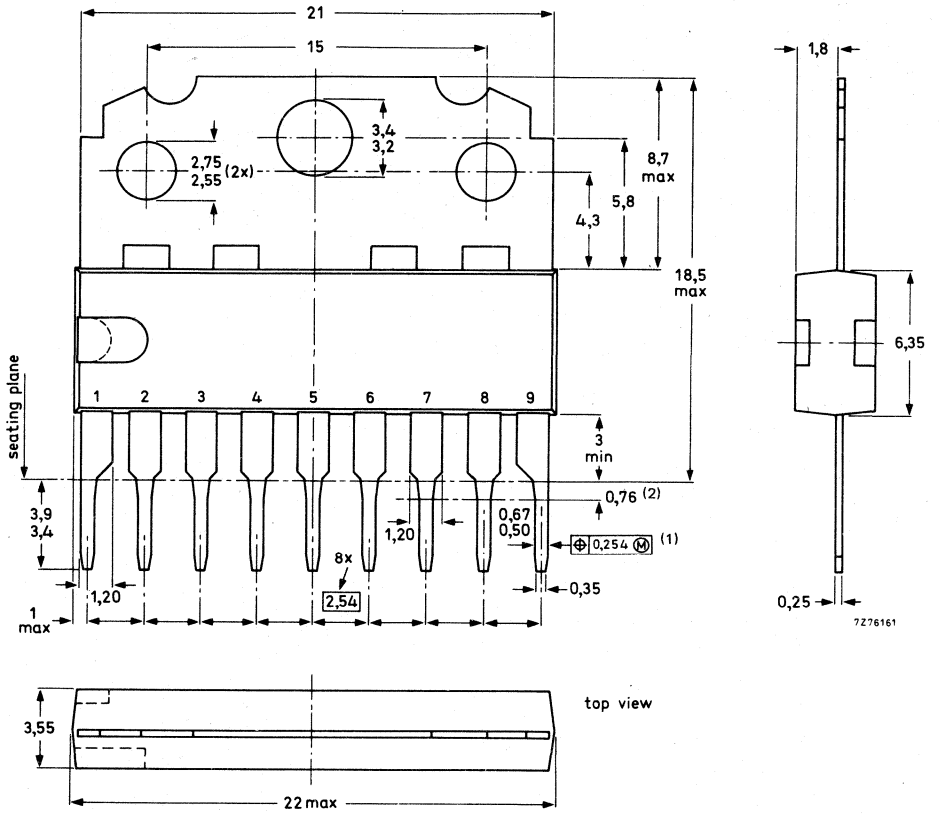
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See SOT-69C, for example.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110A)



Dimensions in mm

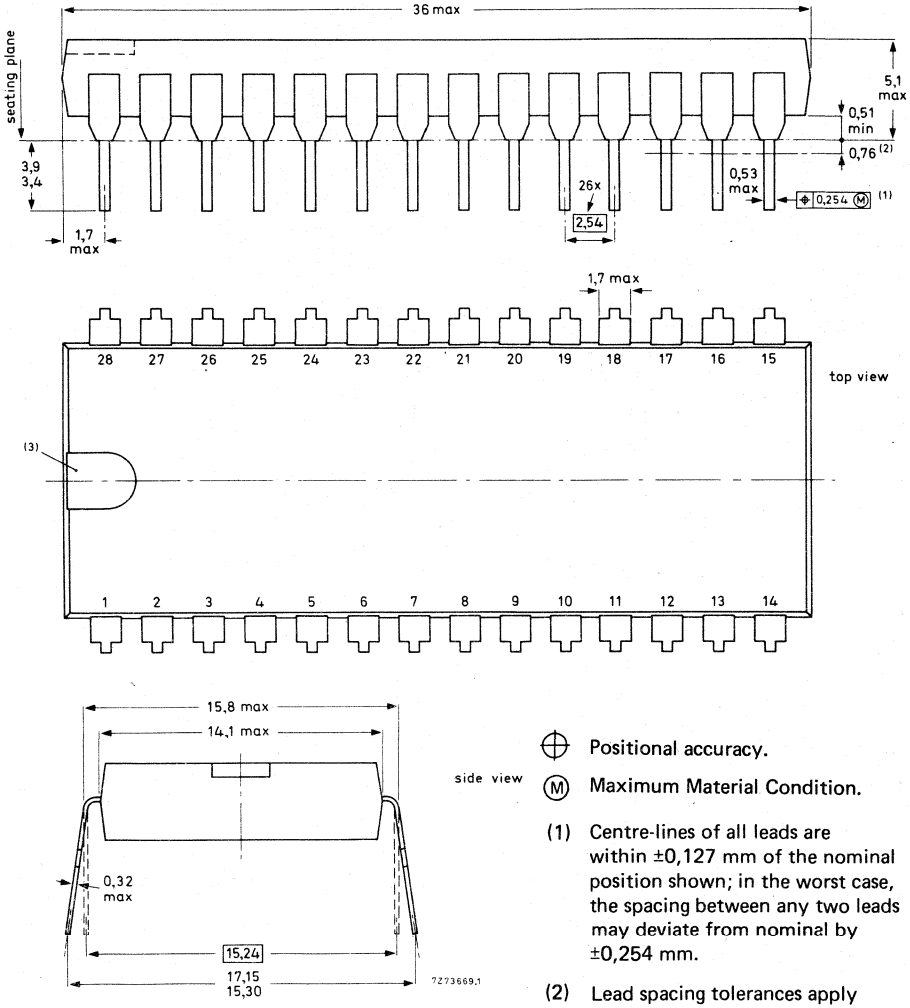
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

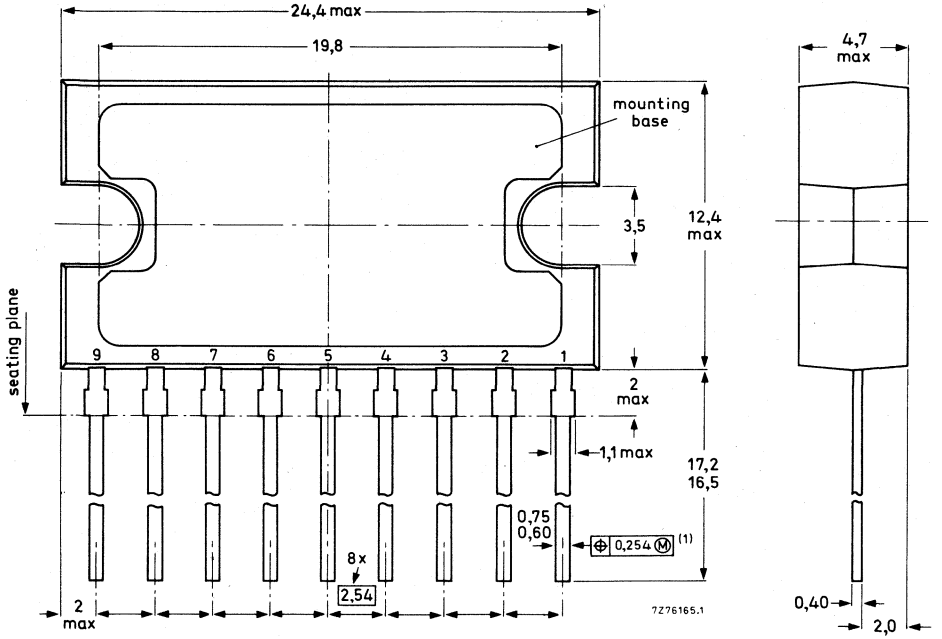
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See SOT-69C, for example.

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131B)



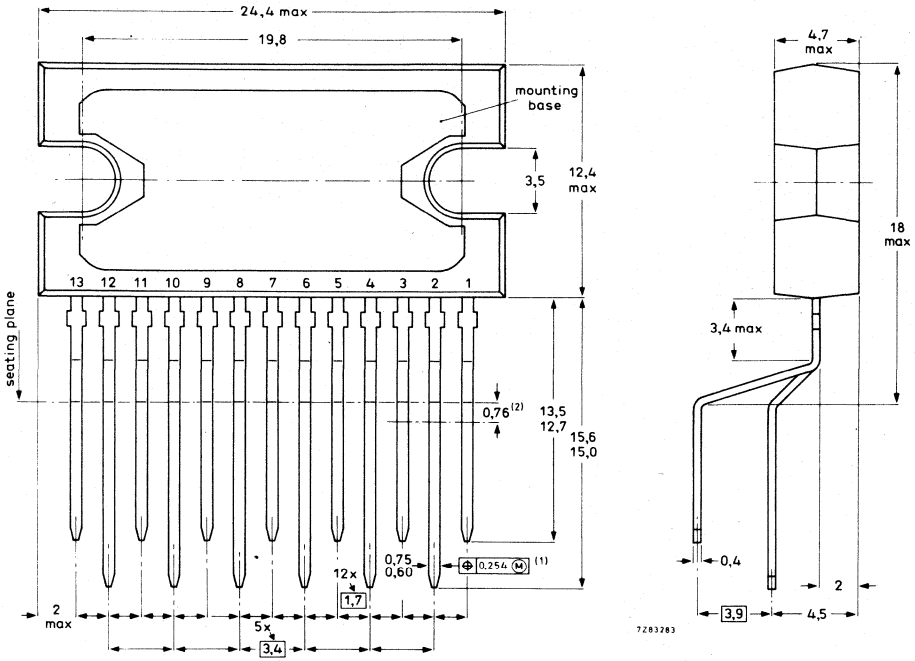
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

13-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-141)



Dimensions in mm

⊕ Positional accuracy.

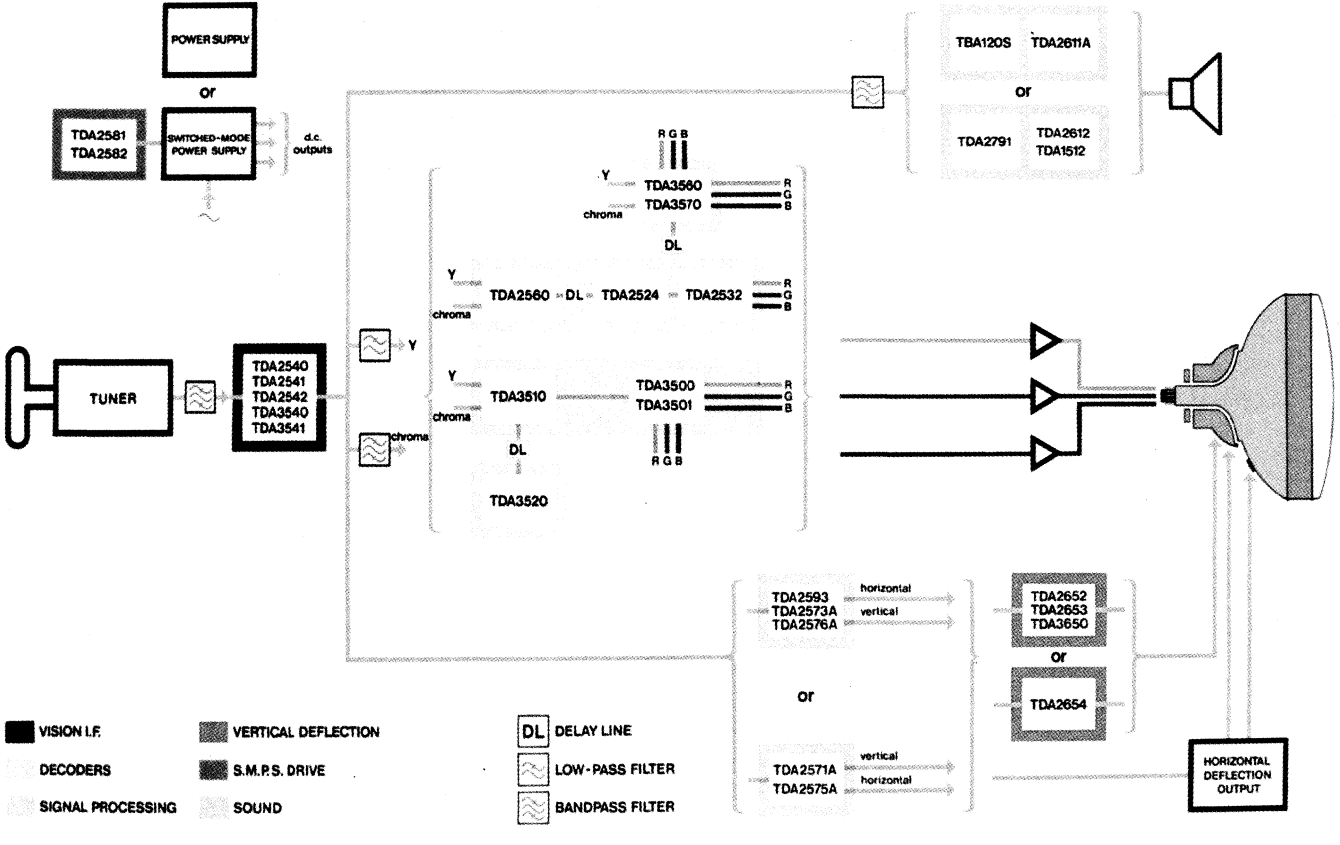
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

INTRODUCTION

INTEGRATING COLOUR TELEVISION



INTRODUCTION TO BIPOLAR ICs FOR VIDEO EQUIPMENT

Bipolar ICs find extensive application in video equipment: black-and-white and colour television, video tape recorders, video long play systems, etc.

The diagram opposite shows our range of bipolar ICs for colour television. The complete range of video ICs is given in this data handbook.

VOLTAGE STABILIZER

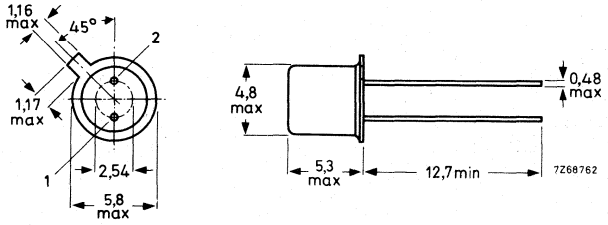
The TAA550 is an integrated monolithic voltage stabilizer, especially designed to provide the supply voltage for variable capacitance diodes in television tuners independent of supply voltage and temperature variations.

QUICK REFERENCE DATA			
Supply current	I_1	typ. 5	mA
Stabilized voltage	V_{12}	32 to 35	V
Differential internal resistance	r_{12}	typ. 10	Ω

PACKAGE OUTLINE

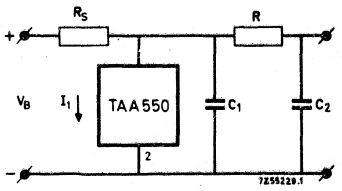
Dimensions in mm

TO-18; 2 pins



pin 1 connected to the case

RECOMMENDED CIRCUIT

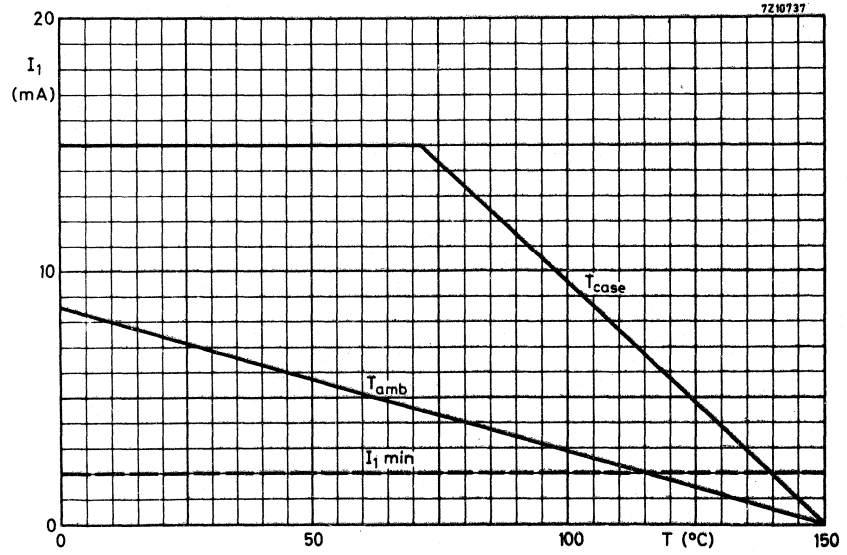


$V_B >> V_{12}$
I_1 typ. 5 mA
$R \geq 22\ \Omega$
C_1 = 300 to 4700 pF

C_2: to be connected if decoupling for low frequent noise is necessary
In practice values up to 10 μF are used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Maximum allowable supply current versus temperature



Temperatures

Storage temperature	T_{stg}	−55 to +150	°C
Operating ambient temperature	T_{amb}	−20 to +150	°C

CHARACTERISTICS

Recommended supply current	I_1	>	2	mA
		typ.	5	mA
Stabilized voltage	V_{12}	30 to 35		V
Differential internal resistance at f = 1 kHz I_1 = 5 mA	r_{12}	typ.	10	Ω
		<	25	Ω
Temperature coefficient at T_{amb} = 10 to 50 °C	$\frac{\Delta V_{12}}{\Delta T_{amb}}$	typ.	−0,13	mV/°C
		−3,1 to +1,55		mV/°C

RGB MATRIX PREAMPLIFIER

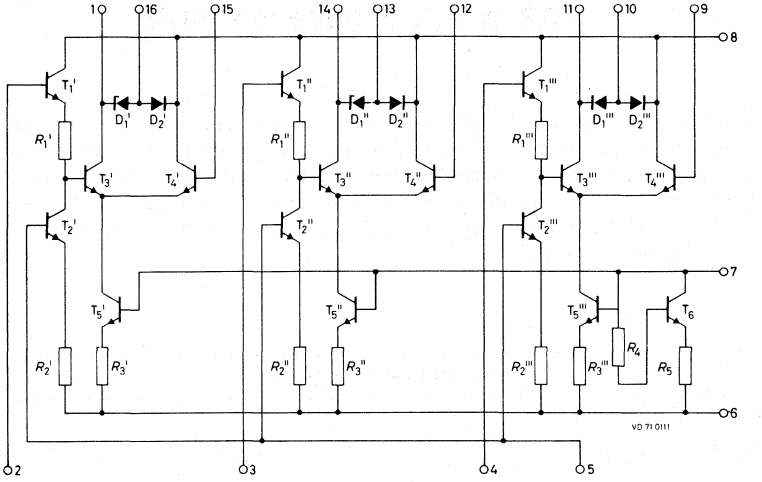
The TBA530 is an integrated circuit for colour television receivers incorporating a matrix preamplifier for RGB cathode or grid drive of the picture tube without clamping circuits. The chip lay-out has been designed to ensure tight thermal coupling between all the transistors in each channel to minimise and equalise thermal drifts between channels. Also, each channel follows an identical lay-out to ensure equal frequency behaviour of the three channels.

QUICK REFERENCE DATA				
Supply voltage	V_{8-6}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of luminance and colour-difference channels	G	typ.	100	
Total current consumption	I_{tot}	typ.	30	mA

PACKAGE OUTLINES

TBA530 : 16-lead DIL; plastic (SOT-38).
TBA530Q: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{8-6}	max.	13.2	V
Currents				
Supply currents	I_1 ; I_{11} ; I_{14}	max.	10	mA
	I_{10} ; I_{13} ; I_{16}	max.	50	mA[1])
Power dissipation				
Total power dissipation	P_{tot}	max.	400	mW[1])
Temperatures				
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +60		°C

CHARACTERISTICS measured in circuit on page 5

Measuring conditions: V_{8-6} = 12 V; T_{amb} = 25 °C
black level: $V_{R-Y} = V_{G-Y} = V_{B-Y}$ = 7.5 V
V_Y = 1.5 V

Colour difference input peak-to-peak values	$V_{2-6(p-p)}$	typ.	1.4	V
	$V_{3-6(p-p)}$	typ.	0.82	V
	$V_{4-6(p-p)}$	typ.	1.78	V
Luminance input signal (peak-to-peak value)	$V_{5-16(p-p)}$	typ.	1	V
Gain of colour channels (B-Y;G-Y;R-Y) at f = 0.5 MHz	G_{2-6}, G_{3-6}, G_{4-6}	typ.	100	2)
Ratio of gain of luminance amplifier to colour amplifiers		typ.	1	
D.C. output voltage	V_R, V_G, V_B	typ.	165	V

1) At increased voltages due to external failures (e.g. collector-basis breakdown in the output transistors) a maximum current of 50 mA is permitted between pins 16 and 8, 13 and 8, 10 and 8. The maximum allowable dissipation in this case is 500 mW.

2) G is defined as the voltage ratio between the input signals at the pins 2, 3, 4 and the output signals at the collectors of the output transistors.

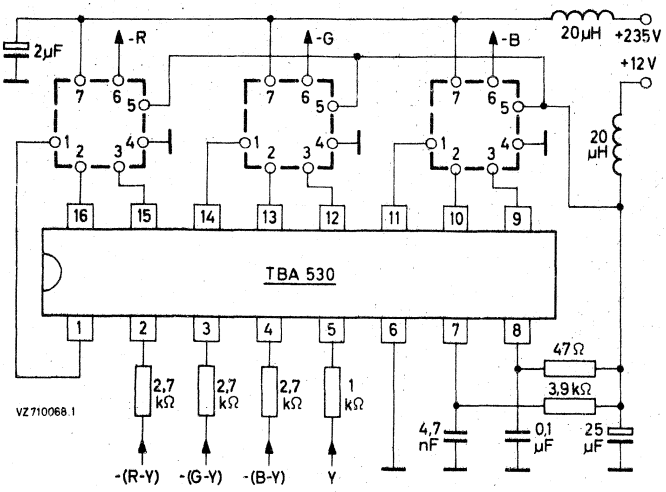
CHARACTERISTICS (continued)

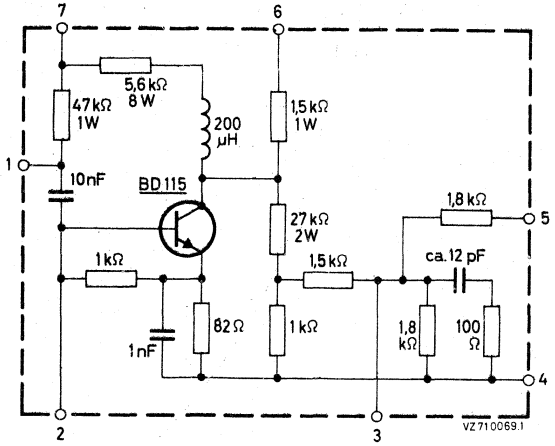
Input resistance of colour difference amplifiers at f = 1 kHz	R_{2-6} R_{3-6} R_{4-6}	typ.	60	kΩ
Input capacitance of colour difference amplifiers at f = 1 MHz	C_{2-6} C_{3-6} C_{4-6}	typ.	3	pF
Input resistance of luminance amplifier at f = 1 kHz	R_{5-6}	typ.	20	kΩ
Input capacitance of luminance amplifier at f = 1 MHz	C_{5-6}	typ.	10	pF
Bandwidth of all channels (3 dB)	B	typ.	6	MHz
Total current drain	I_{tot}	typ.	30	mA

PINNING see also APPLICATION INFORMATION circuit diagram on page 5.

1. Output load resistor (red signal)
2. R-Y input signal
3. G-Y input signal
4. B-Y input signal
5. Luminance signal input
6. Earth (negative supply)
7. Current feed point
8. 12 V positive supply
9. Blue channel feedback
10. Blue signal output
11. Output load resistor (blue signal)
12. Green channel feedback
13. Green signal output
14. Output load resistor (green signal)
15. Red channel feedback
16. Red signal output

APPLICATION INFORMATION





APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin numbering (see also page 5)

1. Output load resistor, red signal (pin 11: blue signal, pin 14: green signal)
Resistors (47 kΩ, 1 W) connected to +200 V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by an internal zener type junction and the d.c. feedback and is approximately +8 V. The maximum current which can be allowed at each of these pins is 10 mA.

2. R-Y input signal
This signal is fed via a low-pass filter from the TBA520 demodulator i.c. (pin 7) having a d.c. level of +7.5 V and an amplitude of 1.40 V peak to peak. The input resistance for this pin is typically 60 kΩ with an input capacitance of less than 3 pF (similarly for pins 3 and 4).

3. G-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 0.82 V peak to peak (see pin 2).

4. B-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 1.78 V peak to peak (see pin 2)

5. Luminance signal input
The d.c. level on this pin for picture black is +1.5 V. The required signal amplitude is 1 V black-to-white with negative-going sync (or blanking) for cathode drive as shown. The input resistance at this pin is 20 kΩ approximately with a capacitance of typ. 10 pF.

6. Negative supply (earth)

7. Current feed point
A current of approximately 2.5 mA is required at this pin, fed via a 3.9 kΩ resistor from +12 V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.

8. Positive 12 V supply
Maximum supply voltage permitted, 13.2 V. Current consumption approximately 30 mA.

9. Blue channel feedback (green channel, pin 12: red channel, pin 15)
The d.c. working points and gains of both the output stages and the i.c. amplifier stages are stabilised by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the d.c. level of the colour difference signals produced by the TBA520 demodulator i.c. The gains of the R-G-B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (VR1, VR2). (See notes on setting up decoder).

APPLICATION INFORMATION (continued)

10. Blue signal output (green and red signal outputs on 13 and 16)
These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a d.c. level shift appropriate for driving the output transistor bases directly. To by-pass the zener junctions at h.f. three 10 nF capacitors are required.

11. Output load resistor, blue channel (pin 1).

12. Green channel feedback (see pin 9).

13. Green signal output (see pin 10).

14. Output load resistor , green channel (see pin 1).

15. Red channel feedback (see pin 9).

16. Red signal output (see pin 10).

BRIEF PERFORMANCE DETAILS AND COMMENTS

1. Spread of the ratio of voltage gains for colour difference and luminance signal inputs 0.9 to 1.1.

2. Very careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon h.f. response of inevitable differences, e.g., the absence of a potentiometer in one of the stages, the compensating capacitors C_1, C_2 and C_3 may be appropriately selected for any given board layout.

3. The signal black level at the collectors of the R-G-B output stages depends upon the +12 V supply, the d.c. level of the colour difference signals from the TBA520 demodulator i.c. and the black level potential of the luminance signal applied to the TBA530 matrix i.c. The d.c. levels of the signals produced and handled by the i.c.'s are designed to have approximately proportional tracking with the 12 V supply potential,

$$\text{i.e.,} \quad \frac{\Delta V_{(\text{d.c. level, signal})}}{\Delta V_{12V}} \approx \frac{V_{\text{nom(d.c. level, signal)}}}{12}$$

To ensure that changes in picture black level due to variations on the 12 V supply to the i.c.'s occur in a predictable way, all the i.c.'s should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12 V supply should have a stability of not worse than ±3% due to operational variations, and preferably be tracked with the screen-grid supply of the picture tube.

REFERENCE COMBINATION

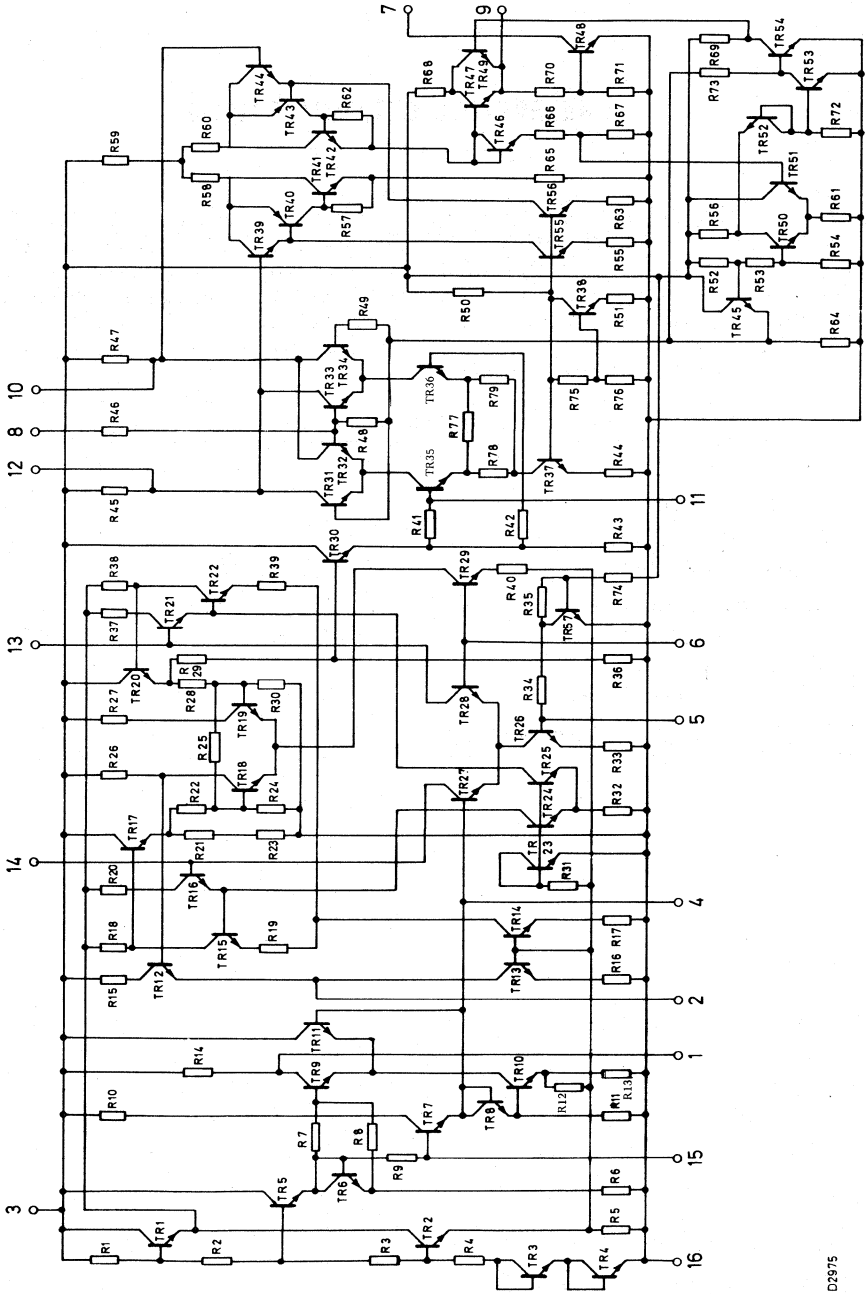
The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

QUICK REFERENCE DATA				
Supply voltage	V_{3-16}	nom.	12	V
Total current drain	I_3	typ.	33	mA
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1,5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output voltage range at correct phase of PAL switch	V_{9-16}		+4 to +0,2	V
at incorrect phase of PAL switch	V_{9-16}		+4 to +11	V

PACKAGE OUTLINES

TBA540 : 16-lead DIL; plastic (SOT-38).
TBA540Q: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{3-16}	max.	13.2	V
Power dissipation				
Total power dissipation at T_{amb} = 50 °C	P_{tot}	max.	680	mW
Temperatures				
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	−20 to	+60	°C

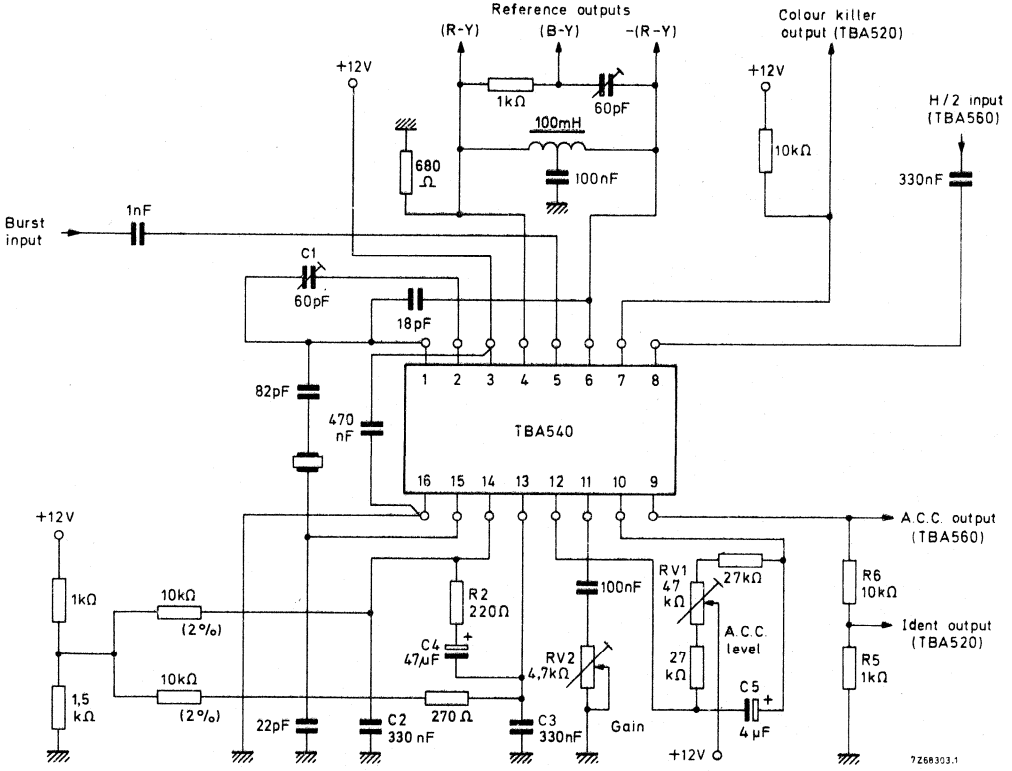
CHARACTERISTICS at V_{3-16} = 12 V; T_{amb} = 25 °C; $V_{5-16\,M}$ = 0.7 V (burst signal input); $V_{8-16(p-p)}$ = 2.5 V (P.A.L. square wave input) Measured in circuit shown on page 4.

Output signals				
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output signal range				
at correct phase of P.A.L. switch	V_{9-16}	+4 to	+0.2	V
at incorrect phase of P.A.L. switch	V_{9-16}	+4 to	+11	V
Oscillator section (amplifier)				
Input resistance	R_{15-16}	typ.	3.5	kΩ
Input capacitance	C_{15-16}	typ.	5	pF
Voltage gain	G_{15-1}	typ.	4.7	
Reactance control section				
Voltage gain with pins 13 and 14 interconnected	G_{15-2}	typ.	1.3	
Rate of change of gain G_{15-2} with phase difference between burst and reference signal	$\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$	typ.	5	$\frac{1}{\text{rad}}$
Supply current consumption	I_3	typ.	33	mA

PINNING

1. Oscillator feedback output
2. Reactance control stage feedback
3. Supply voltage (12 V)
4. Reference waveform output
5. Burst waveform input
6. Reference waveform input
7. Colour killer output
8. P.A.L. flip-flop square wave input
9. A.C.C. output
10. A.C.C. level setting (see also pin 12)
11. A.C.C. gain setting
12. A.C.C. level setting (see also pin 10)
13. } D.C. control points for
14. } oscillator phase control loop
15. Oscillator feedback input
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output
The crystal receives its energy from this pin. The input impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback
This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply
The maximum voltage must not exceed 13.2 V.

4. Reference waveform output
This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-(R-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input
A burst waveform amplitude of 1 V peak-to-peak is required to be a.c.-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5 The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input
This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output
This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input
A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. A.C.C. output
An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1) The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is excercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting
The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control
RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)

14. D.C. control points in reference control loop
Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d.c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3 and R_4, C_4. The d.c. potentials on these pins are nominally +7,2 V.

15. Oscillator feedback input
The input impedance at this pin is nominally 3.5 kΩ in parallel with 5 pF. No d.c. connection is required on this pin. The voltage in the i.c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)

PERFORMANCE AND COMMENTS

Initial adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.

(c) Set the a.c.c. level adjustment RV1, to give +4 V on pin 9.

(d) Apply burst signal.

(e) Adjust a.c.c. gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, $\pm 10^{o}$.

(b) Typical holding range, ± 600 Hz.

(c) Typical pull-in range, ± 300 Hz.

(d) Temperature coefficient of oscillator frequency, i.c. only, 2 Hz/^{o}C.

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560C is a monolithic integrated circuit used in the decoding system of colour television receivers. The circuit consists of a luminance and a chrominance amplifier.
The luminance amplifier input is matched to the luminance delay line and performs the following functions:
d.c. contrast control * brightness control * black level clamping * blanking.

The chrominance amplifier comprises:
gain-controlled amplifier * chrominance gain control tracked with contrast control * separate d.c. saturation control * PAL delay line driver * burst gate * colour killer.

QUICK REFERENCE DATA

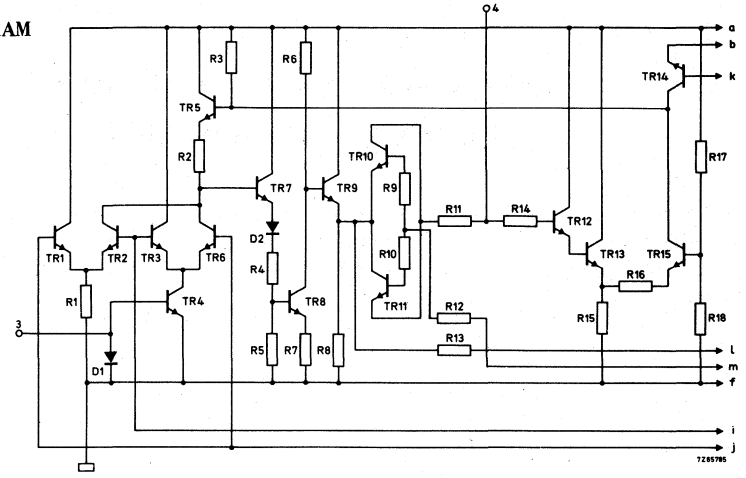
Supply voltage	V_{11-16}	nom.	12	V	
Supply current	I_{11}	nom.	30	mA	
Luminance signal input current	$I_{3(p-p)}$	typ.	1,5	mA	
Chrominance input signal	$V_{1-15(p-p)}$	>	4	mV	
		<	80	mV	
Luminance output signal at nominal contrast setting	$V_{5-16(p-p)}$	typ.	3	V	[1]
Chrominance output signal at nominal contrast and saturation setting	$V_{9-16(p-p)}$	typ.	1	V	[1]
Contrast control range		≥	20	dB	
Saturation control range		≥	20	dB	
Burst output (closed a.c.c. loop)	$V_{7-16(p-p)}$	typ.	1	V	

[1]) Nominal setting: maximum contrast and/or saturation minus 6 dB

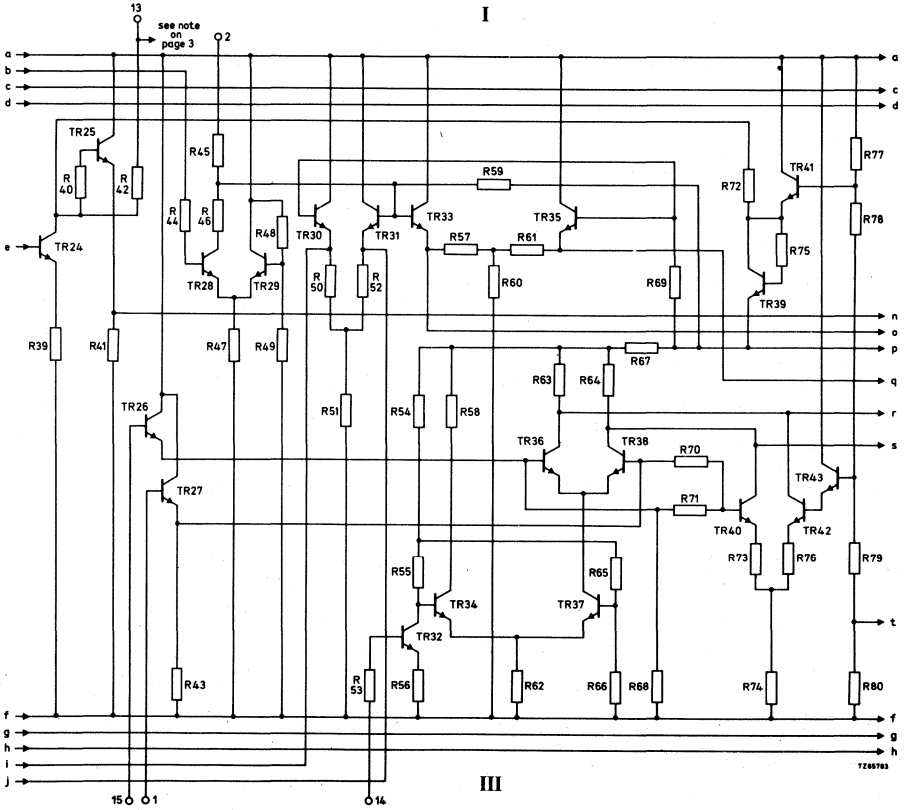
PACKAGE OUTLINES

TBA560C : 16-lead DIL; plastic (SOT-38).
TBA560CQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM

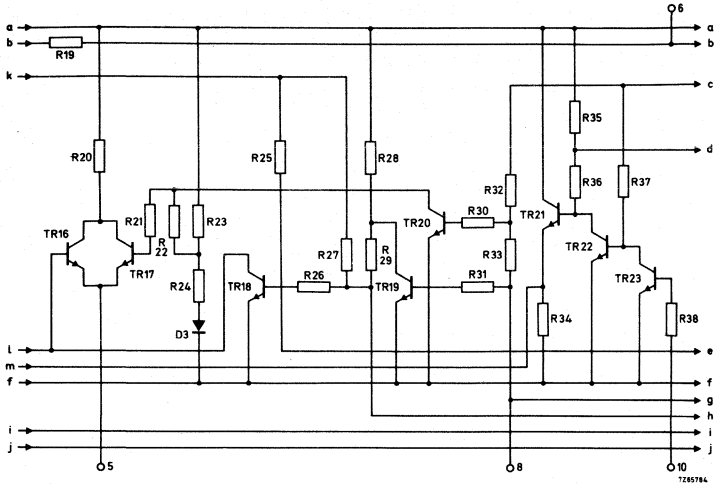


I

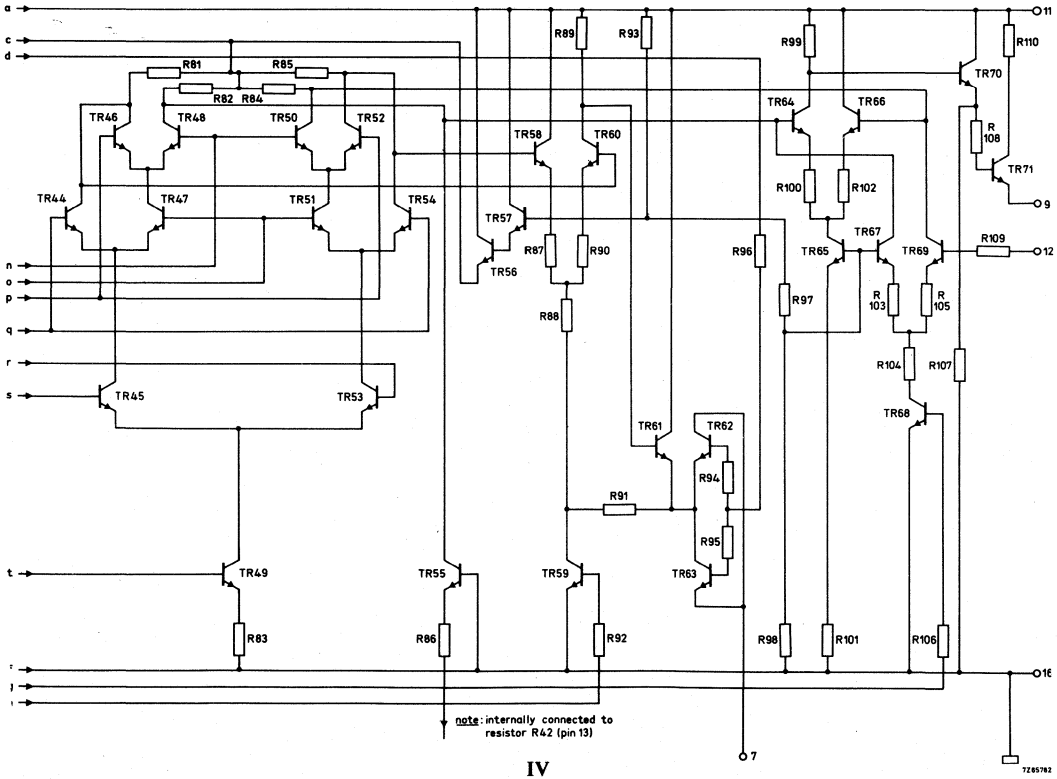


III

Note: the circuits are interconnected in the numerical sequence I, II, III, IV


a
b
k
l
m
f
i
j
R19
R20
R25
R28
R32
R35
R36
R37
R30
TR16
R21
R 22
R23
TR17
R24
D3
TR18
R26
R27
R 29
TR19
TR20
TR21
TR22
TR23
R31
R33
R34
R38
6
5
8
10
c
d
e
g
h
7Z65784

II


a
c
d
n
o
p
q
r
s
t
u
v
w
R81
R85
R82
R84
TR46
TR48
TR50
TR52
TR44
TR47
TR51
TR54
TR45
TR53
TR49
R83
R89
R93
TR58
TR60
TR57
TR56
R87
R90
R88
R91
TR61
TR62
R94
R95
TR63
TR55
TR59
R86
R92
note: internally connected to resistor R42 (pin 13)
7
R99
R110
TR70
TR64
TR66
R 108
TR71
R100
R102
9
TR67
R109
12
TR65
TR69
R96
R97
R 103
R 105
R104
R107
TR68
R98
R101
R106
11
16
7Z65782

IV

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage	V_{11-16}	max.	13	V [1]

Power dissipation

Total power dissipation	P_{tot}	max.	510	mW [1]

Temperatures

Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	0 to +60	°C

Voltages with respect to pin 16

V_{1-16}	0 to +5 V	V_{10-16}	min. −5 V
V_{2-16}	0 to +12 V [2]	V_{12-16}	−5 to +6 V
V_{4-16}	0 to +6 V	V_{13-16}	−3 to +6,5 V [2]
V_{6-16}	0 to +3 V	V_{14-16}	min. −5 V
V_{8-16}	−5 to +5 V	V_{15-16}	0 to +5 V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1 mA	I_7	−3 to +2 mA
I_3	−1 to +3 mA	I_9	−10 to 0 mA
I_5	−5 to 0 mA	I_{10}	max. +3 mA
I_6	−1 to +1 mA	I_{14}	max. +1 mA
		I_{15}	0 to +1 mA

1) Permissible while tubes are heating up: V_{11-16} max. 16 V and P_{tot} max. 700 mW.

2) V_{2-16} and V_{13-16} must always be lower than V_{11-16}.

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{11-16}	typ.	12	V	
			10 to 13	V	
Required input signals at V_{11-16} = 12 V and T_{amb} = 25 °C					
Chrominance input signal					
peak-to-peak value	$V_{1-15(p-p)}$		4 to 80	mV	
Luminance input current					
black-to-white value	I_3	typ.	1,5	mA	
Contrast control voltage range					
for 20 dB of control	V_{2-16}	see graph on page 11			
Brightness control voltage	V_{6-16}	see graph on page 11			[1]
Saturation control voltage range					
for 20 dB of control	V_{13-16}	see graph on page 11			
Burst keying pulse (positive)					
peak-to-peak value	$I_{10(p-p)}$		0,05 to 1	mA	
Fly-back blanking pulses (negative)					
peak-to-peak value					
for 0 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−0,5	V	
for 1,5 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	−2,5	V	
Colour killer	V_{13-16}	<	1	V	
Automatic chrominance control starting	V_{14-16}	typ.	1,2	V	[2]

[1] When V_{6-16} is increased above 1,7 V the black level of the output signal remains at 2,7 V

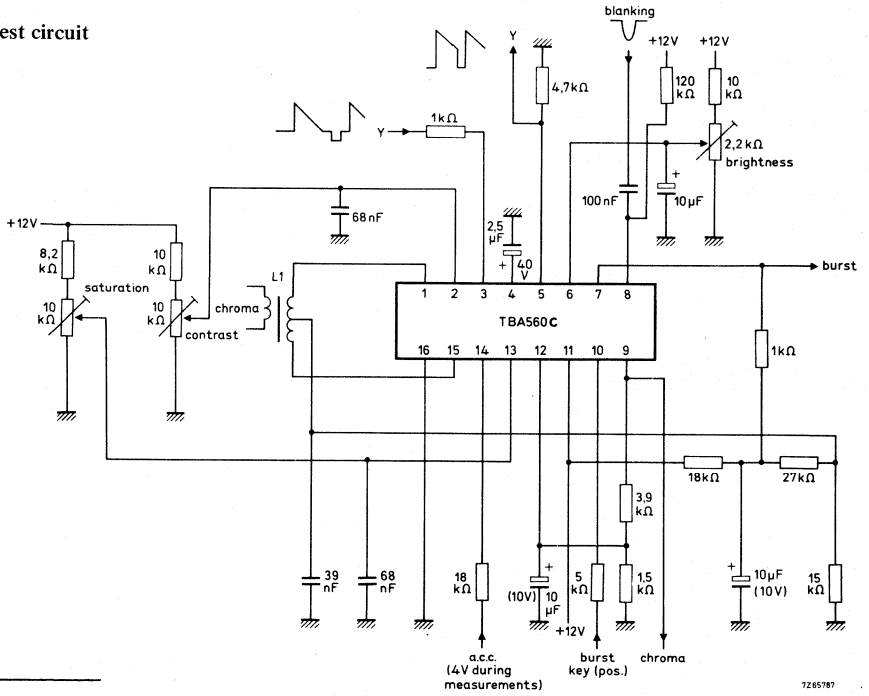
[2] A negative going potential provides a 26 dB a.c.c. range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of min. 500 mV.

CHARACTERISTICS (continued)

Obtainable output signals

Luminance output voltage at nominal contrast (peak-to-peak value)	$V_{5-16(p-p)}$	typ.	3	V	[1]
Burst signal (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	1	V	[2]
Chrominance signal at nominal contrast and saturation (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V	[1]
3 dB bandwidth of chrominance and luminance amplifier	B	typ.	5	MHz	
Change of ratio luminance to chrominance signals at 10 dB contrast control		<	2	dB	

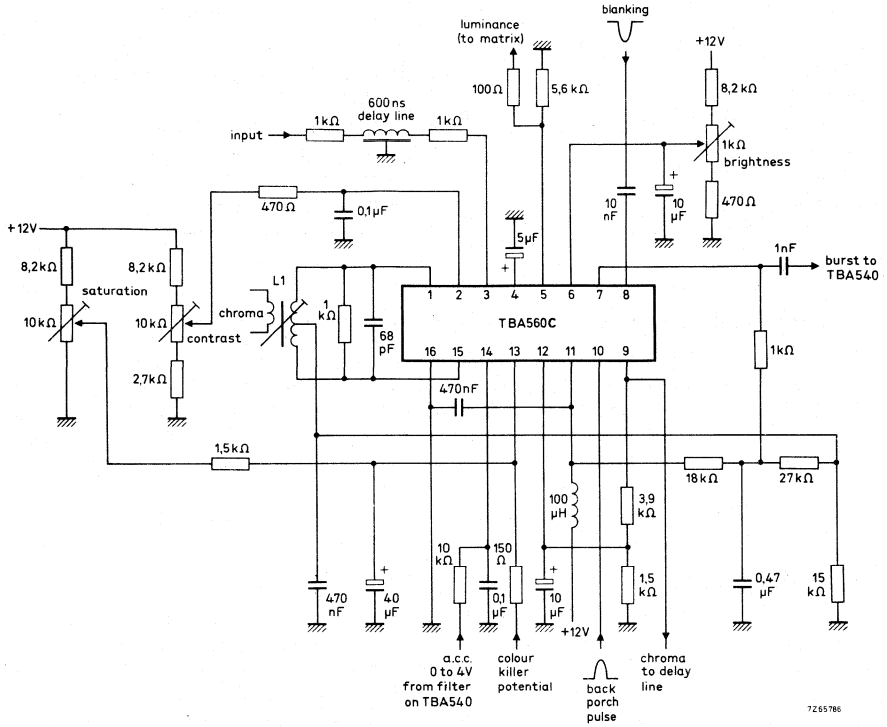
Test circuit



[1]) Nominal setting: maximum contrast and/or saturation minus 6 dB.

[2]) Burst signal is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Application diagram for operation in combination with the TBA540.

APPLICATION INFORMATION (continued)

Pinning

1. Balanced chroma signal input
2. Contrast control
3. Luminance signal input
4. Black level clamp capacitor
5. Luminance signal output
6. Brightness control
7. Burst output
8. Fly-back blanking input
9. Chroma signal output
10. Burst gate and clamping pulse input
11. Supply voltage (12 V)
12. D.C. feedback for chroma channel
13. Chroma saturation control
14. A.C.C. input
15. Chroma signal input
16. Earth (negative supply)

The function is quoted against the corresponding pin number

1. Balanced chroma signal input (in conjunction with pin 15)

   This is derived from the chroma signal bandpass filter, designed to provide the push-pull input. An input signal amplitude of at least 4 mV peak-to-peak is required on pins 1 and 15. Both pins require a d.c. potential of approximately +3,0 V. This is derived as a common-mode signal from a network connected to pin 7 (burst output). In this way d.c. feedback is provided over the burst channel to stabilise its operation.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chroma ratio of input signal is 1 : 2.

2. D.C. contrast control

   With +3,7 V on this pin, the gain in the luminance channel is such that a 1,5 mA peak-to-peak input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 3 V black-to-white. A variation of voltage on pin 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > −14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.

3. Luminance signal input

   This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1,5 mA black-to-white amplitude.

4. Charge storage capacitor for black level clamp (5,0 μF)

5. Luminance signal output

   An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, not less than 1 kΩ.
   Black level shift at contrast control is max. ± 20 mV if the luminance input current during black level is about 0,75 mA. When this current has a different value a larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0,75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current the black level shift will be correspondingly smaller.
   Black level shift with video signal content occurs only when the input signal is a.c. coupled. The value depends on the drive current amplitude and can be calculated from

APPLICATION INFORMATION (continued)

the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).
Black level shift over an ambient temperature variation of 30 °C is typ. −140 mV.

6. The d.c. level of the luminance output signal may be controlled by the d.c. potential applied to this pin

Over the range of potential +0, 9 to +1, 7 V the black level of the luminance output signal (pin 5) is increased from 0 to +2, 7 V. The output signal black level remains at +2, 7 V when the potential on pin 6 is increased above +1, 7 V.

7. Burst output

A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here. Also, to achieve good d.c. stability by negative feedback in the burst channel the d.c. potential at this pin is fed back to pins 1 and 15 via the chroma input transformer. When limiting occurs the burst amplitude is min. 2, 5 V.

8. Fly-back blanking input waveform

Negative-going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1 V negative excursion are applied the signal level at the luminance output (pin 5) during blanking will be 0 V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3 V the signal level at the luminance output during blanking will be +1, 5 V.

9. Chroma signal output

With an 1 V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1 V peak-to-peak. An external d.c. network is required which provides negative feedback in the chroma channel via pin 12.

10. Burst gating and clamping pulse input

A positive pulse of minimum 50 µA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.

11. +12 V L.T power supply

Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 550 mW at 60 °C ambient temperature.

12. D.C. feedback for chroma channel (see pin 9)

13. Chroma saturation control

A control range of +6 to > +14 dB is provided over a range of d.c. potential on pin 13 from +2, 7 to +6, 2 V. Colour killing is also done at this terminal by reducing the d.c. potential to less than +1 V, e.g., from the TBA540 colour killer output terminal. The kill factor is min. 40 dB.

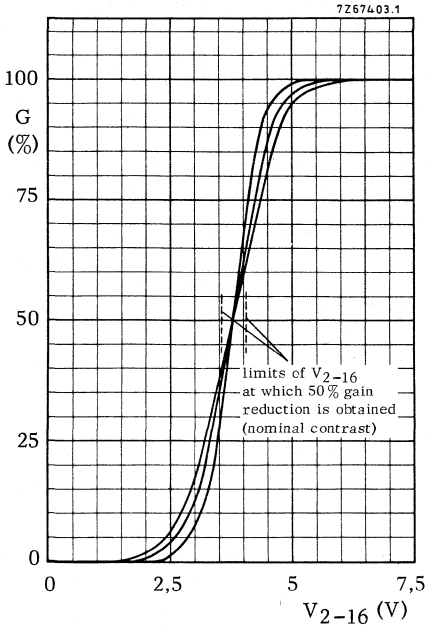
APPLICATION INFORMATION (continued)

14. A.C.C. input

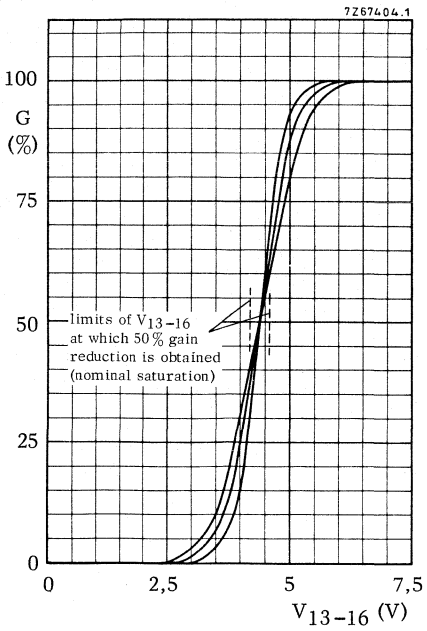
    A negative-going potential gives a 26 dB range of a.c.c. starting at +1, 2 V and giving maximum gain reduction at an input voltage of min. 500 mV.

15. Chroma signal input (see pin 1)

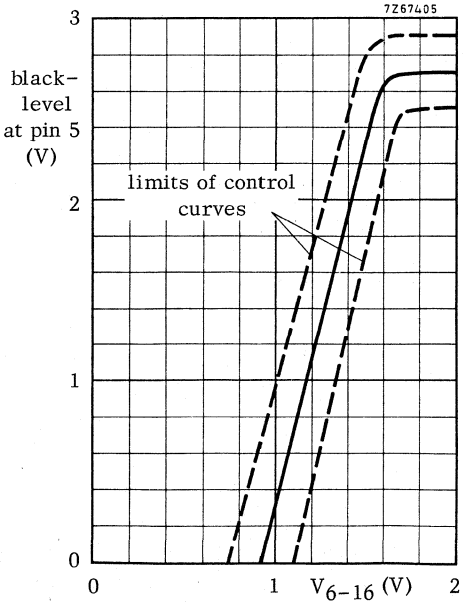
16. Negative supply (earth)



Contrast control of luminance amplifier



Saturation of chrominance amplifier



Control of black level at output luminance amplifier

LINE OSCILLATOR CIRCUIT

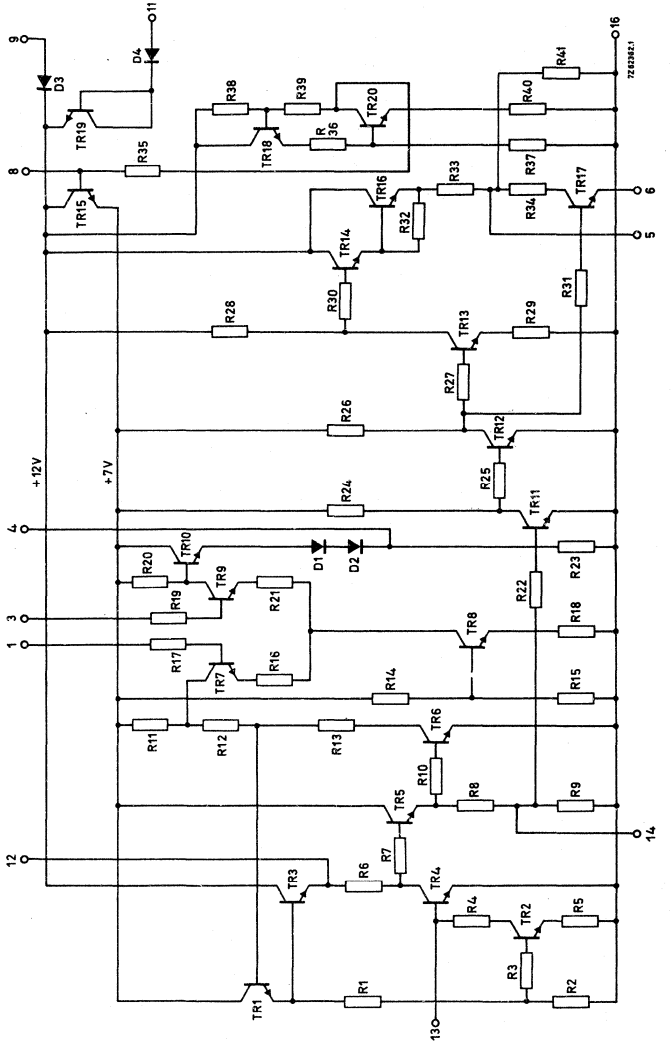
This circuit has been designed for use as line-oscillator and reactance stage in colour and monochrome t.v. receivers.
The circuit consists of a Miller-integrator-oscillator followed by a pulse shaping circuit, which delivers a positive pulse of 8 V and adjustable width. The available output current is in excess of 60 mA. Finally a supply voltage take-over switch for starting purposes is built in. The TBA720A can co-operate with the TBA890.

QUICK REFERENCE DATA			
Supply voltage	V_{11-16}	typ.	12 V
Starting voltage	V_{9-16}	8 to 12	V
Required input signals			
D.C. control voltage at pin 1	V_{1-16}	2,4 to 5,3	V
at pin 3	V_{3-16}	2,4 to 5,3	V
Delivered output signals			
Output voltage at pin 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ. 8	V
Output current at pin 5	I_5	< 60	mA

PACKAGE OUTLINES

TBA720A : 16-lead DIL; plastic (SOT-38).
TBA720AQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages			
Supply voltage	V_{11-16}	max.	16 V
Starting voltage	V_{9-16}	max.	15 V
Currents			
Output current	I_5	max.	60 mA
Power dissipation			
Total power dissipation when mounted on a printed-wiring board	P_{tot}	max.	280 mW
Temperatures			
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		0 to +60 °C

CHARACTERISTICS Measured in the test set-up on page 4

Supply voltage	V_{11-16}	typ.	12 V 10 to 13 V
Starting voltage	V_{9-16}	>	8 V [1]

CHARACTERISTICS at T_{amb} = 25 °C; V_{11-16} = 12 V

Supply current [2]	I_{11}	typ.	10,5 mA 7,5 to 13,5 mA
Required input signals			
D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3	$V_{1-16} = V_{3-16}$		2,4 to 5,3 V
Sensitivity of reactance stage	V_{1-3}	typ.	2 kHz/V
Duty cycle regulation at pin No. 14	I_{14}	typ.	0 μA +400 to −400 μA
Delivered output signals			
Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8 V
Output current	I_5	<	60 mA
Duty cycle; without regulation	δ	typ.	40 % 35 to 45 %
with regulation	δ		20 to 60 %
Rise time at pin No. 5 leading edge of output pulse	t_r	typ.	200 ns

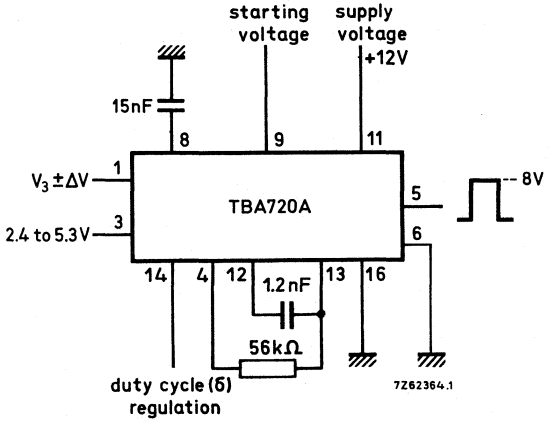
[1] Maximum starting voltage should not exceed the value of the supply voltage minus 1 volt.

[2] No load connected to the output. When the output is loaded, the extra current is: δ x I, in which δ = duty cycle of output pulse and I = current flowing during output pulse.

CHARACTERISTICS (continued)

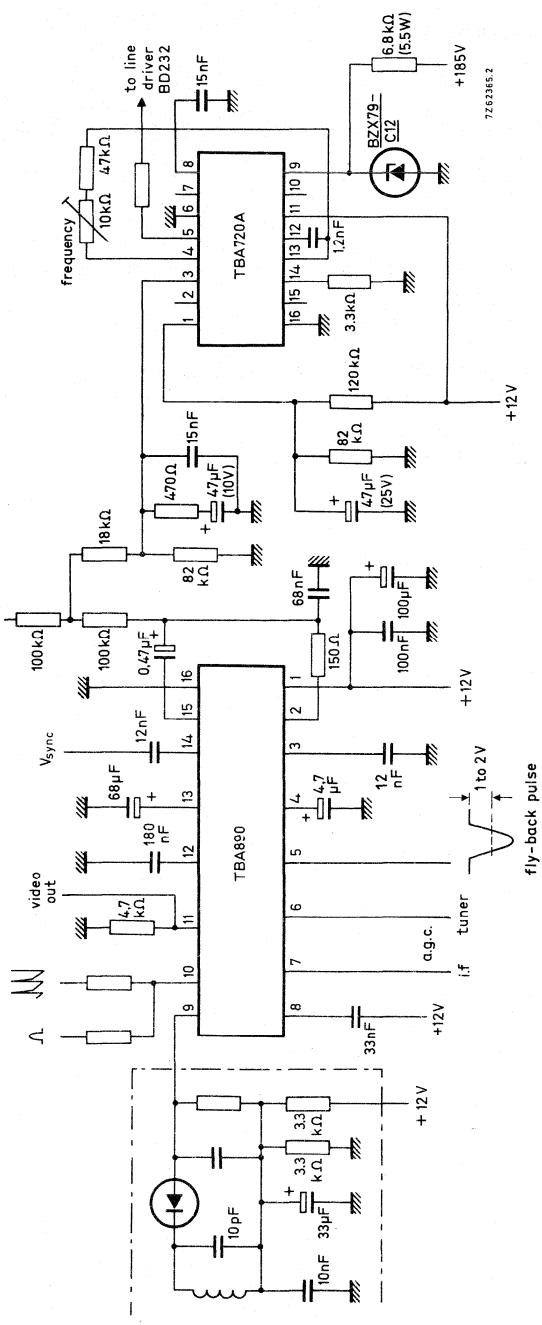
Relative frequency deviation for ΔV_{11} = 1 V			2 ‰
Relative frequency deviation for change of ambient temperature 25 to 55 °C			3 ‰
Allowable hum-ripple on supply line (peak-to-peak value)	$\Delta V_{11\text{-}16(p\text{-}p)}$	typ.	100 mV

Test set-up



APPLICATION INFORMATION

The TBA720A with the TBA890 or TBA900 in a receiver with transistorized line deflection.



APPLICATION INFORMATION (continued)

Notes

1. The TBA720A is intended to drive a line deflection circuit equipped with transistors.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and ground or the supply.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequency deviation is limited to $\pm$1,3 kHz to safeguard the line timebase output circuits.
5. Besides the oscillator, the TBA720A incorporates a reactance stage and a supply voltage take-over switch for starting purposes (pin 9). The latter can be used to advantage if the 12 V supply is derived from the line flyback pulse.
6. Pins 2, 7, 10 and 15 should not be connected.

LIMITER/AMPLIFIER

The TBA750C is a limiter/amplifier with f.m. detector, d.c. volume control and a.f. preamplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz. The limiter/amplifier is a four-stage differential amplifier that gives very good noise and interference suppression. The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB. The a.f. preamplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

QUICK REFERENCE DATA

Supply voltage	V_{2-5}	typ	12 V
Total current drain	I_{tot}	typ	34 mA
Frequency	f_o		5,5 MHz
Input voltage at start of limiting	$V_{i\ lim}$	typ	130 μV
A.M. rejection at V_i = 1 mV	α	typ	45 dB
A.F. output voltage at $\Delta f = \pm$ 15 kHz at pin 16	$V_{o(rms)}$	typ	2,7 V
D.C. volume control range		>	80 dB

PACKAGES OUTLINES

TBA750C: 16-lead DIL; plastic (SOT-38).
TBA750CQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM

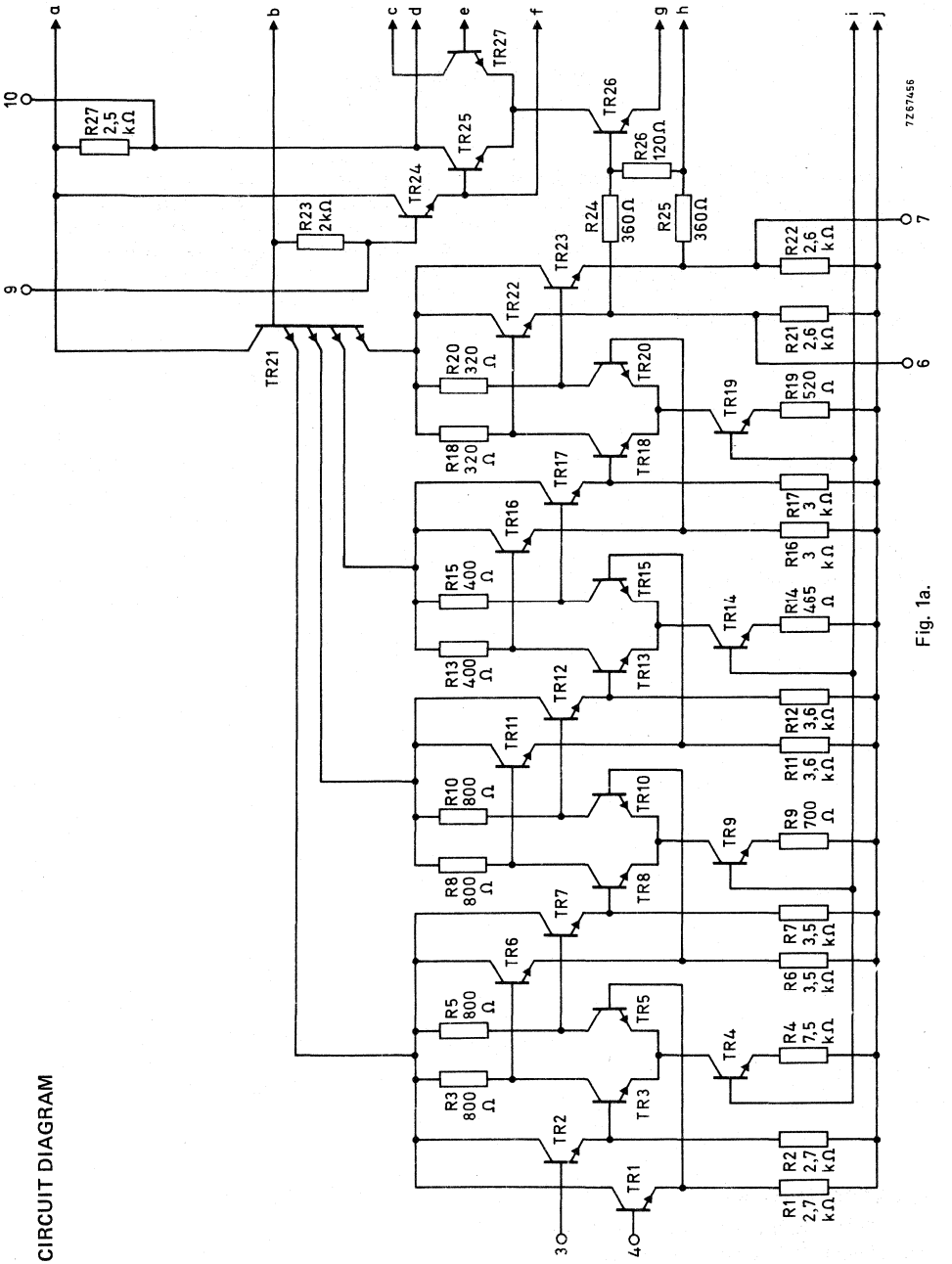


Fig. 1a.

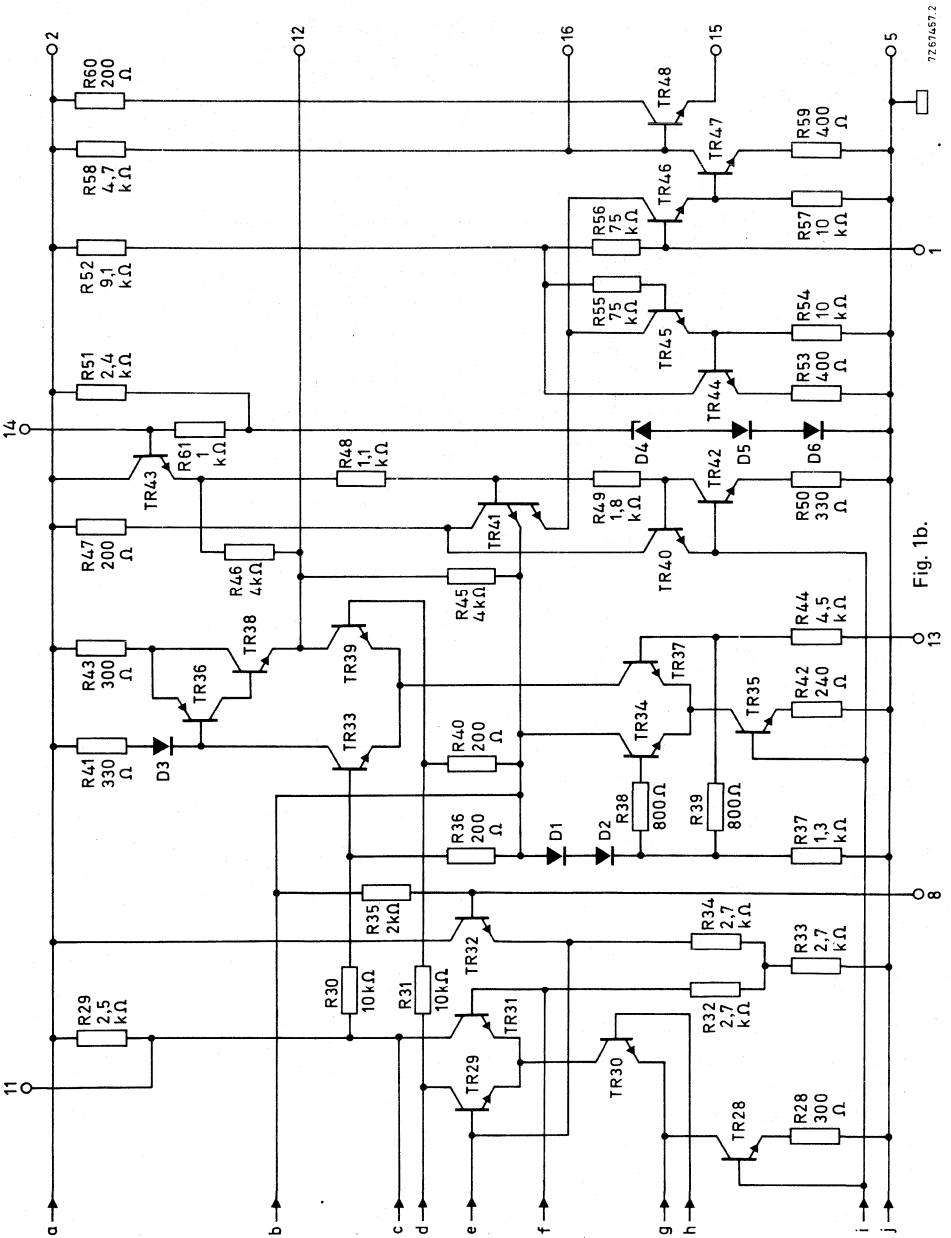

2
12
16
15
5
14
11
1
13
8
a
b
c
d
e
f
g
h
i
j
R60 200 Ω
R58 4,7 kΩ
R52 9,1 kΩ
R51 2,4 kΩ
R61 1 kΩ
R47 200 Ω
R46 4kΩ
R43 300 Ω
R41 330 Ω
R29 2,5 kΩ
R48 1,1 kΩ
R45 4kΩ
R40 200 Ω
R36 200 Ω
R35 2kΩ
R30 10kΩ
R31 10kΩ
R49 1,8 kΩ
R56 75 kΩ
R55 75 kΩ
R59 400 Ω
R57 10 kΩ
R54 10 kΩ
R53 400 Ω
R50 330 Ω
R44 4,5 kΩ
R42 240 Ω
R38 800Ω
R39 800Ω
R37 1,3 kΩ
R34 2,7 kΩ
R33 2,7 kΩ
R32 2,7 kΩ
R28 300 Ω
TR43
TR36
TR38
TR39
TR33
TR41
TR48
TR47
TR46
TR45
TR44
TR42
TR40
TR37
TR35
TR34
TR32
TR31
TR29
TR30
TR28
D1
D2
D3
D4
D5
D6
7267457.2

Fig. 1b.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{2-5}	max	16 V *
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 55 °C
Power dissipation			

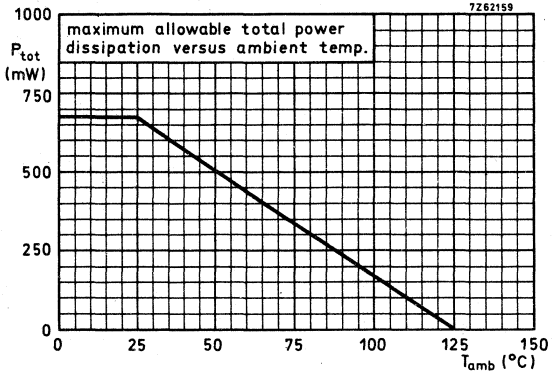


Fig. 2.

CHARACTERISTICS

Measured in test circuit Fig. 3.

Supply voltage range see also Fig. 4	V_{2-5}		10 to 25 V
Total current drain; pin 15 not connected	I_2		25 to 45 mA
Input limiting voltage at V_o = −3 dB (r.m.s. value)	$V_{i\ lim(rms)}$	typ	130 μV
I.F. output voltage at pins 6 and 7 (peak-to-peak value)	$V_{6-5(p-p)}$) $V_{7-5(p-p)}$)	typ	380 mV
A.M. rejection			
V_i = 1 mV	α	typ	45 dB
V_i = 10 mV	α	typ	50 dB
V_i = 100 mV	α	typ	55 dB
D.C. volume control range; see also Fig. 5		>	80 dB
A.F. preamplifier voltage gain pin 1 to pin 16	G_v	typ	10
Input resistance at pin 1	R_i	⩾	35 kΩ

* Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply (see also Fig. 4).

CHARACTERISTICS (continued)

A.F. output voltages (r.m.s. values) $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz			
	$V_{10-5(rms)}$ } $V_{11-5(rms)}$ }	typ	65 mV
	$V_{12-5(rms)}$	typ	250 mV
	$V_{16-5(rms)}$	typ	2,7 V
Total harmonic distortion			
at pin 12; $\Delta f = 15$ kHz	d_{tot}	typ	3 %
at pin 1 with respect to pin 16; $V_{o(rms)} = 3$ V	d_{tot}	typ	2,6 %

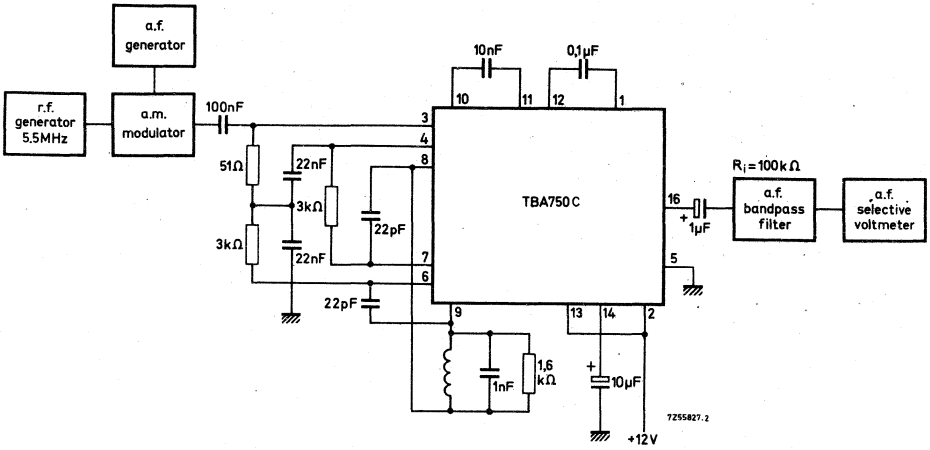


Fig.3 Test circuit; for f.m.: $f_o = 5{,}5$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 70$ Hz. For a.m.: $m = 0{,}3$; $f_m = 1$ kHz.

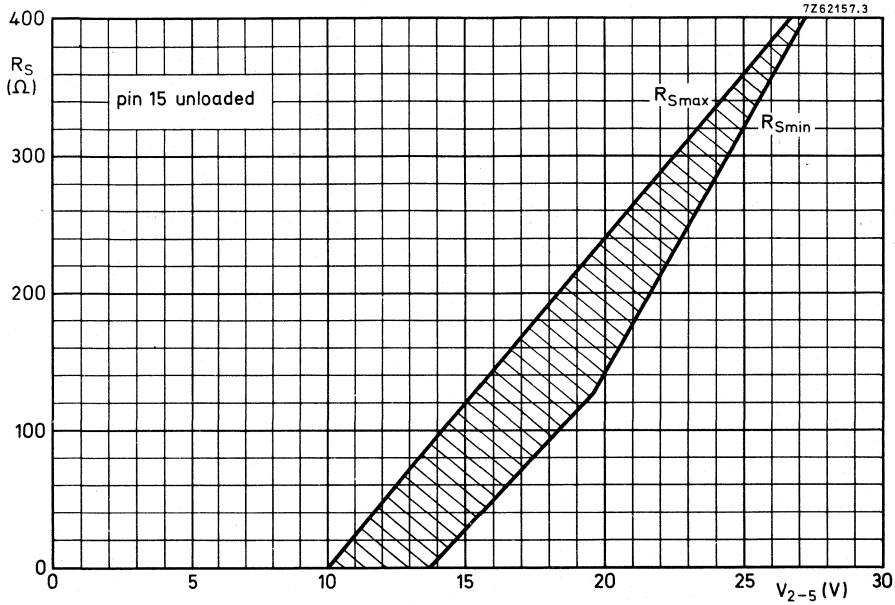


Fig. 4 Maximum and minimum values for the power supply series resistance (R_S).

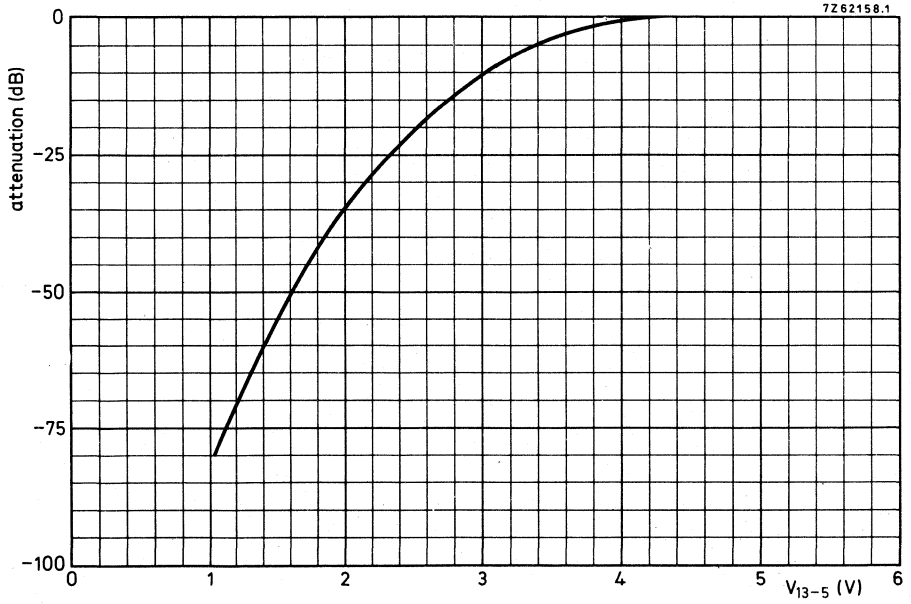


Fig. 5 Remote control characteristic.

APPLICATION INFORMATION at f = 5,5 MHz

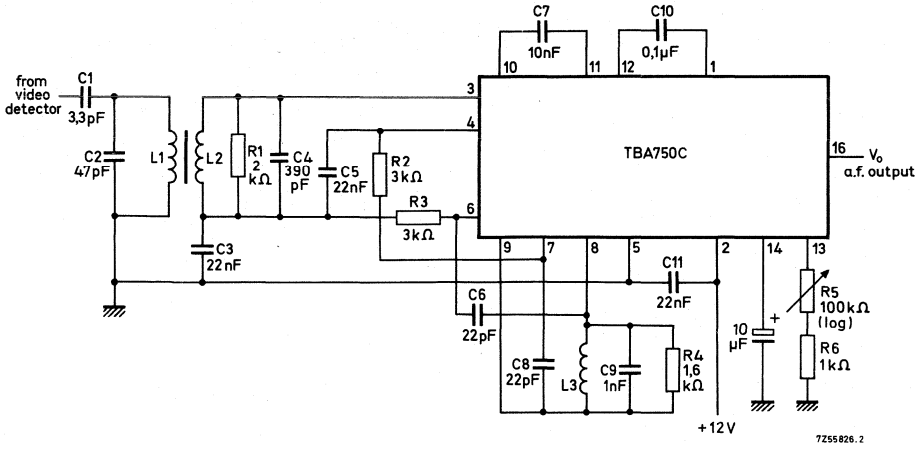


Fig. 6.

L1 = 18 μH; Q_{L1} = 36
L2 = 2,2 μH; Q_{L2} = 21
L3 = 0,84 μH; Q_{L3} = 22

Note

Q_{L1}, Q_{L2} and Q_{L3} are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1}$ = 0,54.

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

TELEVISION SIGNAL PROCESSING CIRCUIT

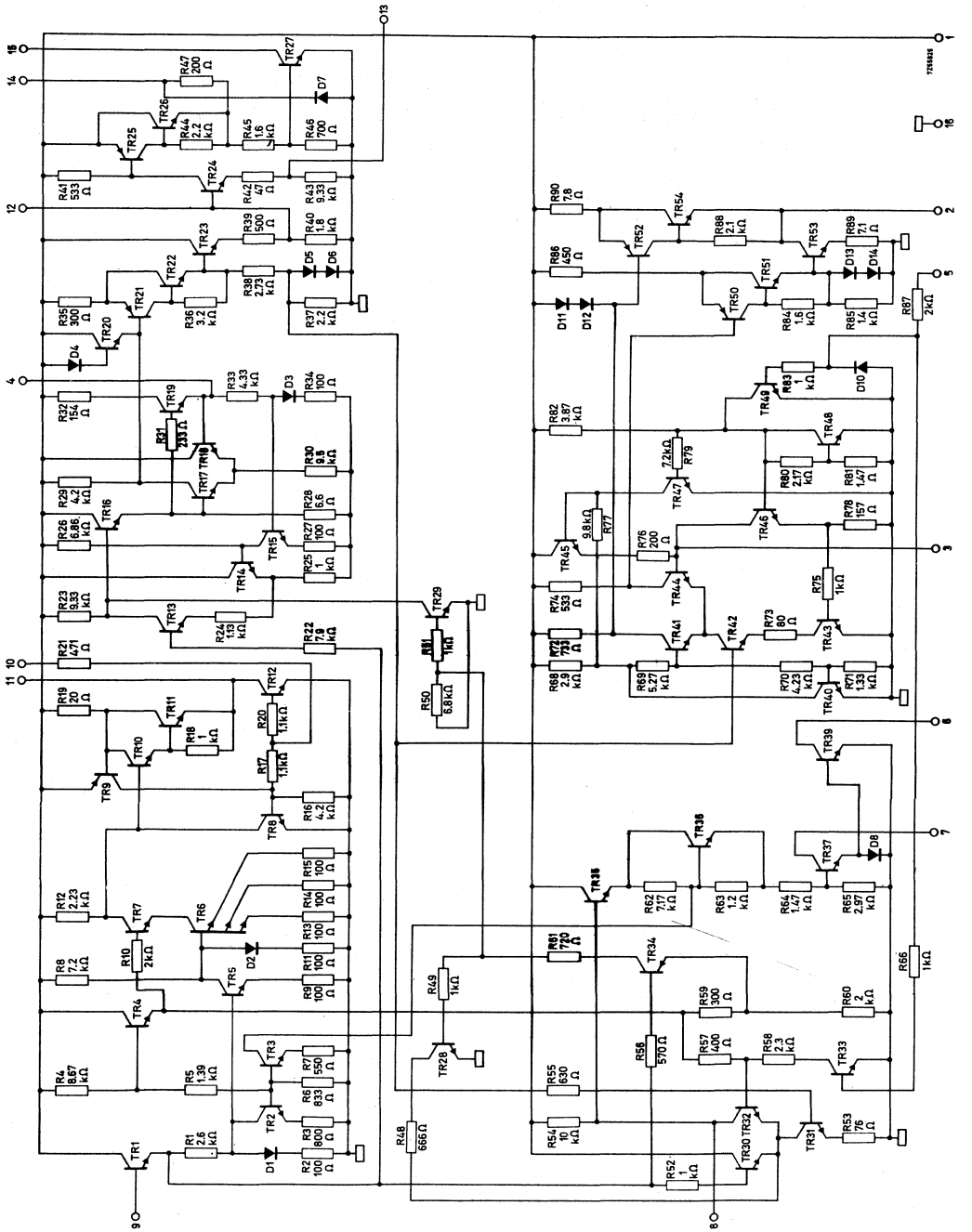
The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.
It combines the following functions:
- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.
The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V
Voltage gain of the video amplifier	G_v	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}	1,0 to	12	V
A.G.C. voltage for tuner	V_{6-16}	0,3 to	12	V
Output voltage range horizontal phase detector	V_{2-16}	2 to	10	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

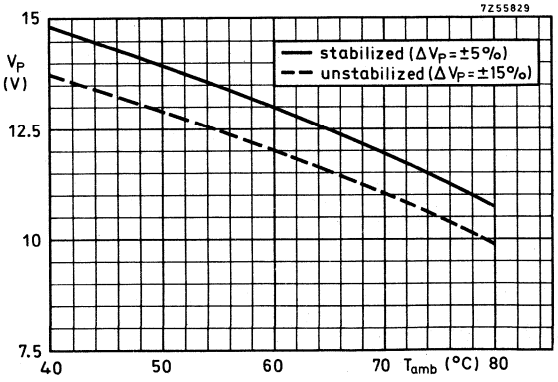
PACKAGE OUTLINES

TBA890 : 16-lead DIL; plastic (SOT-38).
TBA890Q: 16-lead QIL; plastic (SOT-58).



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.		20	V [1]
Power dissipation	P_{tot}	max.		700	mW
Temperatures					
Storage temperature	T_{stg}	-55	to	+125	°C
Operating ambient temperature	T_{amb}	-25	to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

[1] Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range	V_P	See curves on page 3		

The following characteristics are measured in the circuit on p. 7 at T_{amb} = 25 °C; V_P = 12 V.

Video amplifier				
Input resistance	R_{9-16}	>	30	kΩ
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	t_r; t_f	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V[1]
D.C. bias video detector voltage	V_{bias}	typ.	6	V[2]
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V[1]
Black level at the output	V_{11-16}	typ.	5	V[3]
Available video output current (peak value)	I_{11M}	≤	30	mA[4]
Tolerances on the video output voltages				
I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV[5]
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV[6]
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

I.C. processing spreads	$\pm\Delta V_{11\text{-}16}$	<	420	mV[1]
Temperature drift	$-\Delta V_{11\text{-}16}$	typ.	1.7	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11\text{-}16}$	<	130	mV[2]
Supply voltage	$\frac{\Delta V_{11\text{-}16}}{\Delta V_P}$	typ.	0.4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		1 to 5	V
Input resistance	$R_{10\text{-}16}$	typ.	1	kΩ
Output voltage during blanking	$V_{11\text{-}16}$	<	500	mV

A.G.C. circuit

Range of control voltage i.f. amplifier	$V_{7\text{-}16}$		1 to 12	V[3]
Range of control voltage tuner	$V_{6\text{-}16}$		0.3 to 12	V[3]
Signal expansion for full control of i.f. amplifier and tuner		typ.	0.5	dB
Current i.f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	20	mA
Current i.f. control point for tuner take-over	I_7	see note 4		
Keying input pulse (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	see note 5		
Input resistance	$R_{5\text{-}16}$	typ.	2	kΩ

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i.f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit				
Sync. separator			see note 1	
Output voltage range of phase detector	V_{2-16}		2 to 10	V [2]
Control steepness	S_φ	typ.	2.5	V/μs [3]
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ.	1.5	μs
Variation φ_0 caused by internal spreads	$\pm\Delta_{\varphi 0}$	typ.	0.3	μs [4]
Output voltage range as a frequency detector	V_{2-16}		4 to 8	V [5]
Vertical synchronization circuit				
Output voltage vertical sync. pulse generator	V_{14-16}	typ.	11	V
Output impedance	R_{14-16}	typ.	2	kΩ

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

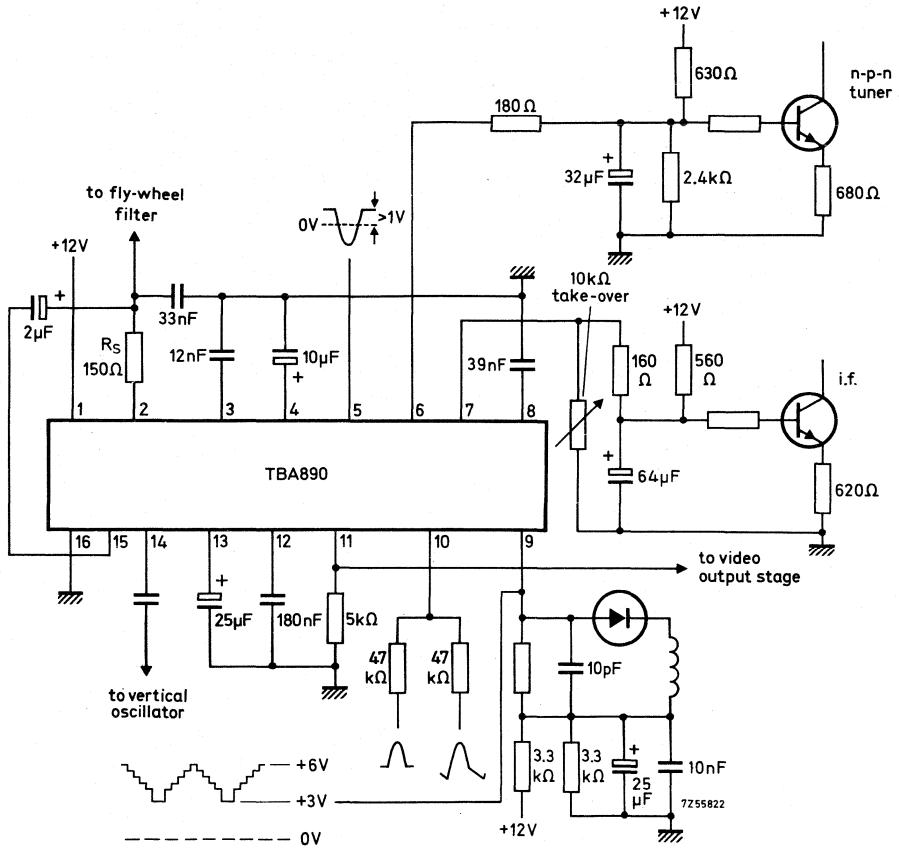
2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example R_S = 56 Ω, S_φ = 5 V/μs and R_S = 0, S_φ = ≥25 V/μs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION



HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor-thyristor-or tube equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loopgain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA				
Supply voltage	V_{1-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Input signals				
Video input voltage (positive-going sync) top sync to white value	$V_{8-16(p-p)}$	typ.	3 1 to 7	V V
Noise gate input current (peak value)	I_{9M}	>	30	μA
Input resistance of noise gate	R_{9-16}	typ.	200	Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1	V
Flyback signal input current (peak value)	I_{5M}	typ.	1	mA
Output signals				
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V
Line driver output current (average value)	$I_{2(AV)}$	max.	20	mA
Line driver output current (peak value)	I_{2M}	max.	200	mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10	V

PACKAGE OUTLINES

TBA920 : 16-lead DIL; plastic (SOT-38).
TBA920Q: 16-lead QIL; plastic (SOT-58).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Supply voltage	V_{1-16}	max.	13,2	V
Pin No. 3 voltage	V_{3-16}		0 to 13,2	V
Pin No. 8 voltage	$-V_{8-16}$	max.	12	V
Pin No. 10 voltage	V_{10-16}		−0,5 to +5	V
Currents				
Pin No. 2 current (average value)	$I_{2(AV)}$	max.	20	mA
(peak value)	I_{2M}	max.	200	mA
Pin No. 5 current (peak value)	I_{5M}	max.	10	mA
Pin No. 7 current (peak value)	I_{7M}	max.	10	mA
Pin No. 8 current (peak value)	I_{8M}	max.	10	mA
Pin No. 9 current (peak value)	I_{9M}	max.	10	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	600	mW [1]
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C

Measured in circuit on page 6 (CCIR standard).

Current consumption at $I_2 = 0$	I_1	typ.	36	mA
Required input signals				
Video signal				
Input voltage (positive going sync) peak-to-peak value	$V_{i(p-p)}$	typ.	3	V
			1 to 7	V
Input current during sync pulse (peak value)	I_{8M}	typ.	100	μA
Noise gating (pin 9)				
Input voltage (peak value)	V_{9-16M}	>	0,7	V
Input current (peak value)	I_{9M}	>	30	μA
		<	10	mA
Input resistance	R_{9-16}	typ.	200	Ω

1) 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Flyback pulse (pin 5)

Input voltage (peak value)	V_{5-16M}	typ.	±1	V	
Input current (peak value)	I_{5M}	>	50	µA	
		typ.	1	mA	
Input resistance	R_{5-16}	typ.	400	Ω	
Pulse duration at 15625 Hz	t_5	>	10	µs	

Delivered output signals

Composite sync pulses (positive; pin 7)

Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	10	V	
Output resistance					
at leading edge of pulse (emitter follower)	R_{7-16}	≈	50	Ω	
at trailing edge	R_{7-16}	typ.	2, 2	kΩ	
Additional external load resistance	$R_{7-16(ext)}$	>	2	kΩ	

Driver pulse (pin 2)

Output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V	
Average output current	$I_{2(AV)}$	<	20	mA	
Peak output current	I_{2M}	<	200	mA	
Output resistance (low ohmic)	R_{2-16}	typ.	2,5 or 15	Ω	[1]
Output pulse duration when synchronised	t_2		12 to 32	µs	[2]
Permissible delay between leading edge of output pulse and flyback pulse at t_5 = 12 µs	$t_{o\ tot}$		0 to 15	µs	
Supply voltage at which output pulses are obtained	V_{1-16}	>	4	V	

[1]) Depends on switch position and polarity output current. R_{2-16} = 2, 5 Ω is valid for V_{2-16} = ± 10, 5 V and a load between pins 2 and 16 (e.g. an external resistor).

[2]) The output pulse duration is adjusted by shifting the leading edge (V_{3-16} from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.
For a line output stage with a BU108 high voltage transistor the resulting duration is about 22 µs, and in such a way that the line output transistor is switched on again about 8 µs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

CHARACTERISTICS (continued)

Oscillator

Frequency; free running (R_{15-16} = 3,3 kΩ)	f_o		15 625	Hz	1)
Spread of frequency at nominal values of peripheral components	$\frac{\Delta f_o}{f_o}$	<	±5	%	2)
Frequency change when decreasing the supply down to minimum 4 V	$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$	<	10	%	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5	Hz/μA	
Adjustment range of network in circuit on page 6	$\frac{\Delta f_o}{f_o}$	typ.	±10	%	
Influence of supply voltage on frequency at V_P = 12 V	$\frac{\delta f_o}{f_o} \Big/ \frac{\delta V_P}{V_{Pnom}}$	<	5	%	

Control loop 1 (between sync pulse and oscillator)

Control voltage range	V_{12-16}		0,8 to 5,5	V	
Control current (peak values)					
at $V_{10-16} > 4,5$ V; $V_{6-16} > 1,5$ V	I_{12M}	typ.	±2	mA	
at $V_{10-16} < 2$ V; $V_{6-16} > 1,5$ V	I_{12M}	typ.	±6	mA	
Loopgain of APC system					
a. Time coincidence between sync pulse and flyback pulse or $V_{10-16} > 4,5$ V	$\frac{\Delta f}{\Delta t}$	typ.	1	kHz/μs	
b. No time coincidence or $V_{10-16} < 2$ V	$\frac{\Delta f}{\Delta t}$	typ.	3	kHz/μs	
Catching and holding range	Δf	typ.	±1	kHz	3)

1) The oscillator frequency can be changed for other t.v. standards by an appropriate value of C_{14-16}.

2) Exclusive external components tolerances.

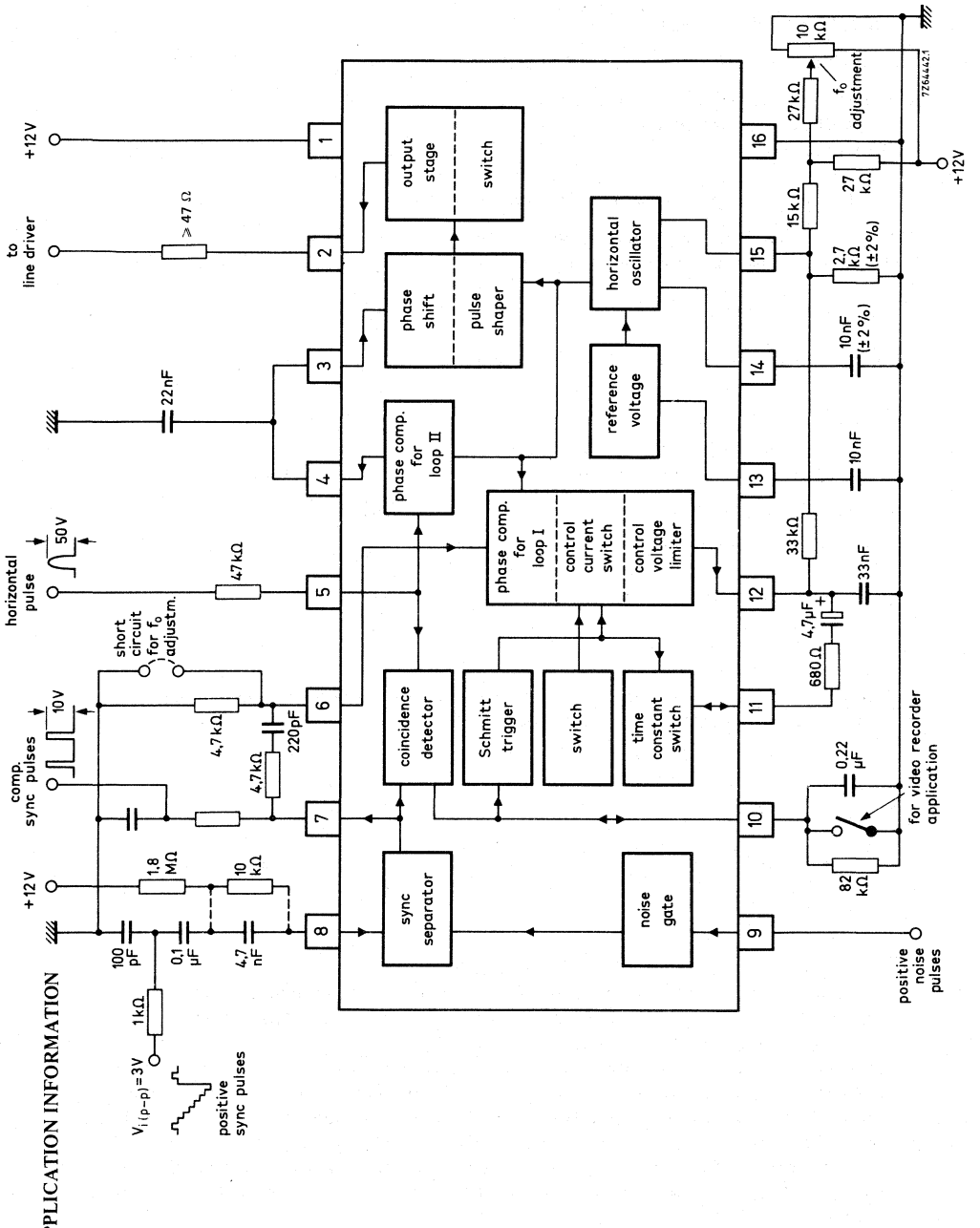
3) Adjustable with R_{12-15}.

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_o = \pm 3\%$ (Δf = 470 Hz)	t	≈	20	ms	1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	≈	20	ms	1)
Control loop II (between flyback pulse and oscillator)					
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	$t_{d\ tot}$		0 to 15	µs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	<	0,5	%	2)
Output current during flyback pulse (peak value)	I_{4M}	typ.	±0,7	mA	
Overall phase relation					
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	µs	3)
Tolerance of phase relation	$\lvert\Delta t\rvert$	<	1	µs	4)
Voltage for T_2 = 12 to 32 µs	V_{3-16}		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T_2}{\Delta V_{3-16}}$	typ.	10	µs/V	
Input current	I_3	<	2	µA	
External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.					
Required switch-over voltage					
at R_{11-16} = 150 Ω	V_{10-16}	>	4,5	V	
at R_{11-16} = 2 kΩ	V_{10-16}	<	2	V	
Required switch-over current					
at R_{11-16} = 150 Ω; V_{10-16} = 4,5 V	I_{10}	typ.	80	µA	5)
at R_{11-16} = 2 kΩ; V_{10-16} = 2 V	I_{10}	typ.	120	µA	

1) See application information circuit on page 6.
2) The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3) This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at C_{5-16} = 560 pF.
4) The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5) With sync pulses at pin 7 and 8; without RC network at pin 10.

APPLICATION INFORMATION

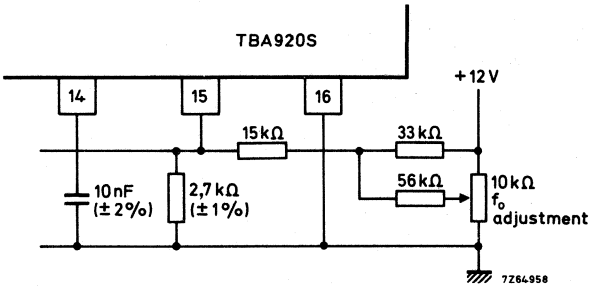


HORIZONTAL COMBINATION

The TBA920S is identical to the TBA920, except for the following data:

Oscillator

Spread of frequency at $R_{15-16} = 3,3\ k\Omega$; $C_{14-16} = 10\ nF$	$\frac{\Delta f_o}{f_o}$	<	1,5	%
Adjustment range of frequency (in network below)	$\frac{\Delta f_o}{f_o}$	typ.	±5	%

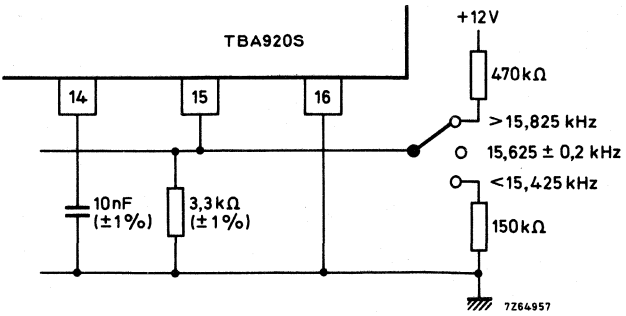


Note: The above network is the only part that differs from the circuit given on page 6 of TBA920 data.

Overall phase relation

Tolerance of phase relation between leading edge of sync pulse and middle of flyback pulse	$\lvert\Delta t\rvert$	<	0,4	µs

Other circuit possibilities for oscillator frequency adjustment



TELEVISION SIGNAL PROCESSING CIRCUIT

The TCA270S is a monolithic integrated circuit combining the following functions:
- synchronous demodulator
- video amplifier with buffer output stages
- noise inverters
- A.G.C. detector with output stages for n-p-n tuner and i.f. amplifier
- A.F.C. demodulator with buffer output stage

Opposite polarity video signals are available from emitter followers, the negative-going signal being matched to integrated circuit type TBA920.

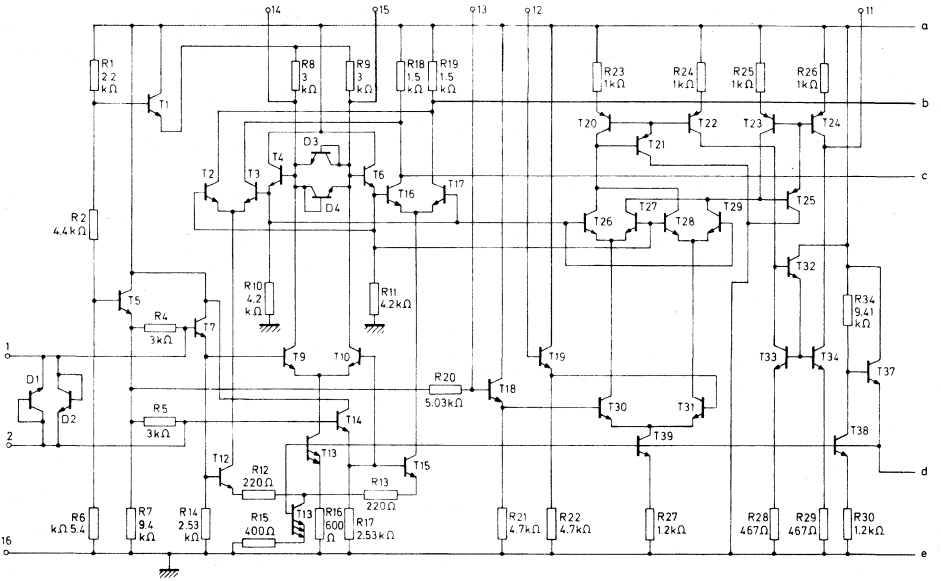
QUICK REFERENCE DATA

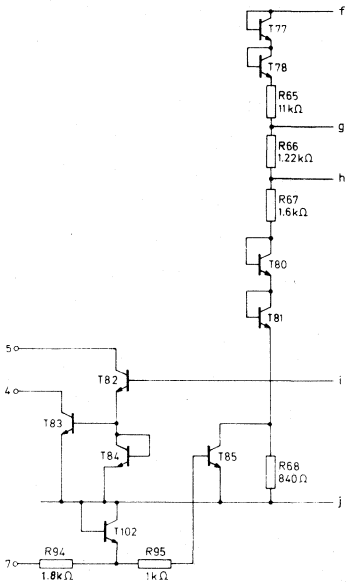
Supply voltage	V_{3-16}	nom.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Frequency	f	typ.	38,9	MHz
Supply current	I_3	typ.	47	mA
Video output voltage (peak value)	V_{9-16M}	typ.	3	V
Bandwidth (3 dB)	B	typ.	5	MHz
Intermodulation products (blue colour bar)				
1,1 MHz with respect to B-W level		typ.	−60	dB
3,3 MHz with respect to B-W level		typ.	−67	dB
A.F.C. output control voltage swing (peak-to-peak value)	$V_{11-16(p-p)}$	>	10	V
A.G.C. control current for n-p-n i.f. (pin 4)	I_4	>	10	mA
A.G.C. control current for tuner (pin 5)	I_5	>	10	mA

PACKAGE OUTLINES

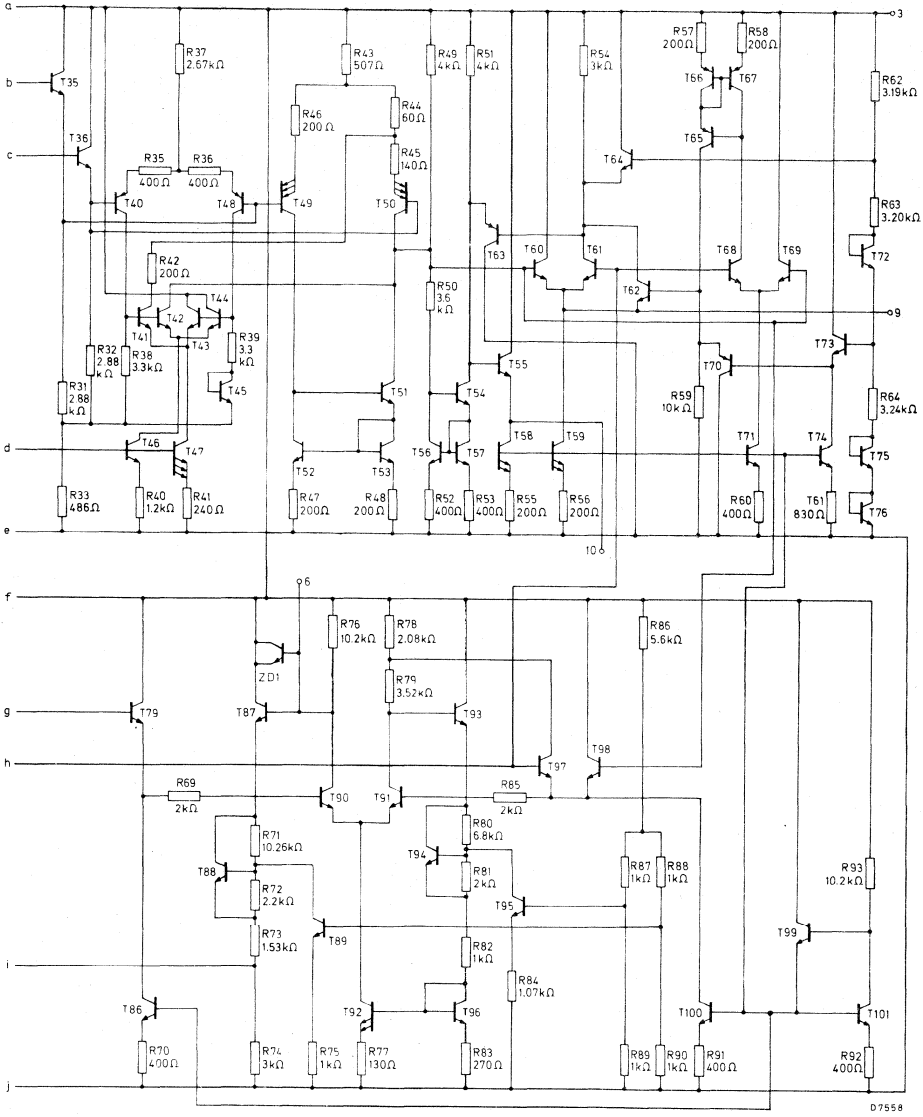
TCA270S : 16-lead DIL; plastic (SOT-38).
TCA270SQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM





CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage during switch on ($t \leq 10$ s)	V_{3-16}	max.	18	V
Power dissipation	P_{tot}	max.	1	W
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +55	°C

CHARACTERISTICS

Supply voltage range	V_{3-16}	typ.	12,0	V
			10,2 to 13,8	V
Supply current range	I_3	typ.	47	mA
			33 to 62	mA
D.C. output voltage (zero signal; pin 9)	V_{9-16}	typ.	6	V
D.C. output voltage (zero signal; pin 10)	V_{10-16}	typ.	6	V
D.C. output voltage at start of a.g.c. (pin 9)	V_{9-16}	typ.	3	V
Unbalanced r.m.s. input voltage for a.g.c.	$V_{i(rms)}$	typ.	70	mV
			50 to 100	mV
Input resistance at pin 1	R_{1-16}	typ.	3	kΩ
Input resistance at pin 2	R_{2-16}	typ.	3	kΩ
Bandwidth (3 dB) of video output	B	typ.	5	MHz
Differential gain		<	10	% [1]
Differential phase		<	10	° [1]
Intermodulation products (blue colour bar)				
1,1 MHz		typ.	−60	dB
3,3 MHz		typ.	−67	dB
Carrier frequency rejection at pins 9, 10 and 11		>	40	dB
Twice carrier frequency rejection at pins 9, 10 and 11		>	40	dB

1) CCIR system of modulation, peak of white signal = 10% of carrier.

CHARACTERISTICS (continued)

A.G.C. circuit

Saturation voltage of tuner control at 10 mA (pin 4)	$V_{4\text{-}13sat}$	<	0,3	V
Saturation voltage of i.f. control at 10 mA (pin 5)	$V_{5\text{-}13sat}$	0,7 to	1,2	V
Breakdown voltage at 1 mA (pins 4 and 5)	$V_{(BR)4\text{-}13}$ $V_{(BR)5\text{-}13}$	>	14	V
Control current at pins 4 and 5	I_4; I_5	>	10	mA
Signal expansion for complete a.g.c.		<	0,5	dB
A.G.C. gating (optional) by negative line flyback pulse; input voltage (peak-to-peak value)	$V_{i(p\text{-}p)}$	>	2	V
		<	supply voltage	
input resistance	R_i	typ.	1,8	kΩ
Current ratio of unsaturated outputs (pins 4 and 5) at I_5 = 1 mA	$\frac{I_4}{I_5}$	>	6	

A.F.C. circuit

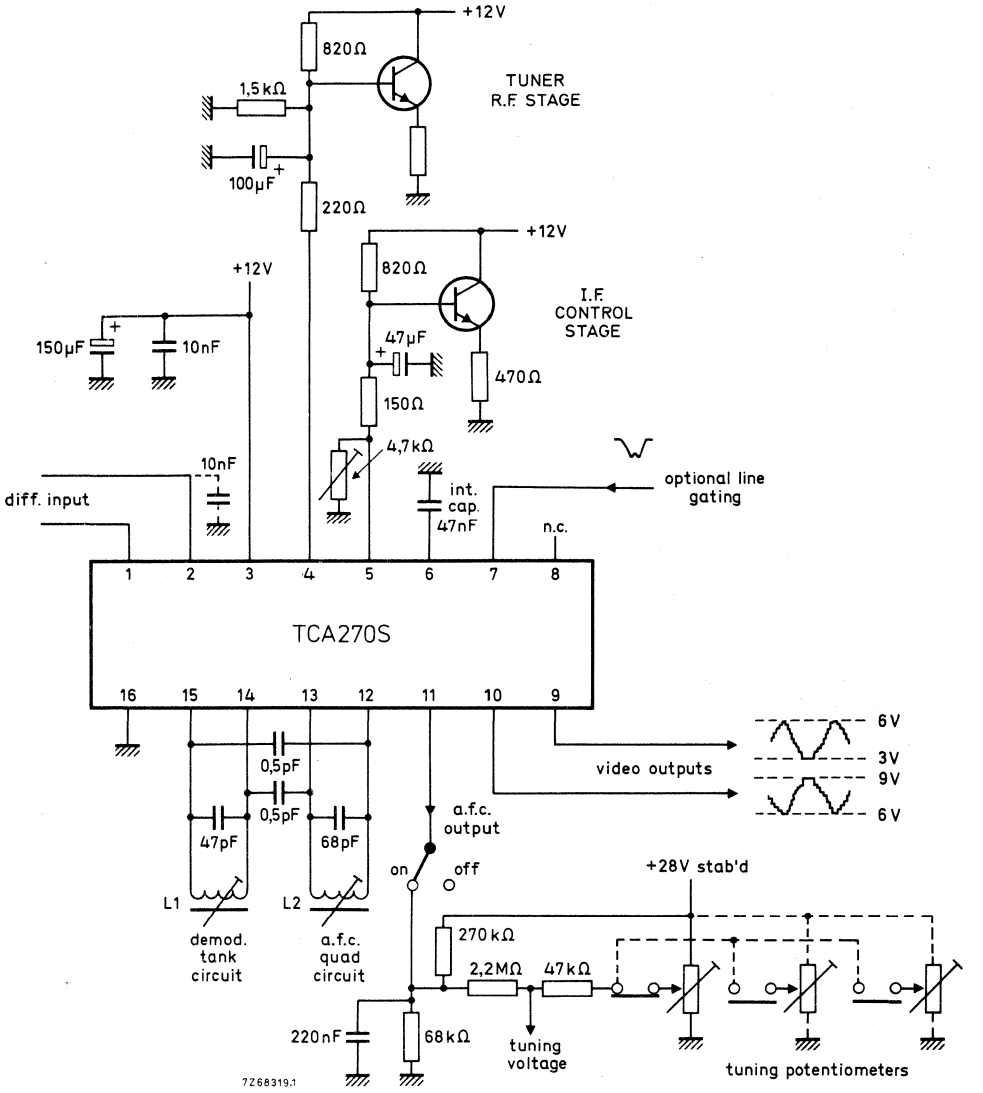
Output control voltage swing (peak-to-peak value)	$V_{11\text{-}16(p\text{-}p)}$	>	10	V
Change of frequency for complete output voltage swing		<	400	kHz
Change of frequency to maintain peak output voltage		>	±1	MHz

Noise inverters [1])

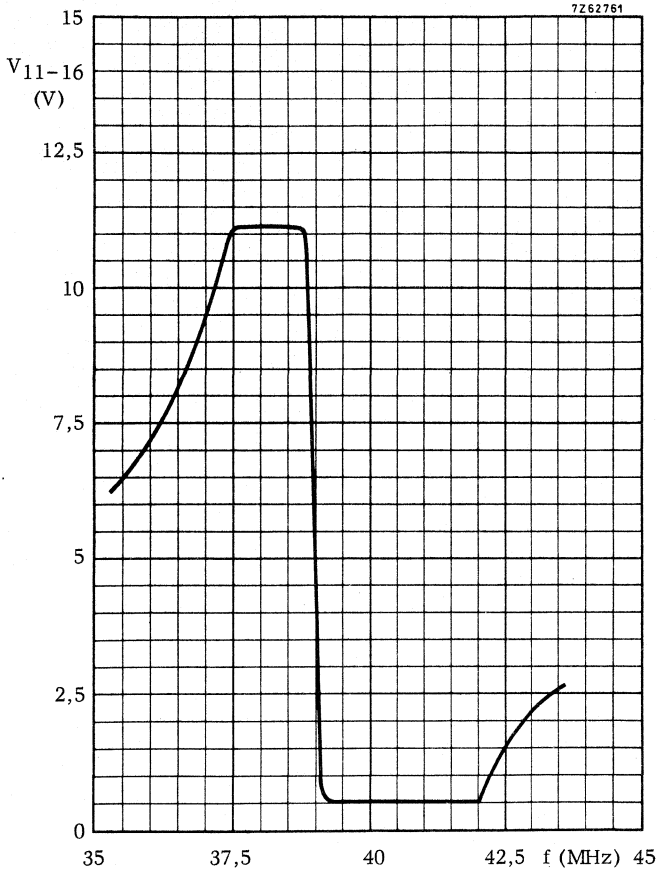
Negative-going noise pulses in pin 9 inversion threshold		typ.	2,55	V
Positive-going noise pulses in pin 9 inversion threshold		typ.	6,6	V

1) Noise pulses are inverted to a point near black level.

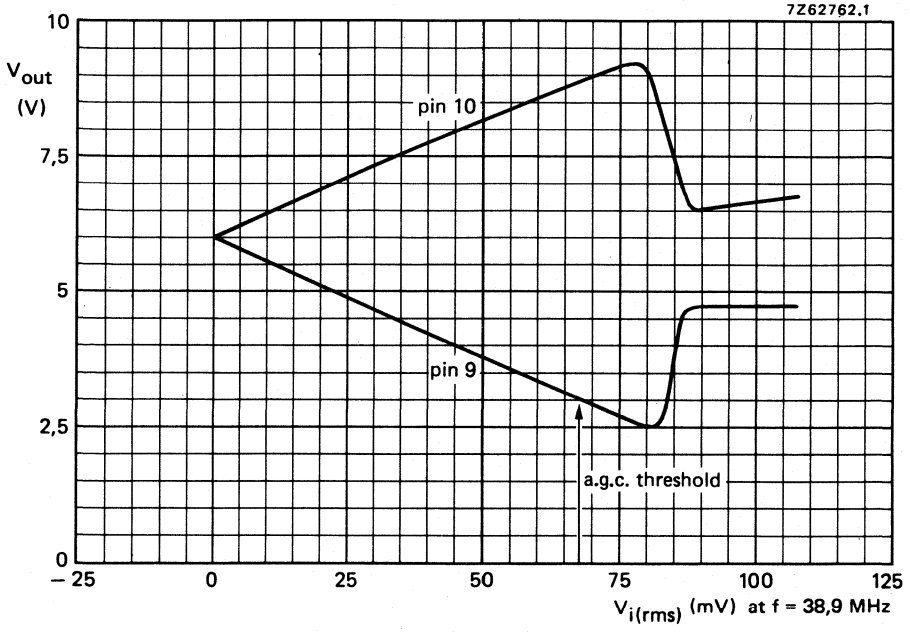
APPLICATION INFORMATION



Unloaded Q of L1 and L2 must be > 50.



A.F.C. output voltage versus frequency


7Z62762.1
10
V_{out}
(V)
7,5
5
2,5
0
pin 10
pin 9
a.g.c. threshold
– 25
0
25
50
75
100
125
$V_{i(rms)}$ (mV) at f = 38,9 MHz

HI-FI F.M./I.F. AMPLIFIER

The TCA420A is a monolithic integrated f.m./i.f. amplifier for car and hi-fi equipment provided with the following functions:

- limiter amplifier
- symmetrical quadrature detector
- symmetrical a.f.c. output
- field-strength indication output
- stereo decoder switching voltage
- adjustable side response suppression
- muting

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	15 V
Supply current (pin 11)	I_P	typ.	26 mA
Input limiting voltage (−3 dB); f_o = 10,7 MHz	$V_{i\,lim}$	typ.	20 μV
A.F. output voltage (pin 5); Δf = ±15 kHz; r.m.s. value	$V_{o(rms)}$	typ.	115 mV
Signal plus noise-to-noise ratio; $V_i > 1$ mV; Δf = ±15 kHz	S+N/N	typ.	72 dB
I.F. input voltage; Δf = ±15 kHz			
S + N/N = 26 dB	V_i	typ.	15 μV
S + N/N = 46 dB	V_i	typ.	45 μV
A.M. rejection; V_i = 10 mV; f_m = 1 kHz (f.m.); Δf = ±15 kHz	α	typ.	50 dB
Total distortion (single tuned circuit); Δf = ±15 kHz	d_{tot}	typ.	0,1 %
Centre shift of f.m. detector curve	$\Delta f = \lvert f_{o1} - f_{o2} \rvert$	typ.	7 kHz
Field-strength indication range	ΔV_i	typ.	70 dB
Supply voltage range (pin 11)	V_P		6 to 18 V
Ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

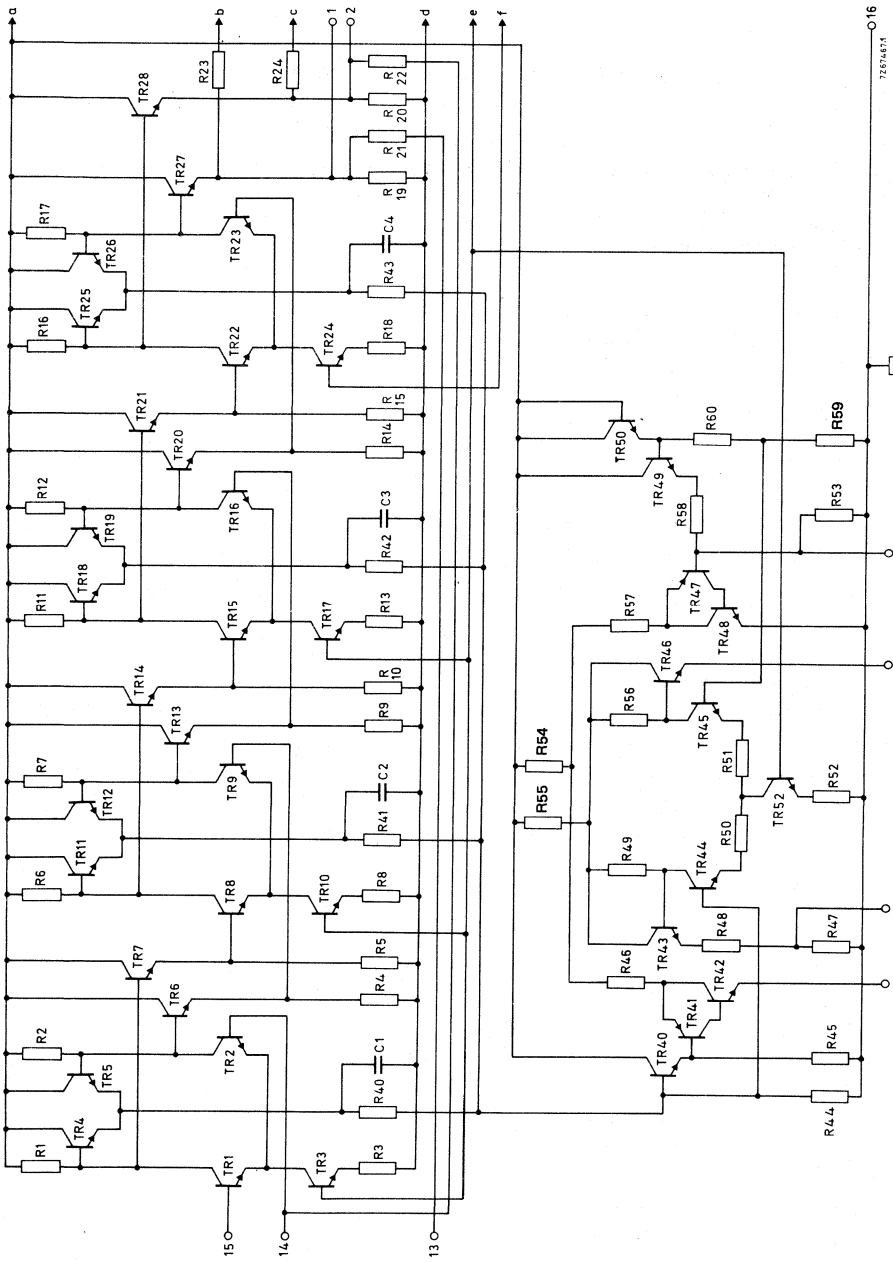


Fig. 1a Part of circuit diagram; other part continued in Fig. 1b.

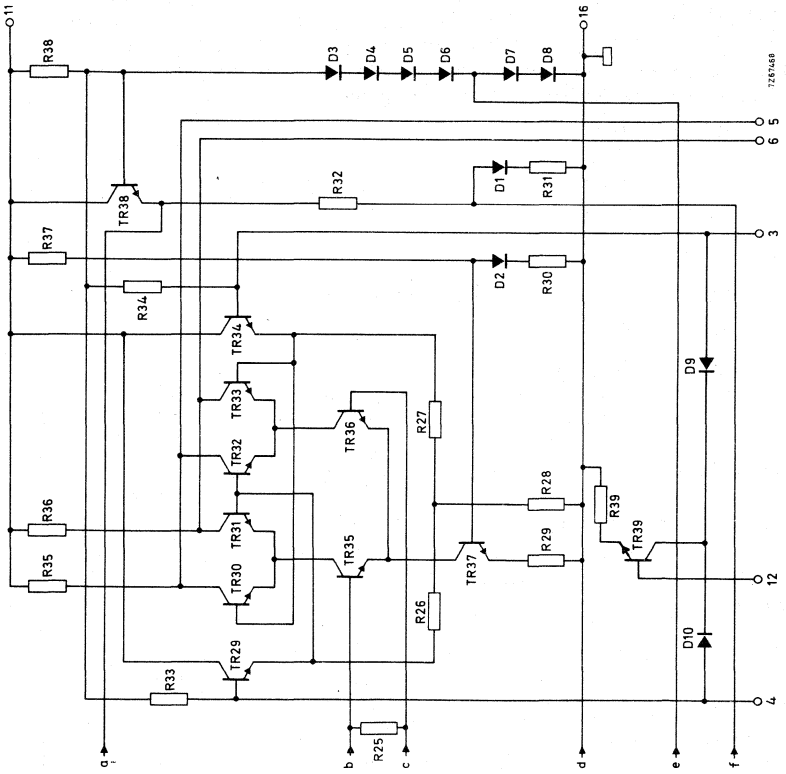


Fig. 1b Part of circuit diagram; continued from Fig. 1a.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-16}$	max.	18 V
Total power dissipation	P_{tot}	max.	720 mW
Storage temperature	T_{stg}		−55 to +150 °C
Operating ambient temperature	T_{amb}		−30 to +80 °C

CHARACTERISTICS

V_P = 8 or 15 V; T_{amb} = 25 °C; f_o = 10,7 MHz; Δf = ±15 kHz; f_m = 1 kHz; R_G = 30 Ω; with de-emphasis (C_{5-6} = 10 nF); adjustment conforms to adjustment procedure unless otherwise specified; the characteristics are valid for a TCA420A mounted on a printed-circuit board (see Figs 2, 3 and 4).

			V_P = 8 V	V_P = 15 V
Supply voltage range (pin 11)		V_P		6 to 18 V
Supply current; R_{7-16} = 5 kΩ; pin 11	I_P	typ.	21	26 mA
		<	–	35 mA
I.F. amplifier/detector				
Input voltages (d.c. value)	V_{13-16}; V_{14-16}; V_{15-16}	typ.	2,6	2,8 V
Input limiting voltage (−3 dB)	$V_{i\,lim}$	typ.	20	20 μV
		<	–	50 μV
I.F. output voltage (peak-to-peak)				
V_i = 5 mV; f = 1 MHz; without detector circuit;	$V_{1-16(p-p)}$	>	300	320 mV
$Z_{1-16} = Z_{2-16}$ = 10 MΩ in parallel with 8 pF	$V_{2-16(p-p)}$	typ.	350	375 mV
Output voltages (d.c. value)	V_{5-16}	>	4,7	8,3 V
	V_{5-16}	typ.	5,0	9,5 V
	V_{6-16}	<	5,3	11,0 V
Output voltage difference (d.c. value)				
V_i = 1 mV; Δf = ±75 kHz	$\pm V_{5-6}$	<	180	350 mV
A.F. output voltage; V_i = 1 mV (pins 5 and 6)				
Δf = ±15 kHz	V_o	>	–	95 mV
		typ.	60	115 mV
Δf = ±40 kHz	V_o	typ.	160	307 mV
Δf = ±75 kHz	V_o	typ.	300	575 mV
Total distortion; V_i = 1 mV; single tuned circuit; Q_L = 20				
with de-emphasis; C_{5-6} = 10 nF				
Δf = ±15 kHz	d_{tot}	<	0,1	0,1 %
Δf = ±40 kHz	d_{tot}	typ.	0,18	0,18 %
Δf = ±75 kHz	d_{tot}	typ.	0,45	0,45 %
without de-emphasis; C_{5-6} = 220 pF				
Δf = ±15 kHz	d_{tot}	<	0,1	0,1 %
Δf = ±40 kHz	d_{tot}	typ.	0,22	0,22 %
Δf = ±75 kHz	d_{tot}	typ.	0,65	0,65 %
		<	1	1 %

		V_P = 8 V	V_P = 15 V
I.F. input voltage; with filter: B = 250 Hz to 16 kHz			
S+N/N = 26 dB; with de-emphasis; C_{5-6} = 10 nF			
Δf = ±15 kHz	V_i	typ. 15	15 μV
Δf = ±75 kHz	V_i	typ. 5	5 μV
S+N/N = 26 dB; without de-emphasis; C_{5-6} = 220 pF			
Δf = ±15 kHz	V_i	typ. 20	20 μV
Δf = ±75 kHz	V_i	typ. 8	8 μV
S+N/N = 46 dB; with de-emphasis; C_{5-6} = 10 nF			
Δf = ±15 kHz	V_i	typ. 45	45 μV
Δf = ±75 kHz	V_i	typ. 20	20 μV
S+N/N = 46 dB; without de-emphasis; C_{5-6} = 220 pF			
Δf = ±15 kHz	V_i	typ. 65	65 μV
Δf = ±75 kHz	V_i	typ. 30	30 μV
Signal plus noise-to-noise ratio; with filter:			
B = 250 Hz to 16 kHz; V_i = 1 mV			
with de-emphasis			
Δf = ±15 kHz	S+N/N	typ. 74	76 dB
Δf = ±75 kHz	S+N/N	typ. 88	90 dB
without de-emphasis			
Δf = ±15 kHz	S+N/N	typ. 68	70 dB
Δf = ±75 kHz	S+N/N	typ. 82	84 dB
Noise output voltage; weighted conform DIN45405			
with de-emphasis			
V_i = 0	V_{no}	typ. 7	12 mV
V_i = 1 mV	V_{no}	typ. 30	50 μV
A.M. rejection; with filter: B = 700 Hz to 5 kHz			
f_m = 70 Hz; Δf = ±15 kHz (for f.m.);			
f_m = 1 kHz; m = 0,3 (for a.m.); simultaneously modulated			
V_i = 0,3 mV	α	typ. 52	52 dB
V_i = 1 mV	α	typ. 40	40 dB
V_i = 10 mV	α	typ. 52	52 dB
V_i = 100 mV	α	typ. 43	43 dB
Zero crossing shift of f.m. detector curve (see note)			
f_m = 70 Hz; Δf = ±75 kHz (for f.m.);		typ. 4	7 kHz
f_m = 1 kHz; m = 85% (for a.m.)	$\Delta f = \lvert f_{o1} - f_{o2} \rvert$	< 9	15 kHz
Detector input impedance	Z_{3-4}	4,4 kΩ//2,25 pF	
Output resistance	R_{5-11};R_{6-11}	typ. 3,3	3,3 kΩ

Note

Zero crossing shift is defined as the difference between frequencies f_{o1} at V_i = 1 mV and f_{o2} at V_i = 30 μV.

CHARACTERISTICS (continued)

			V_P = 8 V	V_P = 15 V
Side response suppression				
Input voltage for 10 dB side response suppression at S1 = 'on' adjust R1, so $V_{10\text{-}16}$ = 1,3 V at V_i = 0; S1 = 'off'; R4 = 3,9 kΩ	$V_{i(rms)}$	typ.	35	30 μV
Side response suppression level Δf = ±15 kHz; $V_{i(rms)}$ = 1 mV				
control voltage for ΔV_o = −1 dB	$V_{12\text{-}16}$	typ.	0,7	0,7 V
control voltage for ΔV_o = −10 dB	$V_{12\text{-}16}$	typ.	1,1	1,1 V
Muting				
Output signal muting at S2 = 'on'; reference signal at S2 = 'off'; $V_{i(rms)}$ = 1 mV; Δf = ±75 kHz; R4 = 3,9 kΩ	ΔV_o	typ.	−80	−80 dB
Field-strength indication				
Output voltages (d.c. value) V_i = 0; $I_{8\text{-}9}$ = 0; $R_{8\text{-}16}$ = 4,3 kΩ	$V_{9\text{-}16}$	typ.	1,75	1,85 V
	$V_{8\text{-}16}$	typ.	1,90	2,00 V
Field-strength indicator current $R_{indicator}$ = 2 kΩ; adjust R2 so $I_{8\text{-}9}$ = 0 at V_i = 0 and R3 = 0 measured at $V_{i(rms)}$ = 120 mV	$I_{8\text{-}9}$	>	130	140 μA
		typ.	190	210 μA
Output resistance	R_o	typ.	810	850 Ω
	$R_{9\text{-}16}$	typ.	3,7	3,7 kΩ
Stereo decoder switching voltage				
Reference voltage; without load: I_7 = 0	$V_{7\text{-}16}$	typ.	2,05	2,25 V
Output voltage; $I_{10} = I_{10max}$	$V_{10\text{-}16}$	typ.	1,70	1,90 V
Available output current	$-I_{10\,max}$	typ.	0,45	0,85 mA
Output voltage as a function of the i.f. input voltage $R_{10\text{-}16}$ = 3,9 kΩ; R1 = 5 kΩ	$\frac{\Delta V_{10\text{-}16}}{20 \log \frac{V_{i1}}{V_{i2}}}$	typ.	−0,9	−1,2 V/20 dB
Input voltage for $V_{10\text{-}16}$ = 0,8 V adjust R1 so $V_{10\text{-}16}$ = 1,3 V at $V_{i(rms)}$ = 0	$V_{i(rms)}$	typ.	98	100 μV
		<	150	200 μV
Input voltage for $V_{10\text{-}16}$ = 1,3 V adjust R1 so $V_{10\text{-}16}$ = 0,8 V at $V_{i(rms)}$ = 3 mV	$V_{i(rms)}$	>	–	0,5 mV
		typ.	1,3	1,3 mV
		<	–	1,75 mV
Input resistance (pin 7)	$R_{7\text{-}16}$	typ.	4	4,7 kΩ

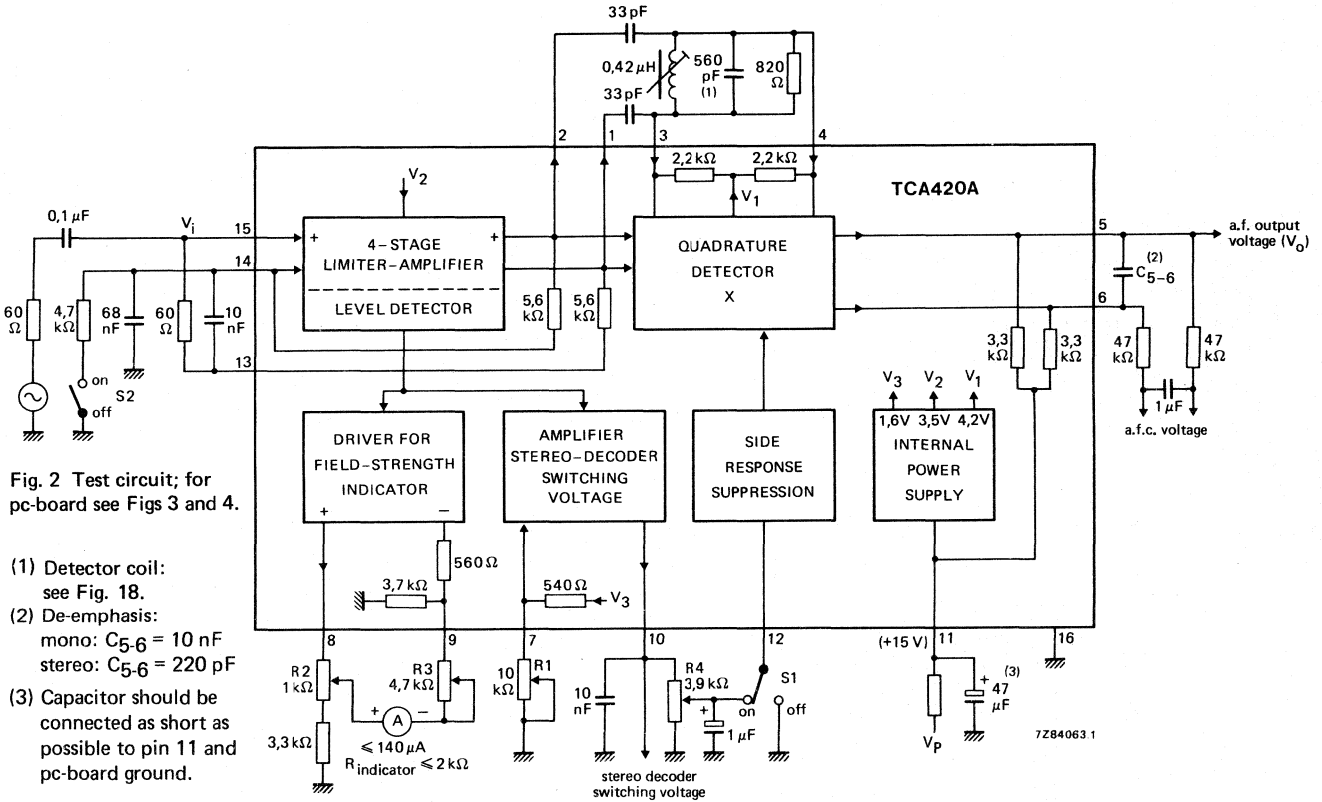
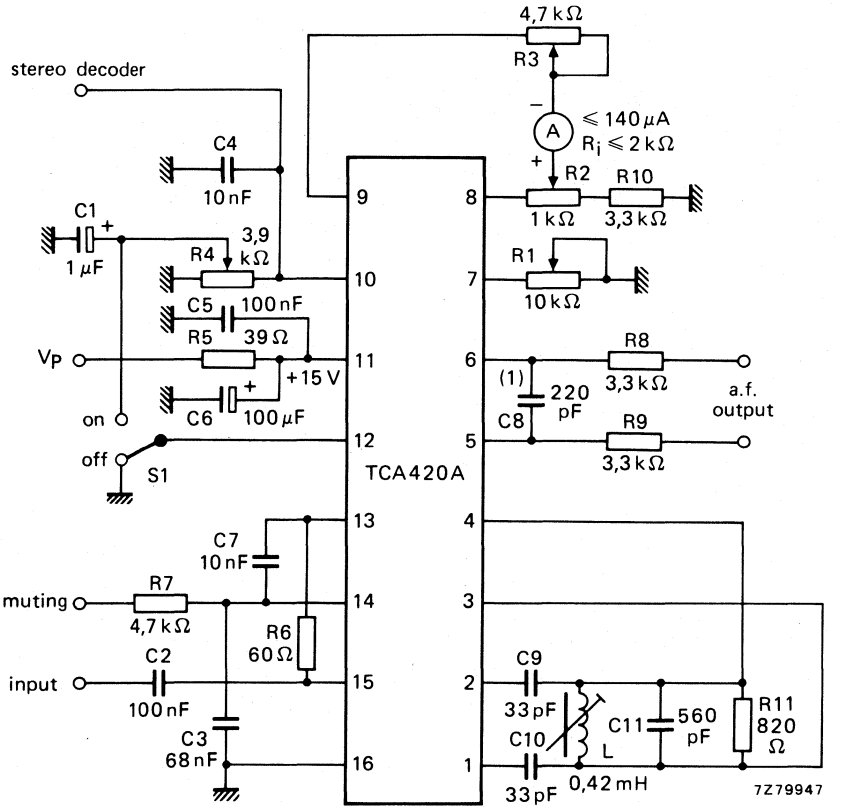


Fig. 2 Test circuit; for pc-board see Figs 3 and 4.

(1) Detector coil: see Fig. 18.
(2) De-emphasis: mono: C_{5-6} = 10 nF stereo: C_{5-6} = 220 pF
(3) Capacitor should be connected as short as possible to pin 11 and pc-board ground.

R1 = preset potentiometer for adjusting output voltage V_{10-16} for mono/stereo switching of stereo decoder.
R2 = preset potentiometer for adjusting the zero level of the field-strength indicator current.
R3 = preset potentiometer for adjusting the maximum level of the field-strength indicator current.
R4 = preset potentiometer for adjusting the side response suppression.
S1 = side response suppression switch.
S2 = output signal muting switch.



(1) $C_8 = C_{5\text{-}6}$ (see Fig. 2).
For mono: C8 = 10 nF.
For stereo: C8 = 220 pF.

Fig. 3 Circuit diagram showing components arrangement for printed-circuit board (Fig. 4). The circuit is similar to the test circuit of Fig. 2.

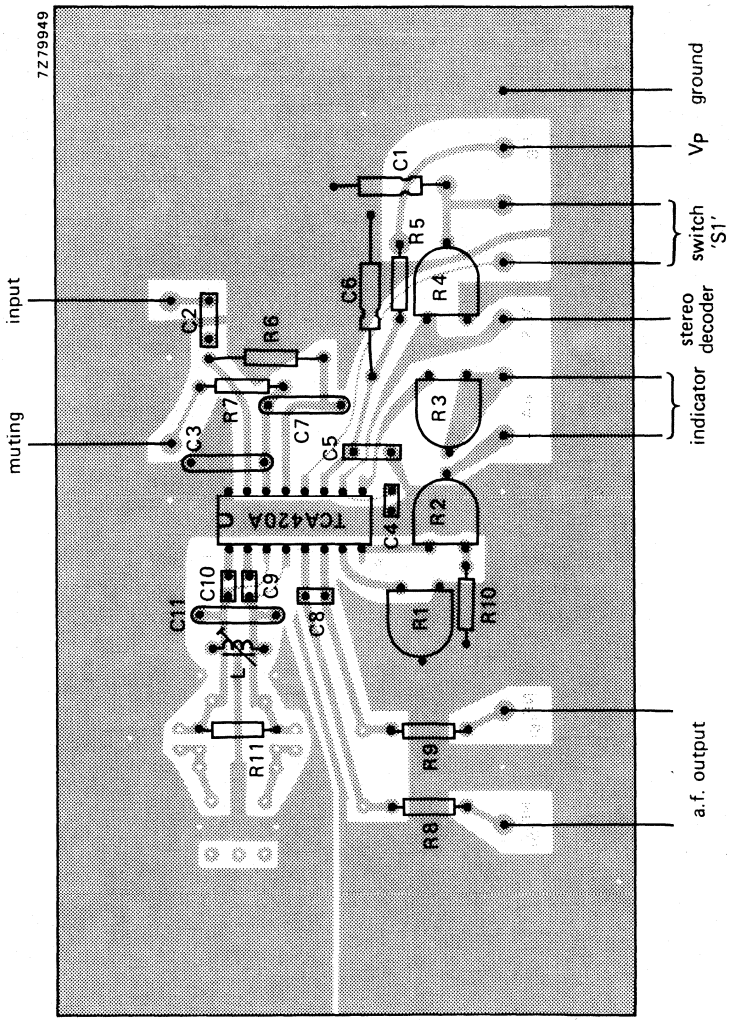


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

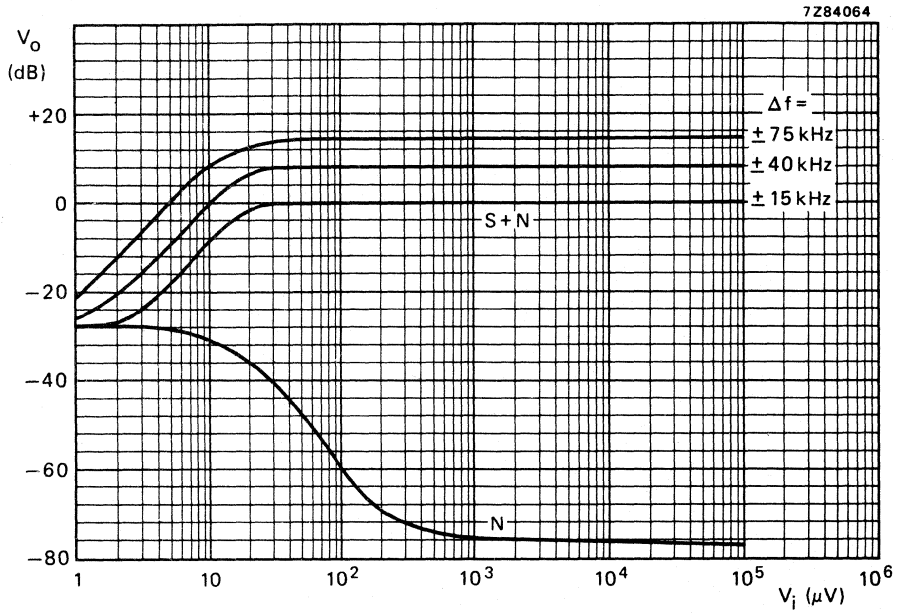


Fig. 5 V_P = 15 V; f_m = 1 kHz; B = 250 Hz to 16 kHz; typical values.

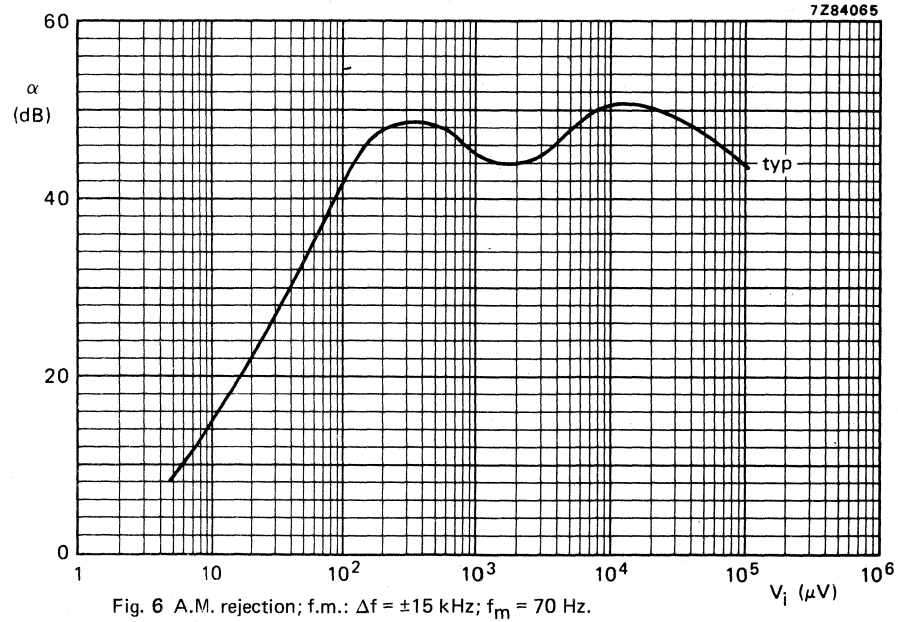


Fig. 6 A.M. rejection; f.m.: Δf = ±15 kHz; f_m = 70 Hz.
a.m.: m = 30%; f_m = 1 kHz; simultaneously modulated.

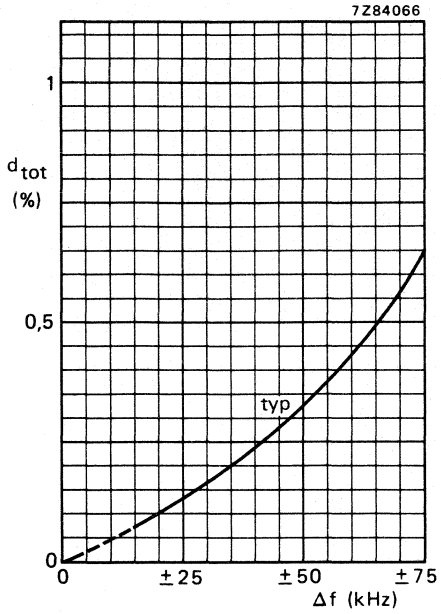


Fig. 7 Total distortion as a function of frequency deviation; single tuned circuit with $Q_L = 20$; $f_m = 1$ kHz; $C_{5\text{-}6} = 220$ pF.

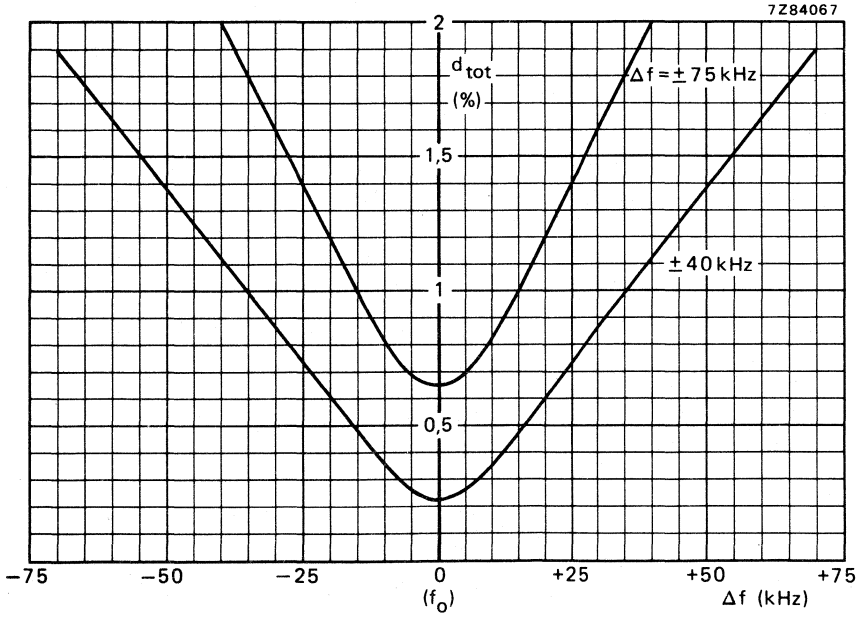


Fig. 8 Total distortion as a function of detuning; single tuned circuit with $Q_L = 20$; $f_m = 1$ kHz; $C_{5\text{-}6} = 220$ pF.

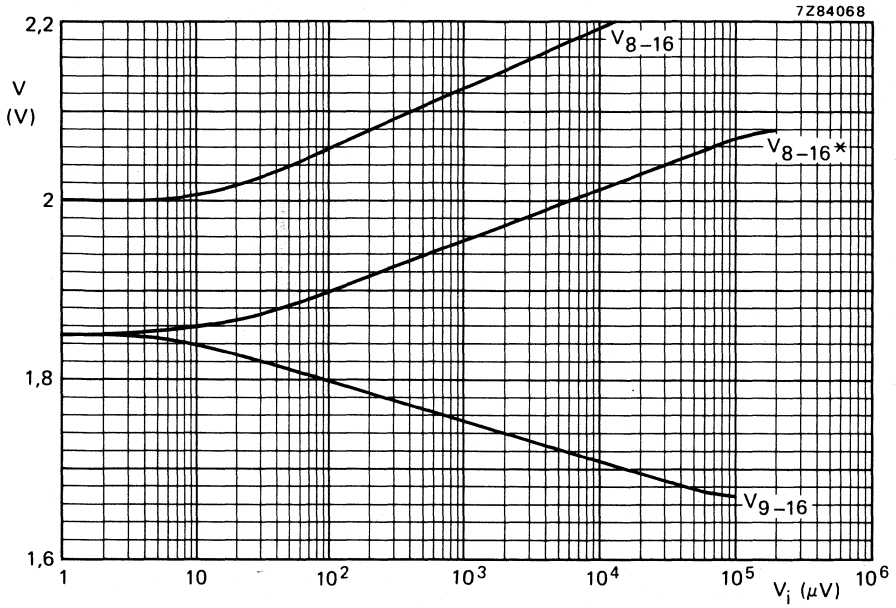


Fig. 9 Field-strength indication output voltages as a function of i.f. input voltage; R2 adjusted so $V_{8-9} = 0$ at $V_i = 0$; $R_{indicator} + R2 = 2\ k\Omega$; for V_{8-16}* definition see Fig. 11.

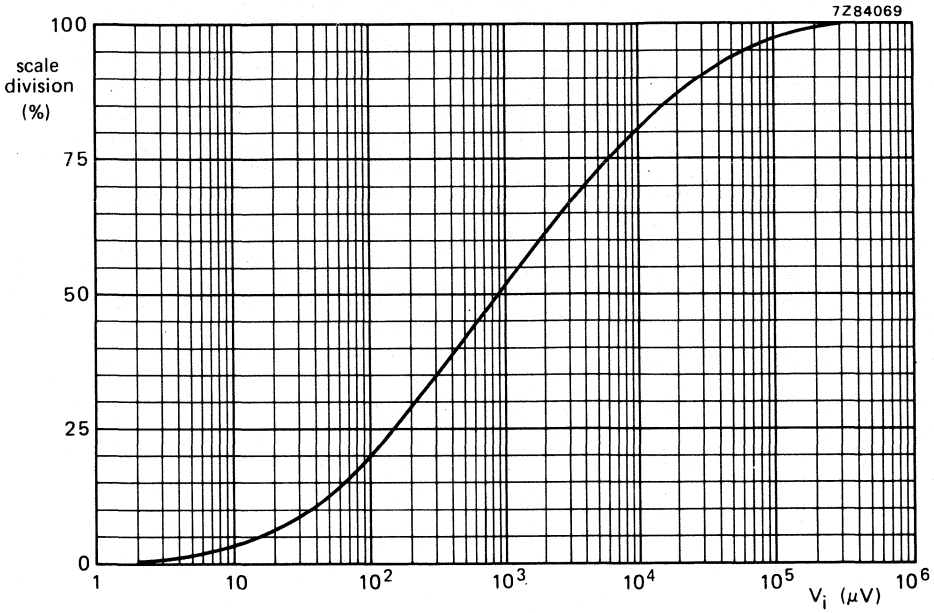


Fig. 9 Scale division of indicator as a function of i.f. input voltage; R2 adjusted so $V_{8-9} = 0$ at $V_i = 0$; $R_{indicator} = 2\ k\Omega$; R3 adjusted at indication 100%; indicator current = 140 μA; see Fig. 11.

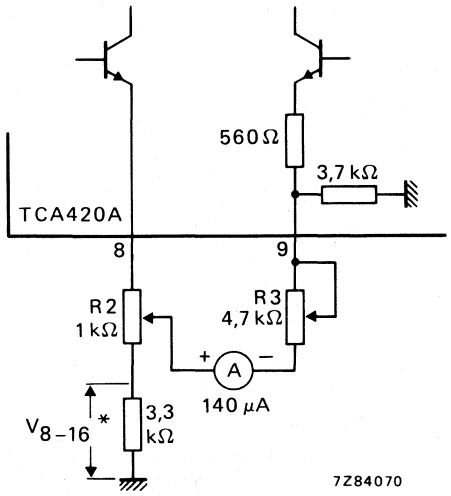


Fig. 11 Circuit diagram showing field-strength indicator adjustment components.

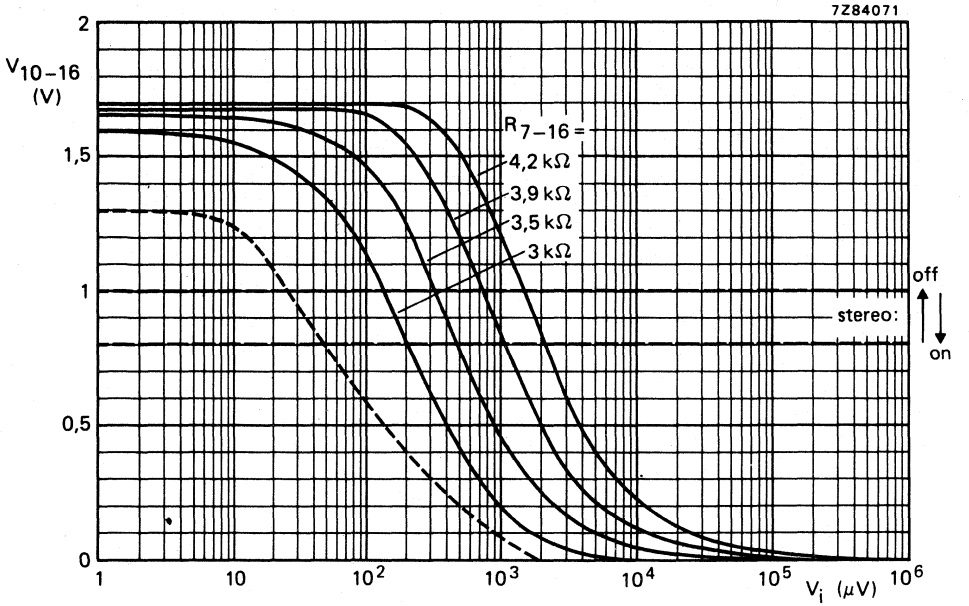


Fig. 12 Stereo decoder switching voltage as a function of i.f. input voltage; R4 = 3,9 kΩ; ----- R1 adjusted so $V_{10-16} = 0$ at $V_i = 0$; see Fig. 13.

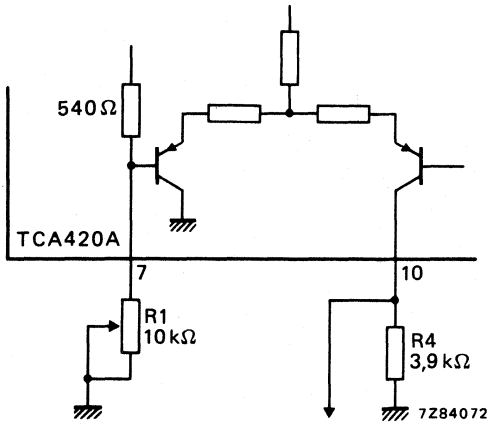


Fig. 13 Circuit diagram showing stereo decoder switching voltage adjustment.

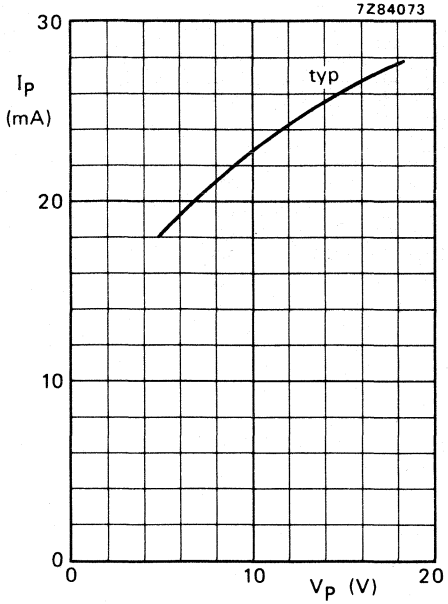


Fig. 14 Supply current consumption.

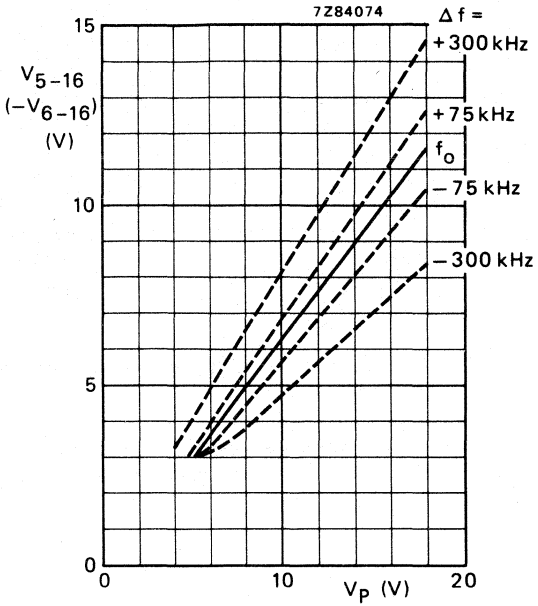


Fig. 15 Output voltage range.

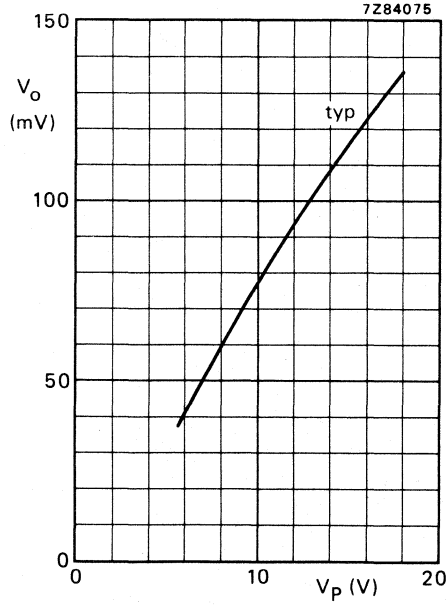


Fig. 16 A.F. output voltage; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz; $V_i = 1$ mV.

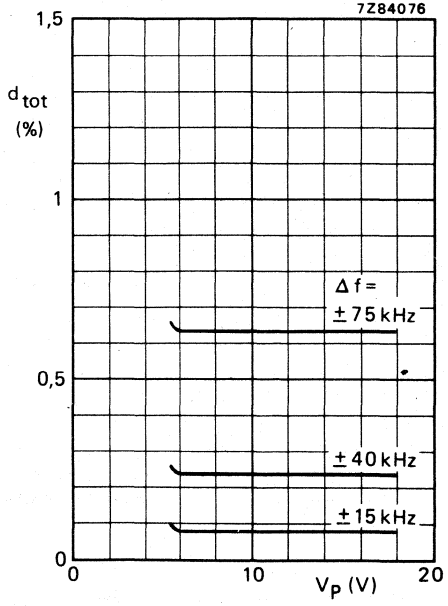


Fig. 17 Total distortion; $f_m = 1$ kHz; $V_i = 1$ mV; $C_{5-6} = 220$ pF.

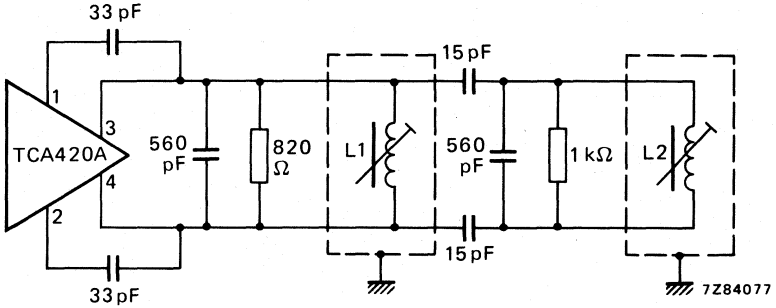


Fig. 18 Example of the TCA420A when using a detector with two tuned circuits; f_o = 10,7 MHz; L1 = L2 ≈ 0,4 μH; Q_o = 70.

Adjustment of the detector:
When having an i.f. input signal on top of the limiter capability, L2 should be detuned, L1 should be adjusted to minimum distortion, and then L2 to minimum distortion.

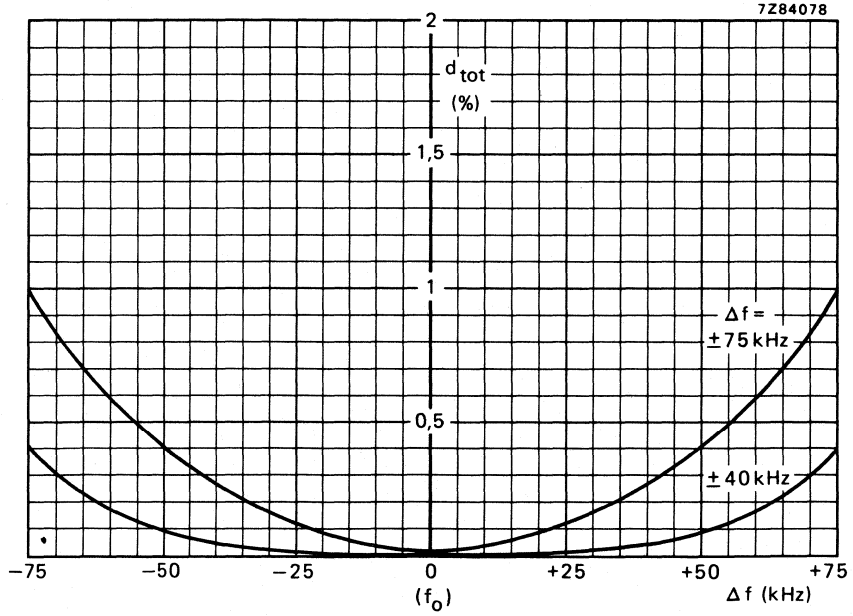


Fig. 19 Total distortion as a function of detuning; circuit as Fig. 18; f_m = 1 kHz; $C_{5\text{-}6}$ = 220 pF. V_o = 500 mV for a frequency deviation Δf = ±75 kHz and $d_{tot} < 0{,}1\%$.

APPLICATION INFORMATION

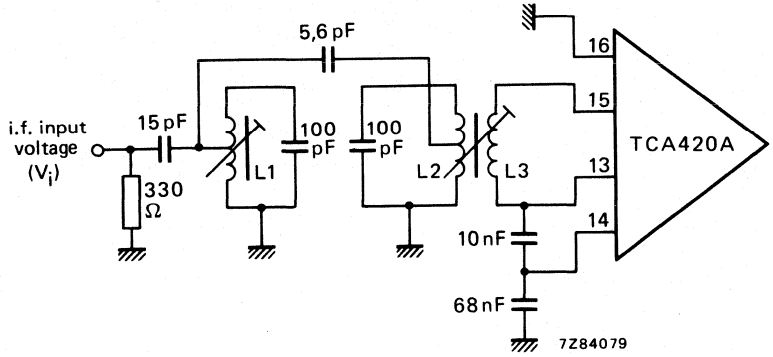


Fig. 20 I.F. coupling circuit, using LC filter; L1 = L2 = 7 + 7 turns h.f. litz wire (5 x 0,04); L3 = 3 turns h.f. litz wire wound on L2 (5 x 0,04).

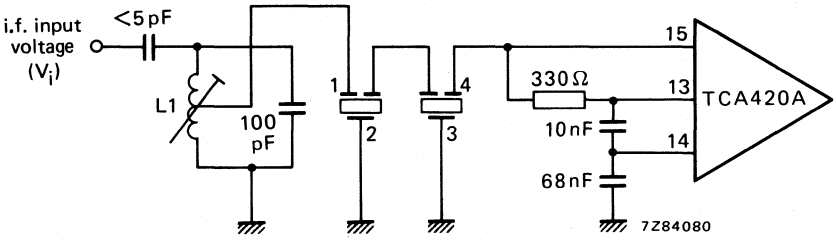
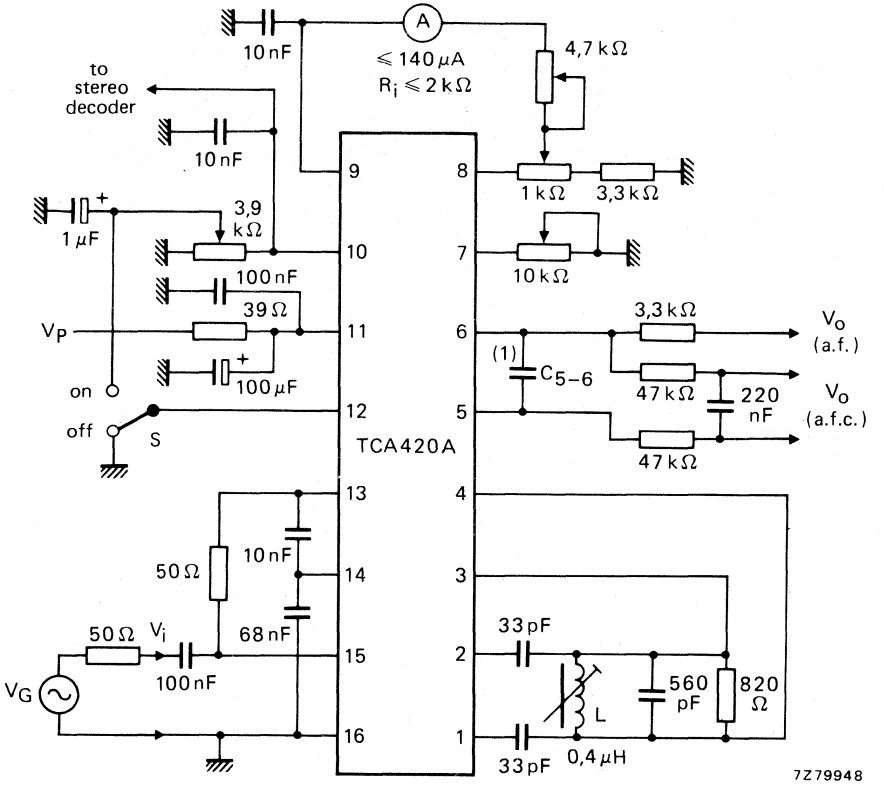


Fig. 21 I.F. coupling circuit, using ceramic filter; L1 = 14 turns h.f. litz wire (5 x 0,04), tab at 3 turns.

APPLICATION INFORMATION (continued)



(1) For mono: C_{5-6} = 10 nF.
For stereo: C_{5-6} = 220 pF.

Fig. 22 Application example of using TCA420A.

INTEGRATED VOLTAGE STABILIZER

The TCA530 is an adjustable 30 V integrated circuit voltage stabilizer for use with variable capacitance diodes.
The circuit features: continuous short-circuit protected output, a.f.c. control voltage input, internal switch-on delay (can be adjusted externally), pre-stabilization and crystal temperature control (temperature sensor and heater).

QUICK REFERENCE DATA

Input (supply) voltage range (for R_i = 3,3 kΩ)	$V_I = V_P$	50 to 68	V
Output voltage	$V_O = V_{6\text{-}16}$	typ. 30	V
Amplitude range of output voltage for a.f.c.	$\Delta V_{6\text{-}16}$	typ. ± 0,75	V
Variation of output voltage as a function of:			
input (supply) voltage variations	$\Delta V_{6\text{-}12}/\Delta V_I$	typ. 0,2	mV/V
output current variations	$\Delta V_{6\text{-}12}/\Delta I_6$	typ. 0,5	mV/mA
temperature variations	$\Delta V_{6\text{-}12}/\Delta T_{amb}$	typ. 0,1	mV/K
heater voltage variations	$\Delta V_{6\text{-}12}/\Delta V_{1\text{-}16}$	typ. 0,2	mV/V
Output current	$I_6 - I_Q$	typ. 3,0	mA
Allowable output voltage range	$V_O = V_{6\text{-}16}$	25 to 30 ± 0,75	V
Allowable output current range	I_6	0 to 4,6	mA

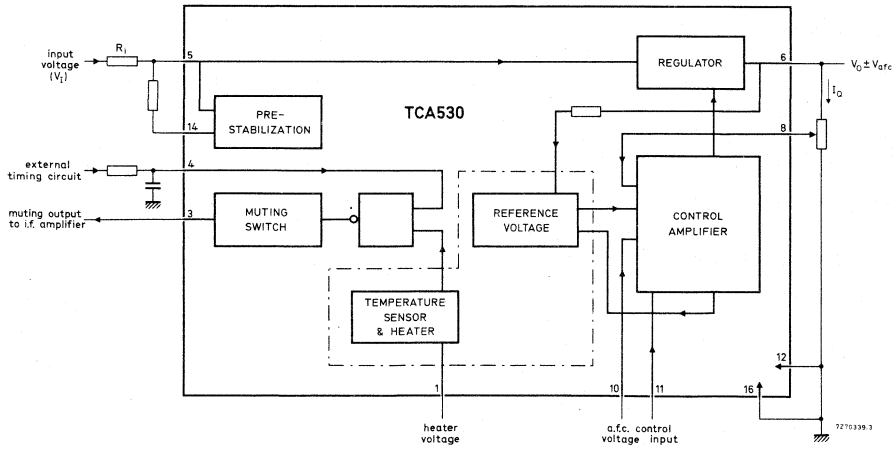


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages: pin 1 (heater voltage)	V_{1-16}		0 to 20 V
pin 3 (muting switch supply)	V_{3-16}	max.	15 V
pins 10 and 11 (a.f.c. input control voltage)	$\pm V_{10-11}$	max.	6 V
Currents: pin 3	$\pm I_3$	max.	5 mA
pin 4	I_4	max.	500 μA
pin 5	I_5	max.	25 mA
pin 6	I_6	max.	30 mA
pin 8	I_8	max.	500 μA
pin 10	I_{10}	max.	500 μA
pin 11	I_{11}	max.	500 μA
pin 14	I_{14}	max.	15 mA
Total power dissipation (excluding heater power) at $T_{amb} = 60\ ^oC$	P_{tot}	max.	500 mW
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−20 to + 80 °C

CHARACTERISTICS

$V_{6-12} = 30$ V; $V_{10-12} = V_{11-12} = 10$ V; $V_{1-16} = 15$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 3.

Voltage control

Input (supply) voltage range* $R_i = 3{,}3\ k\Omega$; $I_6 = 3{,}5$ mA	$V_I = V_P$		50 to 68 V
Current consumption	I_P	typ.	8,1 mA 5,2 to 11,0 mA
	I_5	typ.	$I_6 + (1{,}1 \pm 0{,}3)$ mA
Regulator voltage drop within operating range of the pre-stabilizer	V_{5-6}	typ.	2,7 V 2 to 3,5 V
outside operating range of the pre-stabilizer**	V_{5-6}	<	6 V
Output current (start of current limiting)	I_6	>	8 mA
Internal reference voltage	V_{8-12}	typ.	20 V 18,2 to 21,8 V

* For other input (supply) voltage ranges and output currents, the series resistor R_i has to be altered (see also Fig. 2).

** The specified output voltage dependency of the input (supply) voltage is not guaranteed outside the operating range of the pre-stabilizer.

Input current of control amplifier	I_8	typ. <	0,5 μA 1 μA
Variation of output voltage as a function of *			
input (supply) voltage variations	$\Delta V_{6\text{-}12}/\Delta V_I$	typ.	0,2 mV/V
output current variations	$\Delta V_{6\text{-}12}/\Delta I_6$	typ.	0,5 mV/mA
temperature variations	$\Delta V_{6\text{-}12}/\Delta T_{amb}$	typ.	0,1 mV/K
heater voltage variations	$\Delta V_{6\text{-}12}/\Delta V_{1\text{-}16}$	typ.	0,2 mV/V
Hum suppression at f = 50 Hz			
between input (supply) voltage and pin 6		typ.	80 dB
between pins 5 and 6		typ.	60 dB
between pins 1 and 6		typ.	80 dB
Output noise voltage at f = 10 Hz to 15 kHz (r.m.s. value)	$V_{n(rms)}$	<	50 μV

A.F.C. control amplifier

Common mode input voltage range	$V_{10\text{-}12} = V_{11\text{-}12}$		6,0 to 18,0 V
Common mode rejection ratio	CMRR	typ.	60 dB
Input current	$I_{10} = I_{11}$	typ. <	0,1 μA 0,5 μA
Input resistance	$R_{i(10\text{-}11)}$	>	1 MΩ
Ratio between output voltage variation and a.f.c. input voltage variation	$\Delta V_{6\text{-}12}/\Delta V_{10\text{-}11}$		1,2 : 1
Amplitude range of output voltage	$\Delta V_{6\text{-}12}$	typ. ± 0,5 to ± 1,0	± 0,75 V V

Muting switch

When the crystal temperature has reached approximately its stationary final value, the output of the muting switch (pin 3) becomes high-ohmic. The switching of pin 3 can be delayed by an external RC-circuit at pin 4 or by a switching voltage.

Muting switch ON (pin 3 low-ohmic)			
Input voltage	$V_{4\text{-}16}$	<	8 V
Input current	I_4	typ.	1 μA
Output saturation voltage at I_3 = 1 mA	$V_{3\text{-}16\,sat}$	typ. <	0,45 V 0,6 V
Muting switch OFF (pin 3 high-ohmic)			
Input voltage	$V_{4\text{-}16}$		8 to 11 V
Input current	I_4	>	0,1 μA
Output voltage	$V_{3\text{-}16}$	<	15 V
Output current	I_3	<	1 μA
Internal switch-on delay	t_d	<	3 s

* External component value changes are not taken into account.

CHARACTERISTICS (continued)

Crystal temperature control

Heater voltage range	V_{1-16}	8 to 20	V
Heater peak current at switching on	I_{1M}	typ. 230 < 300	mA mA
Continuous heater current at V_{1-16} = 15 V	I_1	typ. 40 < 55	mA mA
Continuous heater power	P_h	typ. 600	mW

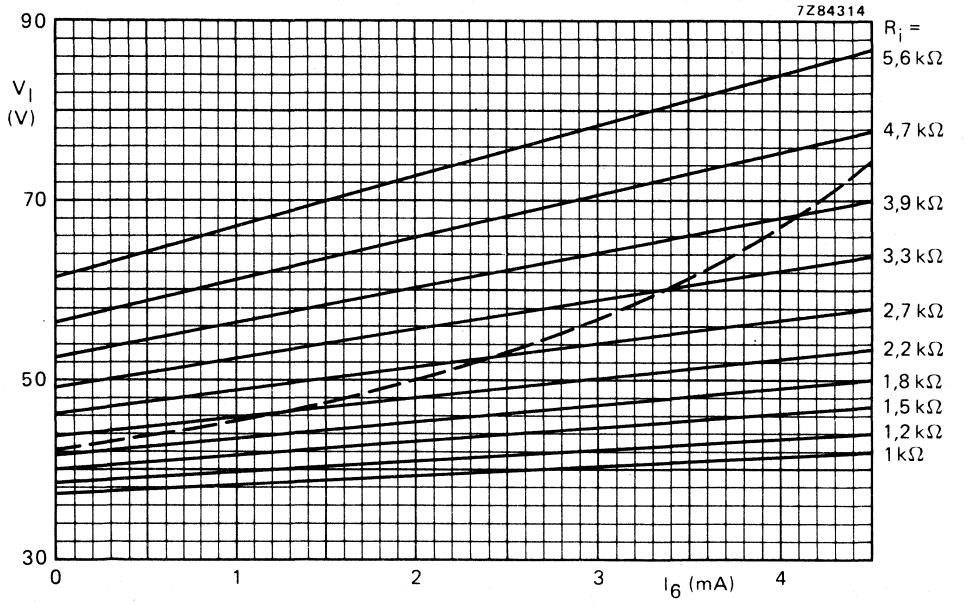
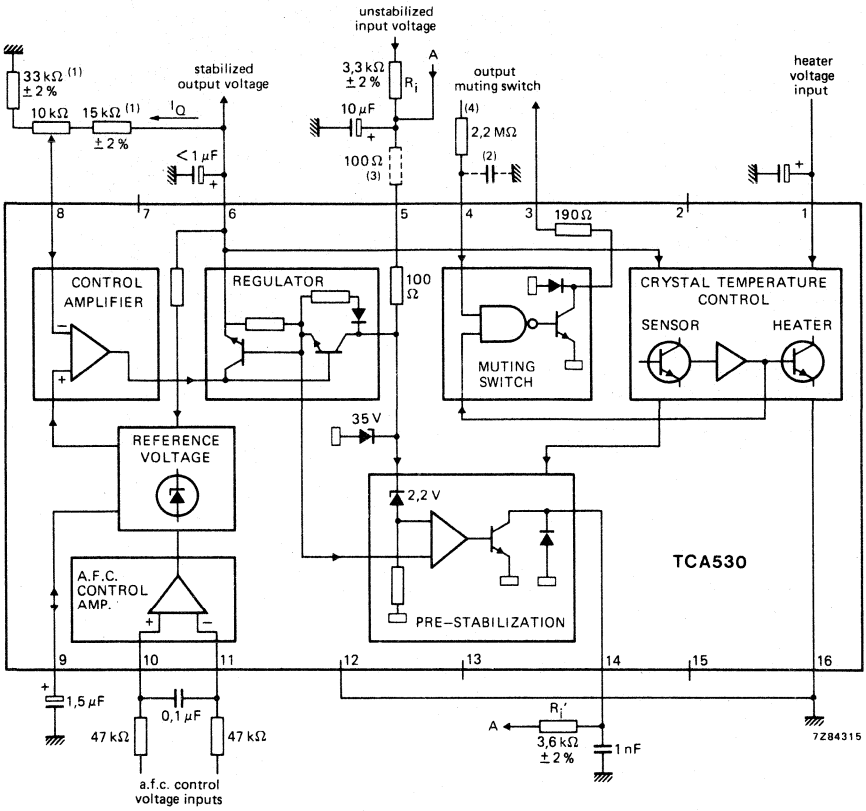


Fig. 2 Curves to obtain R_i-values for various input (supply) voltages and/or output currents. Conditions: V_{6-12} = 30 V; tolerance of I_6 = ± 20%; R_{5-14} = 3,6 kΩ; tolerance of R_i = ± 2%. Above the dotted curve a tolerance of V_I (V_P) of ± 15% is allowed.



(1) It is recommended that fixed resistors of the same kind be used for the voltage divider. The voltage divider of Fig. 4 can be used when a narrow temperature dependency is required.
(2) This capacitor can be applied to increase the internal delay.
(3) This resistor is recommended when the IC is not soldered on a printed-circuit board.
(4) Can be connected to pin 6, for example.

Fig. 3 Test circuit.

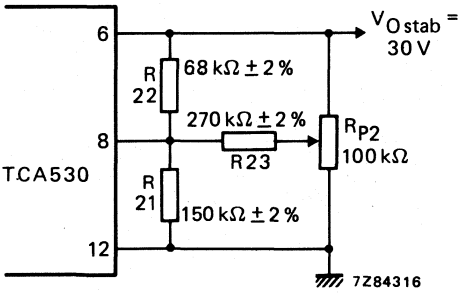


Fig. 4 Voltage divider for the narrowest possible temperature dependency.

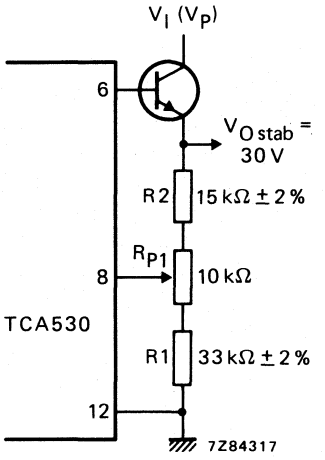


Fig. 5 Circuit extension by means of a series transistor at the output, for output currents > 4,6 mA.

The following table gives some resistor value examples for various output voltages with $\Delta R/R \leqslant \pm 2\%$ and $\Delta R_P/R_P \leqslant \pm 20\%$.

V_{Ostab} V	R_{P2} kΩ	R21 kΩ	R22 kΩ	R23 kΩ	R_{P1} kΩ	R1 kΩ	R2 kΩ
30	100	200	82	300	10	20	10
30	47	180	82	300	47	100	47
29					22	39	18
28	100	220	75	300	22	39	15
28	47	300	100	430			
27					47	68	24
26					22	27	8,2
25	100	560	91	390	47	47	12
25	47	620	100	430			

The series resistors R_i and R_i' (see Fig. 3), as well as the input (supply) voltage V_I (V_P), have to be adapted to the chosen output voltages V_{Ostab}.

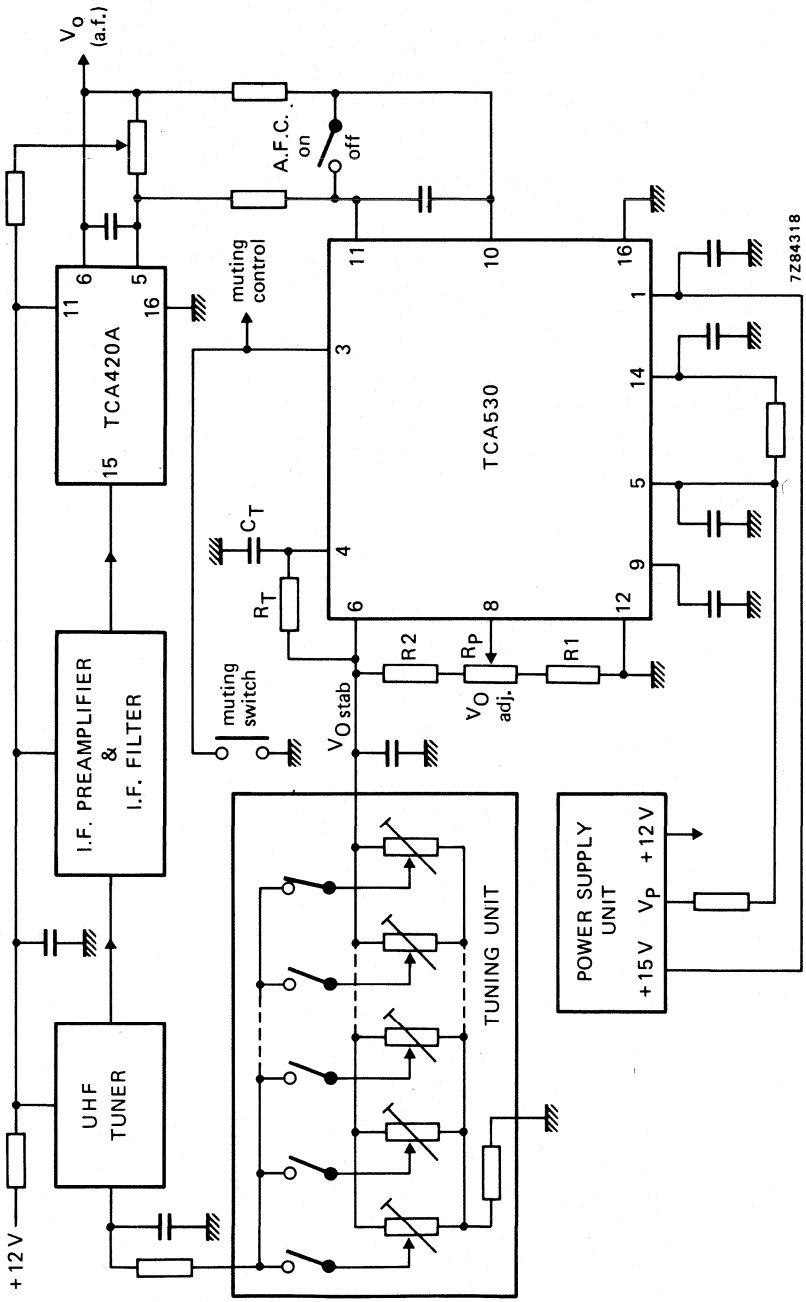


Fig. 6 Application example; f.m. receiver with TCA530 and TCA420A.

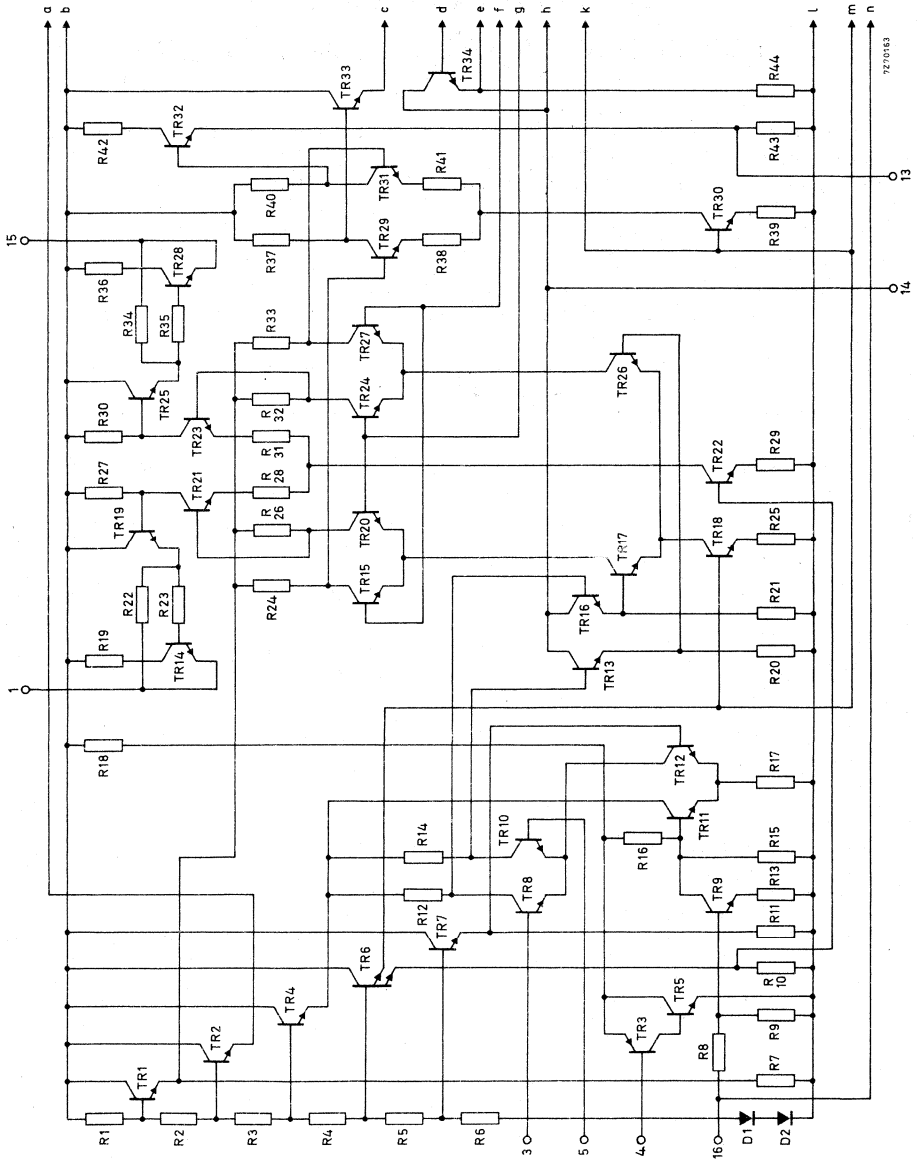
CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the chrominance amplifier the circuit also incorporates a 7,8 kHz flip-flop and an identification circuit for SECAM.
For PAL identification the circuit included in the TBA540 should be used.
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

QUICK REFERENCE DATA						
Supply voltage		V_{14-2}	nom.	12	V	
Supply current		I_{14}	nom.	37	mA	
			PAL		SECAM	
Chrominance input signals (peak-to-peak value)	$V_{3-5(p-p)}$	>	4	7	mV	
		<	80	400	mV	
Chrominance output signals (peak-to-peak value)	$V_{15-2\ (p-p)}$ / $V_{1-2\ (p-p)}$	typ.	500	2000	mV	
Burst output (closed a.c.c. loop) (peak-to-peak value)	$V_{13-2(p-p)}$	typ.	1	–	V	
System switching signal	V_{4-2}	typ.	12	0	V	
Burst blanking of chrominance signal		>	40	–	dB	
Chrominance blanking at field identification		>	–	40	dB	
Square-wave output (7,8 kHz) (peak-to-peak value)	$V_{12-2(p-p)}$	typ.	3	3	V	

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


a
b
c
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TR1
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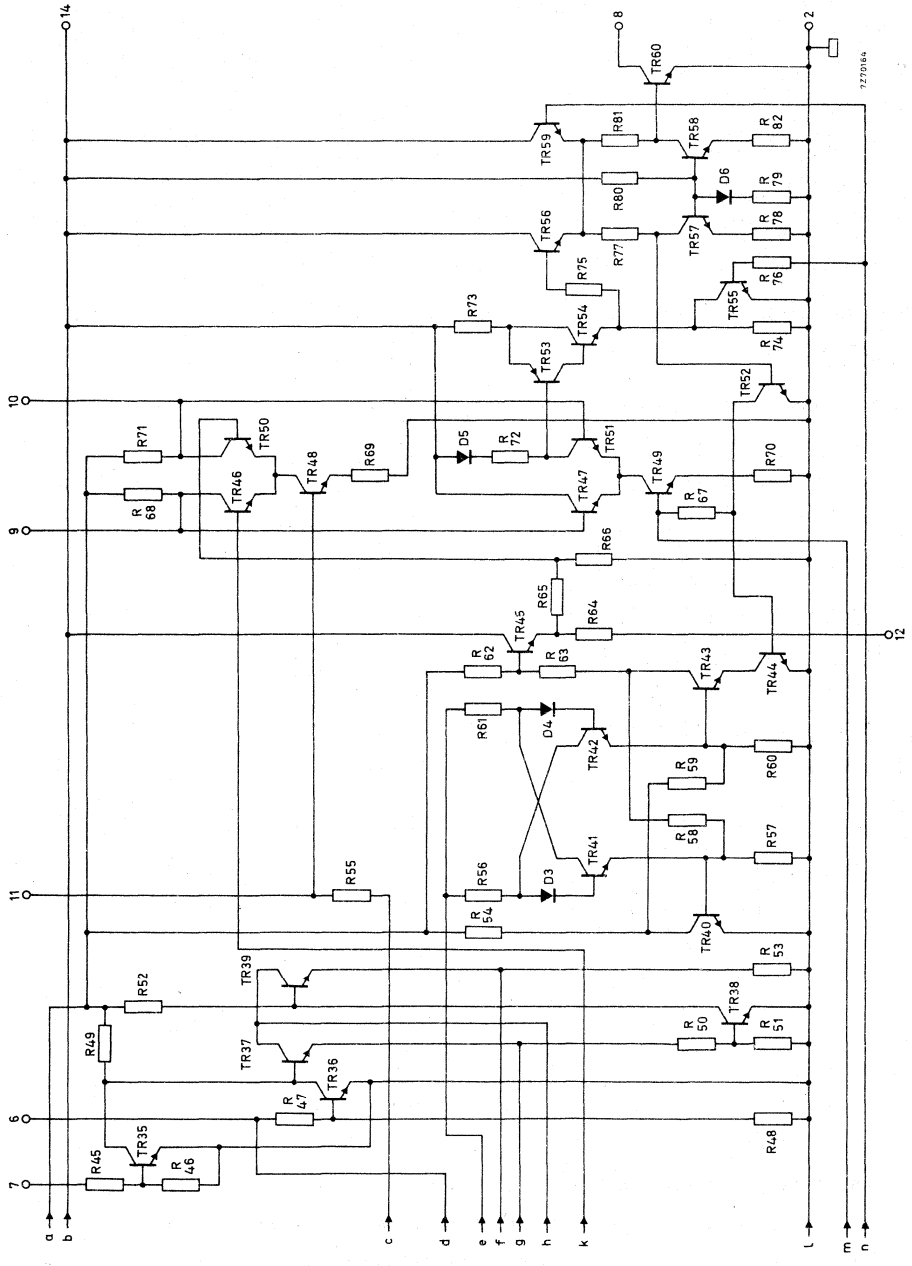
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{14-2}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	625 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C 1)

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}	typ.	12 V
			10,2 to 13,2 V
Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C			
Chrominance input signal			
peak-to-peak value	$V_{3-5(p-p)}$	PAL	4 to 80 mV
		SECAM	7 2) to 400 mV
Automatic chrominance control starting	V_{16-2}	PAL typ.	1,2 V 3)
Flyback pulses for blanking and burst/identification lines-keying			See note 4
Line flyback pulses (positive)			
peak-to-peak value	$V_{6-2(p-p)}$		4,5 to 12 V
Field idenfication pulses (positive)			
peak-to-peak value	$V_{7-2(p-p)}$		4 to 12 V
System switch signal	V_{4-2}	PAL	7 to V_{14-2} V
		SECAM	0 to 1 V
Colour killer threshold	V_{16-2}	PAL typ.	2,5 V 5)

1) When a stabilized power supply of ⩽12 V is applied, T_{amb} is max. 75 °C.

2) Start of limiting.

3) A negative-going potential provides a 26 dB a.c.c. range.

4) The line flyback pulses also provide the clock pulses for the flip-flop.

5) The colour killer is operative above the quoted input voltage.

CHARACTERISTICS (continued)

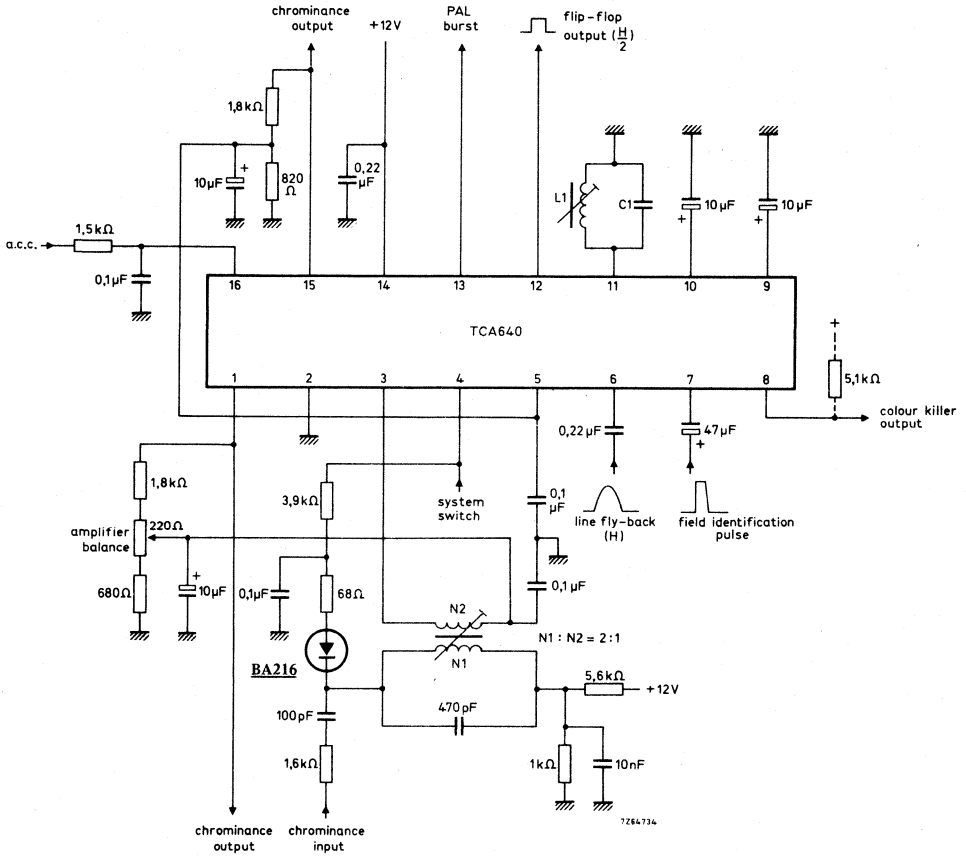
Obtainable output signals

Chrominance output signals						
peak-to-peak value		$V_{15-2(p-p)}$	PAL		425 to 575	mV
		$V_{1-2(p-p)}$	SECAM		1,8 to 2,3	V
Phase difference between output pins		$\Delta\varphi_{15-1}$	PAL		170° to 190°	[1]
Burst signal (peak-to-peak value)		$V_{13-2(p-p)}$	PAL	typ.	1	[2]
Identification signal						
peak-to-peak value		$I_{11(p-p)}$	SECAM		1,4 to 2,4	mA
Output resistance		R_{11-2}			2 to 2,9	kΩ
Flip-flop signal						
peak-to-peak value		$V_{12-2(p-p)}$			2,5 to 3,5	V
Colour killer	killed	V_{8-2}		<	0,5	V
		I_8		<	10	mA
	unkilled	V_{8-2}			V_{14-2}	V
		I_8		<	10	μA
Bandwidth of chrominance amplifier (−1 dB)						
at a carrier frequency of 4,2 MHz				>	±1	MHz
Blanking						
burst rejection			PAL	>	40	dB
rejection identification lines with field identification			SECAM	>	40	dB

1) Over the a.c.c. control range the phase difference varies less than 2,5°.

2) The burst is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Pinning

1. Chrominance output
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Chrominance input
6. Line fly-back pulse input
7. Field identification pulse input
8. Colour killer output
9. } Identification integrating
10. } capacitor (SECAM)
11. Identification tank circuit (SECAM)
12. Flip-flop output
13. Burst output (PAL)
14. Supply voltage (12 V)
15. Chrominance output
16. A.C.C. input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance output (in conjunction with pin 15)

   A balanced output is available at pins 1 and 15.
   At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.
   At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.
   An external d.c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.
   The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)

3. Chrominance input (in conjunction with pin 5)

   The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.
   The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d.c. potential of about 2,5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

   Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a.c.c. voltage at pin 16.
   The chrominance amplifier then provides linear amplification required for the PAL signal.
   Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)

6. Line fly-back pulse input (in conjunction with pin 11)

   Positive going pulses provide

   - blanking of the chrominance signal at the outputs (pins 1 and 15).
   - burst gating for both PAL and SECAM.
     The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit L_1C_1 (see circuit on page 6) is tuned to 4,25 MHz (at C_1 = 470 pF).
   - trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

   Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.
   To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit L_1C_1 (see circuit on page 6) should be tuned to 3,9 MHz and the capacitor C_1 should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

APPLICATION INFORMATION (continued)

8. Colour killer output

   This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a.c.c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)

10. Identification integrating capacitor (SECAM)

11. Identification detector tank circuit (see pins 6 and 7)

12. Flip-flop output

    A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin.
    An external load resistor is not required.

13. Burst output (PAL)

    A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 625 mW at 65 ^{o}C ambient temperature.

15. Chrominance output (see pin 1)

16. A.C.C. input

    With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a.c.c. starting at + 1,2 V
    During SECAM operation, the voltage at the input should not exceed + 0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

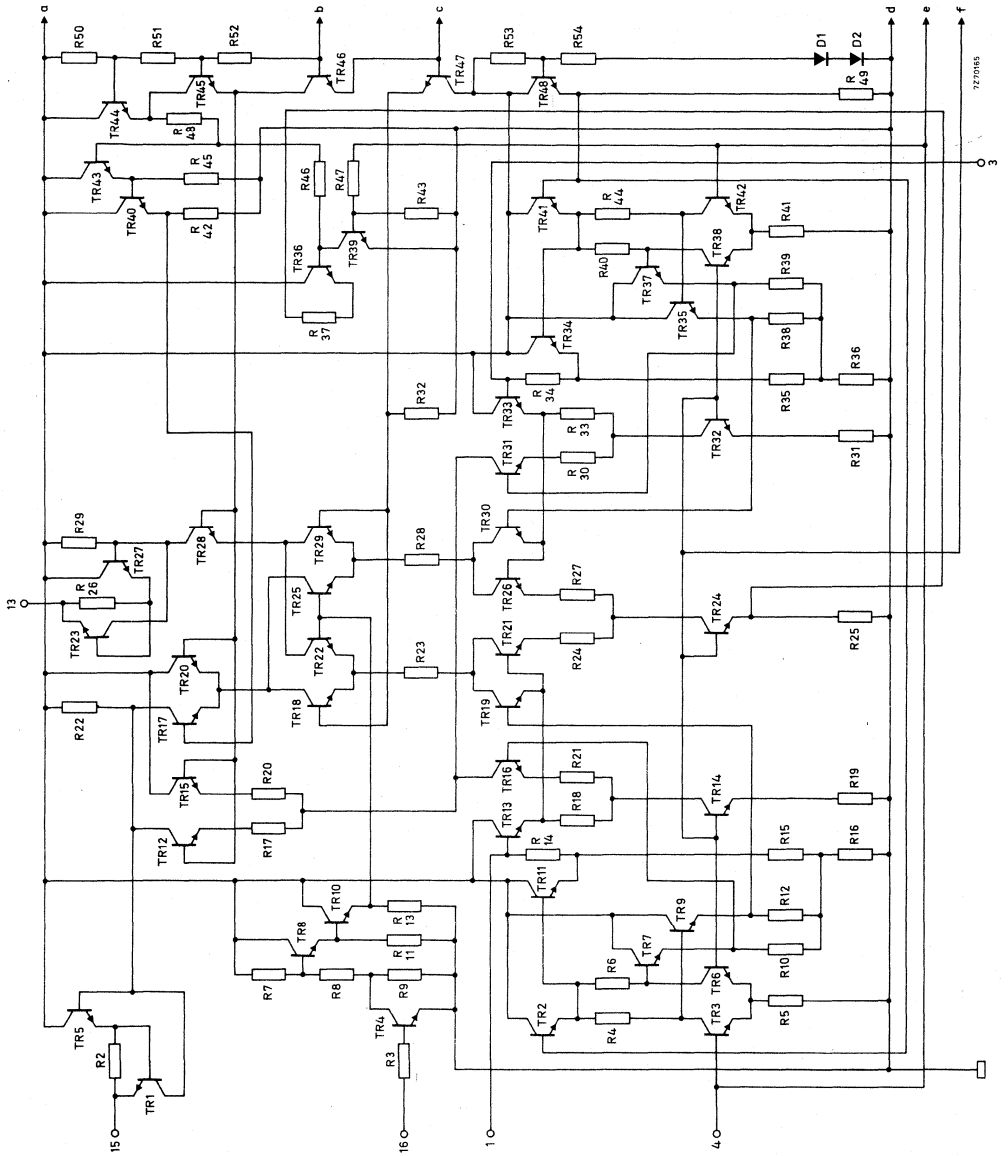
The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the D_R and D_B components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

QUICK REFERENCE DATA						
Supply voltage		V_{14-2}	nom.	12		V
Supply current		I_{14}	nom.	36		mA
				PAL	SECAM	
Chrominance input signals (peak-to-peak value)	$V_{1-2(p-p)}$ / $V_{3-2(p-p)}$		typ.	50	200	mV
System switch input	V_{4-2}		typ.	12	0	V
Colour difference output signals (peak-to-peak value)	(R-Y):	$V_{12-2(p-p)}$	typ.	1,1		V
	(B-Y):	$V_{10-2(p-p)}$	typ.	1,47		V
Reference input signals (PAL) (peak-to-peak value)		$V_{6-2(p-p)}$ / $V_{7-2(p-p)}$	typ.	1		V
Square-wave input (peak-to-peak value)		$V_{16-2(p-p)}$	typ.	3		V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).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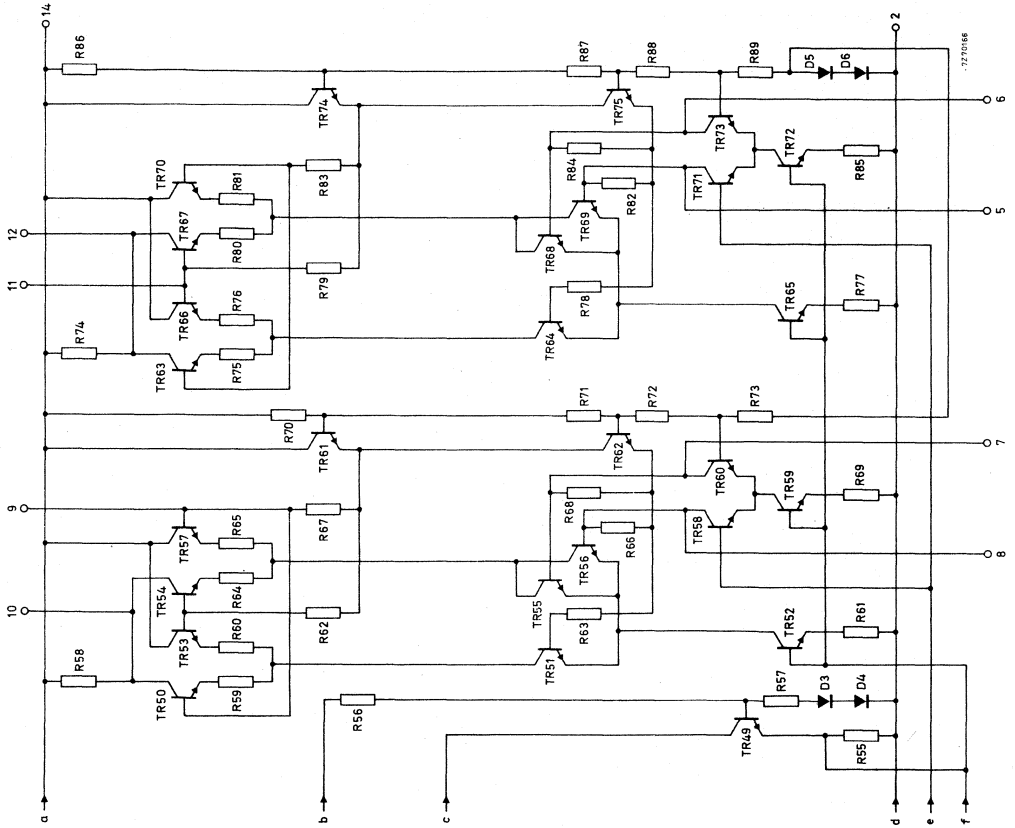
14
R86
R87
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{14-2}		max. 13,2	V
Power dissipation				
Total power dissipation	P_{tot}		max. 510	mW
Temperatures				
Storage temperature	T_{stg}		−25 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +65	°C [1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}		typ. 12 10,2 to 13,2	V V
Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C				
Chrominance input signal				
peak-to-peak value	$V_{1-2(p-p)}$ $V_{3-2(p-p)}$	PAL SECAM	35 to 75 150 to 400	mV mV
Input impedance	$\lvert Z_{1-2}\rvert$ $\lvert Z_{3-2}\rvert$		1,2 to 2,6	kΩ
PAL matrix				
Gain from both inputs to pin 13			2,3 to 3,3	
Gain from both inputs to pin 15			2,6 to 3,6	
Gain difference from line-to-line			< 5	%
Phase errors from line-to-line in the (R-Y) output for zero error in the (B-Y) output			< 2,5°	
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω
SECAM permutator				
Diaphotie			< −46	dB
Output signal (peak-to-peak value)	$V_{13-2(p-p)}$ $V_{15-2(p-p)}$		1,6 [2] to 2,2	V
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω

[1]) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

[2]) At an input voltage of 0,15 V; at an input voltage > 0,2 V the figure is 1,7 V.

CHARACTERISTICS (continued)

Demodulator

Chrominance input signal amplitude

PAL: (B-Y); peak-to-peak value		$V_{9-2(p-p)}$	typ.	0,22	V
(R-Y); peak-to-peak value		$V_{11-2(p-p)}$	typ.	0,28	V
SECAM: peak-to-peak value		$V_{9-2(p-p)}$ / $V_{11-2(p-p)}$		1,5 to 3	V
Input impedance		$\lvert Z_{9-2}\rvert$ / $\lvert Z_{11-2}\rvert$	>	1	kΩ

Reference input signal amplitude

PAL: peak-to-peak value		$V_{6-2(p-p)}$ / $V_{7-2(p-p)}$		0,5 to 1,5	V
SECAM: peak-to-peak value		$V_{5-2(p-p)}$ / $V_{8-2(p-p)}$		0,18 [1] to 1,5	V
Input impedance	$\lvert Z_{5-2}\rvert$; $\lvert Z_{7-2}\rvert$ / $\lvert Z_{6-2}\rvert$; $\lvert Z_{8-2}\rvert$			0,75 to 1,25	kΩ

Colour difference output signal

(R-Y); peak-to-peak value		$V_{12-2(p-p)}$		0,99 to 1,21	V [2]
(B-Y); peak-to-peak value		$V_{10-2(p-p)}$		1,32 to 1,62	V [2]
Output impedance		$\lvert Z_{10-2}\rvert$ / $\lvert Z_{12-2}\rvert$		2,4 to 4,2	kΩ

Diaphotie at SECAM operation

Diaphotie of the total circuit at frequencies corresponding to saturated green D_R = 4,72 MHz and D_B = 4,04 MHz			<	−40	dB

Square wave input

peak-to-peak value		$V_{16-2(p-p)}$		2,5 to 3,5	V
Input impedance		$\lvert Z_{16-2}\rvert$	>	3,8	kΩ

System switch input [3]

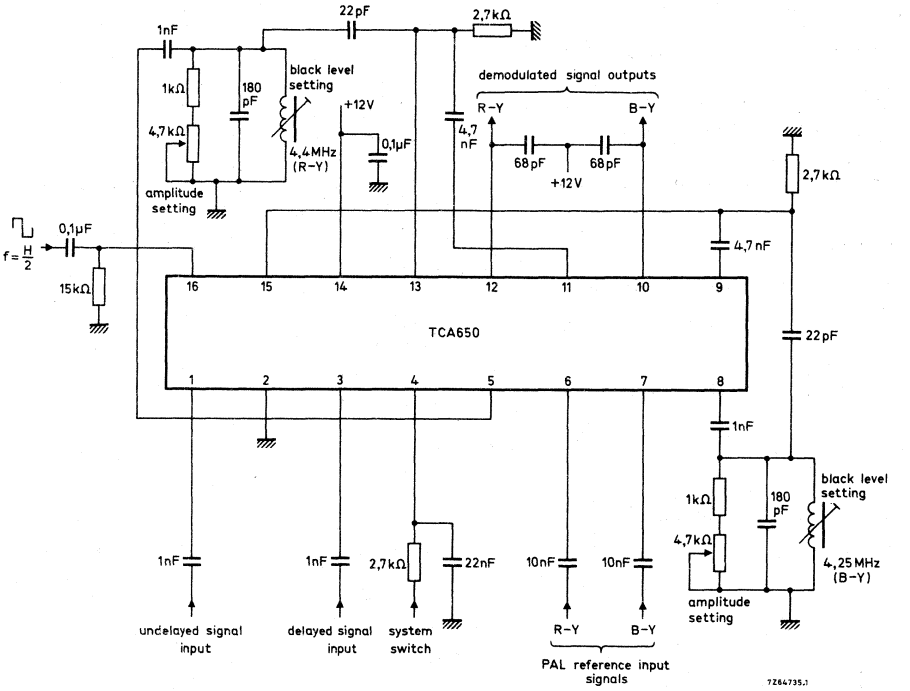
PAL:				7 to V_{14-2}	V
SECAM:				0 to 1	V

[1]) Limiting starts at the quoted value.

[2]) The peak-to-peak clipping level for PAL is about 4,7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3,6 V for (B-Y) and 2,4 V for (R-Y) (SECAM).

[3]) The switching signal is applied to pin 4 via a resistor of 2,7 kΩ (±10%).

APPLICATION INFORMATION



Pinning

1. Chrominance input
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Reference (R-Y) input SECAM
6. Reference (R-Y) input PAL
7. Reference (B-Y) input PAL
8. Reference (B-Y) input SECAM
9. Chrominance (B-Y), D_B input
10. Colour difference (B-Y) output
11. Chrominance (R-Y), D_R input
12. Colour difference (R-Y) output
13. Chrominance (R-Y), D_R output
14. Supply voltage (12 V)
15. Chrominance (B-Y), D_B output
16. Square wave input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance input

   The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)

3. Chrominance input

   The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 µs.

4. System switch input

   The control voltage for switching the standard is applied to this input via a resistor of 2,7 kΩ (± 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black (f_o = 4, 4 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

   A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

   A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black (f_o = 4, 25 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), D_B demodulator

   The output signal of pin 15 is applied via a coupling capacitor of 4, 7 nF.

10. Output of the (B-Y) demodulator

    The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), D_R demodulator

    The output signal of pin 13 is applied via a coupling capacitor of 4, 7 nF.

APPLICATION INFORMATION (continued)

12. Output of the (R-Y) demodulator

See pin 10.

13. Chrominance (R-Y), D_R output

The (R-Y) component of the chrominance signal (D_R component at SECAM) is present at this pin.
The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of <100 Ω.

14. Supply voltage (12 V)

Correct operation occurs within the range 10, 2 to 13, 2 V.
The power dissipation must not exceed 510 mW at 65 °C ambient temperature.

15. Chrominance (B-Y), D_B output

The (B-Y) component of the chrominance signal (D_B component at SECAM) is present at this pin.
The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of <100 Ω.

16. Square wave input

A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.
The square wave is available at pin 12 of the TCA640.

CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.
Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.
In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.
Brightness is controlled by varying the black level of the luminance signal at the output.
An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

QUICK REFERENCE DATA

Supply voltage	V_{13-4}	nom.	12	V	
Supply current	I_{13}	nom.	35	mA	
Luminance input current (black-to-white positive video signal)	I_{16}	typ.	0,7	mA	
Luminance output voltage (black-to-white positive video signal; peak-to-peak value)	$V_{1-4(p-p)}$	typ.	3	V	1)
Black level (nominal value)	V_{1-4}	typ.	4,2	V	
Brightness control (around nominal black level)	V_{1-4}		+1 to −2	V	
Gain of the (R-Y) and (B-Y) amplifier		typ.	5	dB	1) 2)
Gain of the (G-Y) amplifier		typ.	1		
Contrast control range			+3 to −20	dB	3)
Saturation control range			+6 to −20	dB	3)

1) At nominal contrast setting (max. contrast −3 dB)

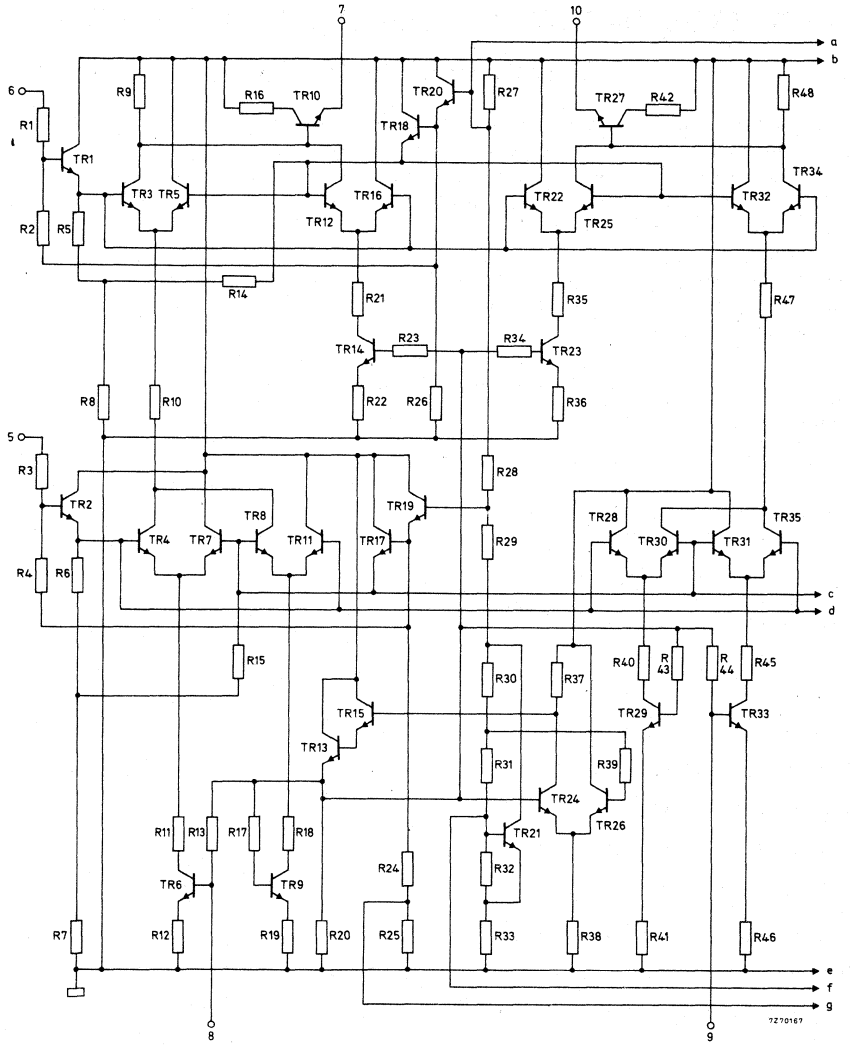
2) At nominal saturation control setting (max. saturation −6 dB)

3) Nominal contrast and nominal saturation are specified as 0 dB.

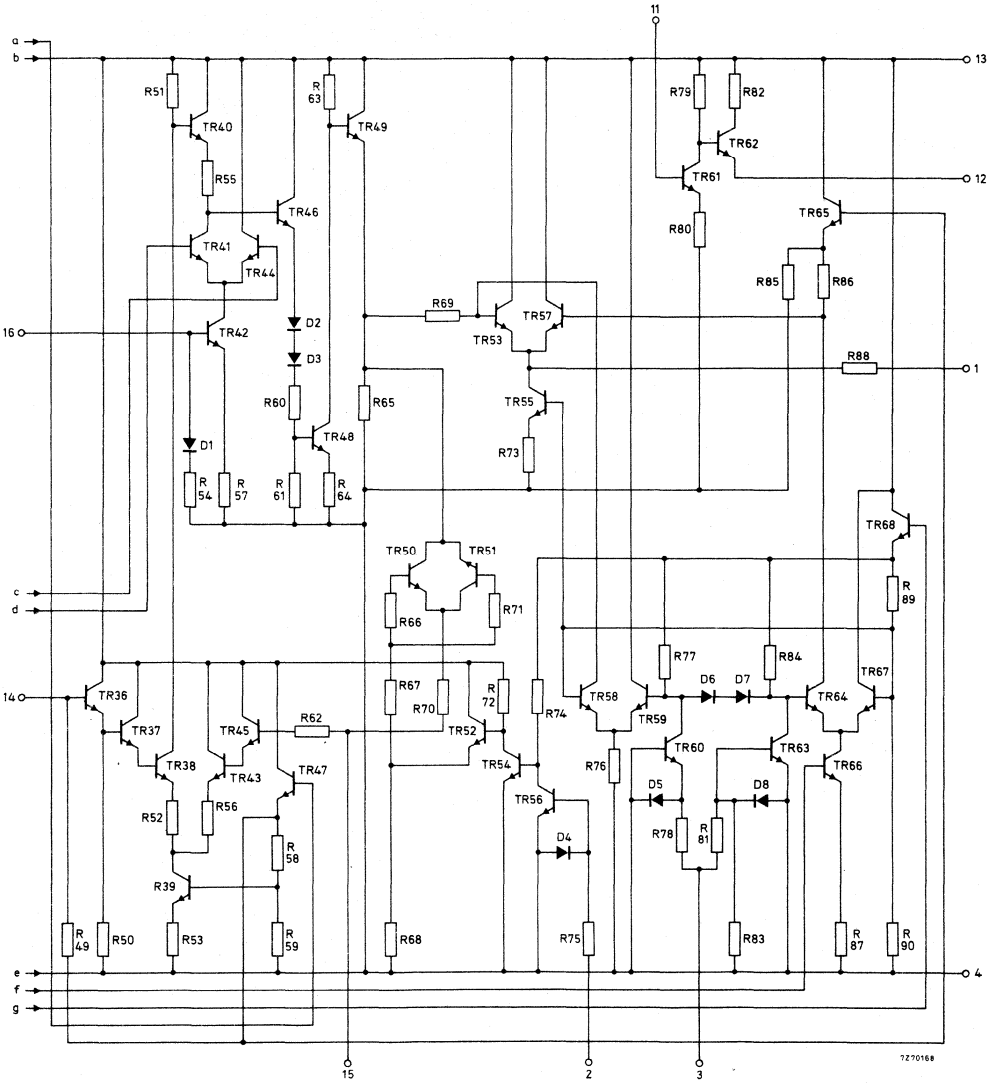
PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage			
Supply voltage	V_{13-4}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	600 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C [1]

CHARACTERISTICS measured in the circuit on page 7

Supply voltage	V_{13-4}	typ.	12 V 10,2 to 13,2 V
Required input signals at V_{13-4} = 12 V and T_{amb} = 25 °C			
Luminance input current			
black-to-white positive video signal	I_{16}	typ.	0,7 mA 0 to 2,5 mA
Input impedance at I_{16} = 1 mA	$\lvert Z_{16-4}\rvert$		60 to 90 Ω
Input impedance variation for an			
input current variation $\Delta I_{16} = \pm 0,5$ mA	$\lvert \Delta Z_{16-4}\rvert$		∓25 Ω
Colour difference input voltage			
(R-Y); peak-to-peak value	$V_{9-4(p-p)}$	<	0,7 V
(B-Y); peak-to-peak value	$V_{8-4(p-p)}$	<	0,9 V
Input voltage variation before clipping			
of the output voltage occurs	ΔV_{8-4} ΔV_{9-4}	typ.	0,8 V
Input impedance	$\lvert Z_{8-4}\rvert$ $\lvert Z_{9-4}\rvert$		3,5 to 6,5 kΩ
Blanking pulse (peak value)	V_{3-4M}		−1,5 to −10 V
Black level reinsertion pulse (peak value)	V_{3-4M}		+2 to +12 V [2]
Black level clamp pulse (peak value)	V_{2-4M}		+1 to +12 V
Luminance output voltage at nominal contrast			
black-to-white positive video signal; peak-to-peak value	$V_{1-4(p-p)}$		2 to 4 V [3]

1) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.
2) During scan V_{3-4} must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.
3) Nominal contrast is specified as maximum contrast −3 dB.

CHARACTERISTICS (continued)

Black level at nominal brightness setting	V_{1-4}	typ.	4,2	V	1)
Black level variation with brightness setting	ΔV_{1-4}		+1 to −2	V	
Contrast control voltage range	V_{5-4}	See graph on page 6			
Black level variation with contrast control	ΔV_{1-4}	<	40	mV	2)
Black level variation with video contents	ΔV_{1-4}	<	20	mV	3)
Variation between video black level and reinserted black level at ΔT_{amb} = 25 °C and ΔV_{13-4} ± 10%	V_{1-4}	<	±20	mV	
Blanking level with respect to nominal brightness	V_{1-4}		−0,8 to −1,2	V	
Bandwidth (−3 dB) of luminance signal	B	>	6	MHz	
Colour difference output signal for nominal contrast and saturation 4) 5)					
(R-Y); peak-to-peak value	$V_{10-4(p-p)}$	typ.	1,25	V	6)
(B-Y); peak-to-peak value	$V_{7-4(p-p)}$	typ.	1,6	V	6)
D.C. output level	V_{7-4} / V_{10-4}	typ.	6,1	V	
Output level variation with contrast and saturation control	ΔV_{7-4} / ΔV_{10-4}	<	500	mV	
Permissible d.c. load impedance	$\lvert Z_{7-4}\rvert$ / $\lvert Z_{10-4}\rvert$	>	4	kΩ	
Saturation control voltage range	V_{6-4}	See graph on page 6			
Saturation control at $V_{6-4} < 0,5$ V		<	−50	dB	
Bandwidth (−3 dB) of colour difference signal	B	>	2,5	MHz	

1) Nominal brightness setting V_{14-4} = 5,7 V.
2) Only valid if the input current does not exceed 0,5 mA during black.
3) For a.c. coupling only.
4) Nominal contrast is specified as maximum contrast −3 dB.
5) Nominal saturation is specified as maximum saturation −6 dB.
6) This value is obtained at the specified maximum input voltage.

CHARACTERISTICS (continued)

(G-Y) amplifier

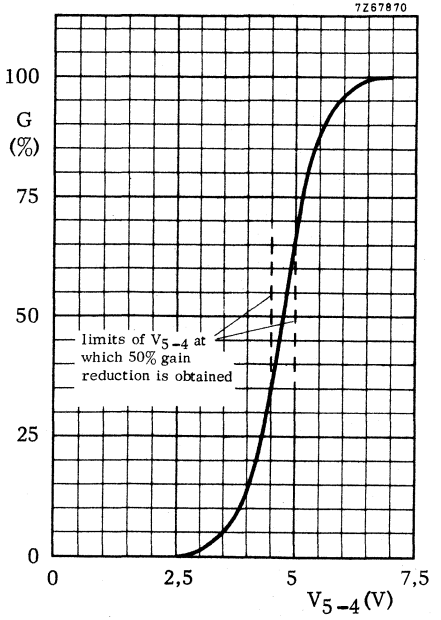
input voltage (peak-to-peak value)	$V_{11-4(p-p)}$	<	1	V
output voltage (peak-to-peak value)	$V_{12-2(p-p)}$	<	1	V
voltage gain	G_{11-12}		−1 to +0,5	dB

Tracking during contrast and saturation control

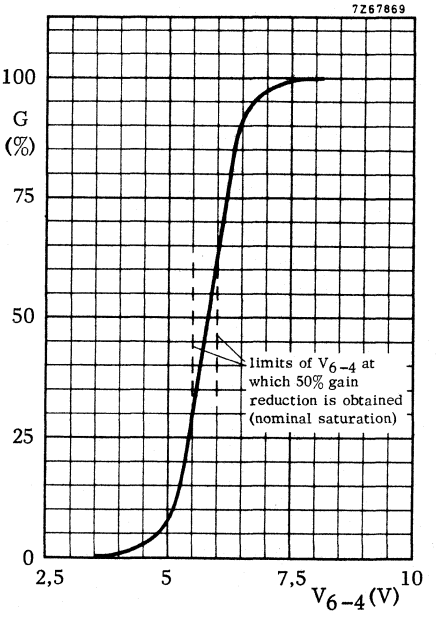
at a contrast decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB
change of the ratio $\frac{Y}{(B-Y)}$			0 to 4	dB
at a saturation decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB

Cross coupling

luminance signal to colour difference signal		<	−40	dB
(B-Y) signal to (R-Y) signal		<	−30	dB
colour difference signal to luminance signal		<	−40	dB

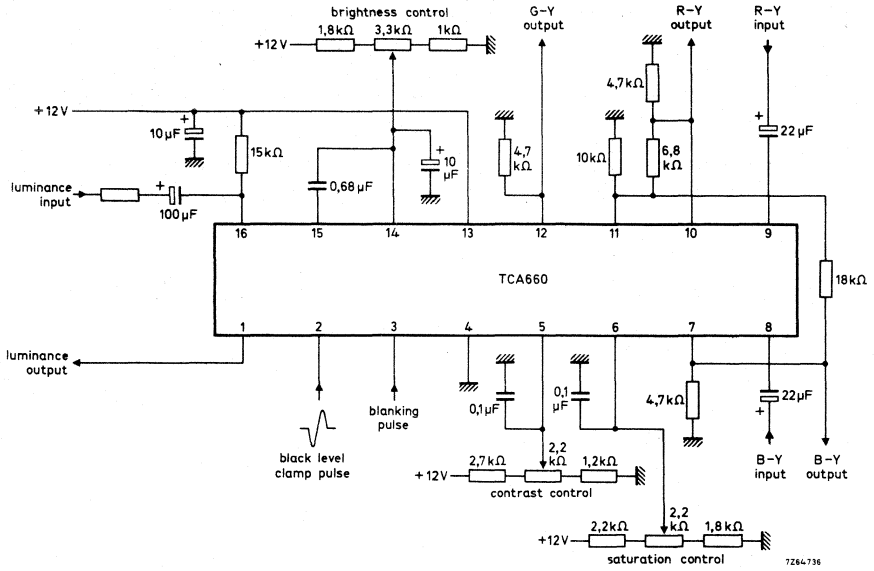


Contrast control of luminance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



Pinning

1. Luminance signal output
2. Black level clamp pulse input
3. Blanking pulse input
4. Earth (negative supply)
5. Contrast control input
6. Saturation control input
7. (B-Y) signal output
8. (B-Y) signal input
9. (R-Y) signal input
10. (R-Y) signal output
11. (G-Y) signal input
12. (G-Y) signal output
13. Supply voltage (12 V)
14. Brightness control input
15. Black level clamp capacitor
16. Luminance signal input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Luminance signal output

   A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.
   By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

   A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 µs.

3. Blanking pulse input

   Two modes operation can be selected by the choice of the amplitude of the pulse applied:

   - blanking

   - black level reinsertion

   Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from −1,5 to −10 V. An artificial black level of nominally +4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to +12 V.
   During scan the amplitude at pin 3 should remain between +0,7 V and −0,7 V to avoid blanking.

4. Negative supply (earth)

5. Contrast control input

   The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

   The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

   The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ±0,8 V is provided, whereas the input signal has a typical value of ±0,45 V for a saturated colour bar signal.

APPLICATION INFORMATION (continued)

9. (R-Y) signal input

The signal has to be a.c. coupled to the input.
To cope with the variation of picture contents an input voltage margin of ± 0, 8 V is provided, whereas the input signal has a typical value of ± 0, 35 V for a saturated colour bar input.

10. (R-Y) signal output

The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1, 25 V peak-to-peak is obtained at an input amplitude of 0, 7 V peak to peak.
The average level is typically 6, 1 V.

11. (G-Y) signal input

The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6, 5 V.
An average level of typical 5, 9 V is required to produce an average output level of 6, 1 V.
The gain of the inverter stage is typically 1.

12. (G-Y) signal output

An inverted signal with an amplitude of maximum 1 V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

Correct operation occurs within the range 10, 2 to 13, 2 V.
The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

The black level of the luminance output signal tracks the potential applied to this pin.
A typical value for setting the brightness control is 5, 7 V, for which a black level of 4, 2 V is obtained.
It is recommended that a capacitor of at least 10 µF be connected between this pin and earth.

15. Black level clamp capacitor

The level of the back porch of the luminance output signal is stored in an external capacitor of about 0, 68 µF; the latter to be connected between pins 14 and 15.

16. Luminance signal input

A positive luminance signal of 0, 7 mA peak-to-peak between black and white level drives the luminance amplifier.
A black level of about 0, 3 mA is recommended. For a.c. coupling a bias resistor to the supply line is required to bias the amplifier properly.
The resistance depends on the signal amplitude e. g.: 15 kΩ is recommended for a input signal of 0, 7 mA peak-to-peak.

MULTI-STABILIZER FOR ELECTRONIC TUNING

The TCA750 is basically a stabilizer for use in electronic tuning systems. The circuit is combined with an external reference diode which entirely determines the thermal stability of the system and can be adapted to the stability requirements of AM, FM or TV receivers.

The reference diode BZV38 used in conjunction with the TCA750 form an ideal pair for FM tuners in radio or TV receivers.

Additional to a stabilized voltage (V_o1) for the electronic tuning system, the TCA750 incorporates two other output voltages (V_o2 and V_o3) for stabilized supply of the entire receiver combination as well as the following attractive features:

- The output current of any of the three stabilizers can be increased by a discrete power transistor without affecting circuit stability.
- For mute control at switching on, V_o2 can be delayed by external components.
- An a.f.c. coupling circuit provides a constant correction factor by superimposing an a.f.c. voltage on V_o1.
- Adjustable a.f.c. amplification factor (< 5).
- Pulse or touch contact operation switches off the a.f.c. whilst changing stations.
- Delayed switching on of the a.f.c., externally adjustable ($t_d < 2$ s).
- Search tuning becomes very simple when using the a.f.c. current source (pin 10).
- All three stabilized outputs are protected against short-circuit and are individually adjustable.

QUICK REFERENCE DATA see page 2

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

QUICK REFERENCE DATA

Input voltage range	$V_{13\text{-}16}$	26,5 to 54	V
Ambient temperature	T_{amb}	typ. 25	°C
Input voltage	$V_{13\text{-}16}$	typ. 45	V
→ Tuning voltage (V_o1) *	$V_{12\text{-}16}$	21 to 34	V
Output current (I1) *	I_{12}	< 14,5	mA
Stabilizing time	t_{stab}	typ. 0,8	s
Temperature coefficient (V_o1)			
TCA750	$\Delta V_o1/\Delta T$	typ. 1	ppm/°C
BZV38		typ. 30	ppm/°C
Line regulation	$\Delta V_o1/\Delta V_{in}$	typ. 10	ppm/V
→ Output voltage (V_o2) *	$V_{14\text{-}16}$	8 to 21	V
Output current (I2) *	I_{14}	< 6	mA
→ Output voltage (V_o3) *	$V_{2\text{-}16}$	8 to 29	V
Output current (I3) *	I_2	< 6	mA

* Symbols used in test circuit Fig. 3.

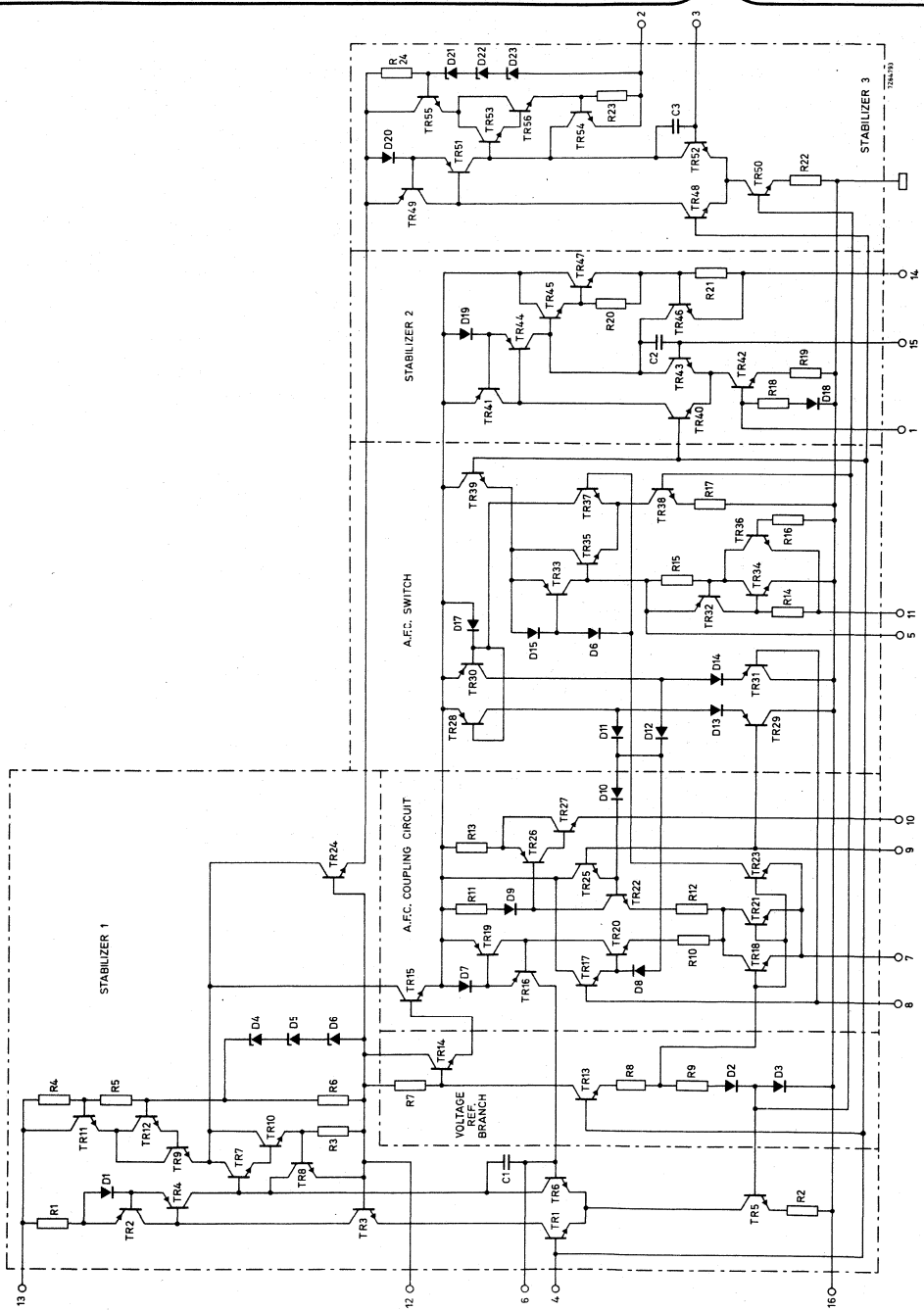


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input voltage (supply)	V_{13-16}	max.	54 V
A.F.C. input voltages (pins 8 and 9)	V_{8-16}, V_{9-16}	max.	17 V
	$\pm V_{8-9}$	max.	6 V
Output current			
pin 12	I_{12}	max.	55 mA
pin 14	I_{14}	max.	20 mA
pin 2	I_2	max.	25 mA
Input current (pin 11)	$\pm I_{11}$	max.	6 mA
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C *
Total power dissipation	see derating curve Fig. 2		

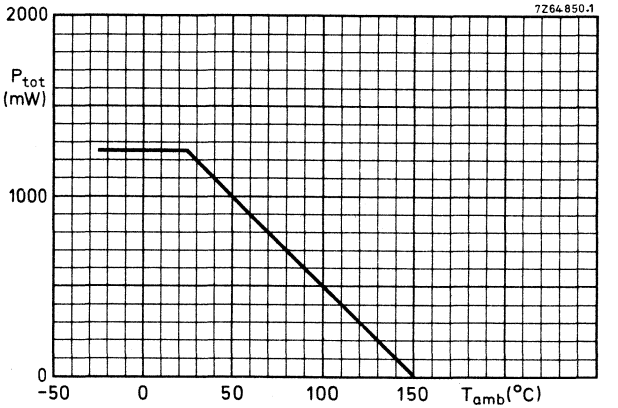
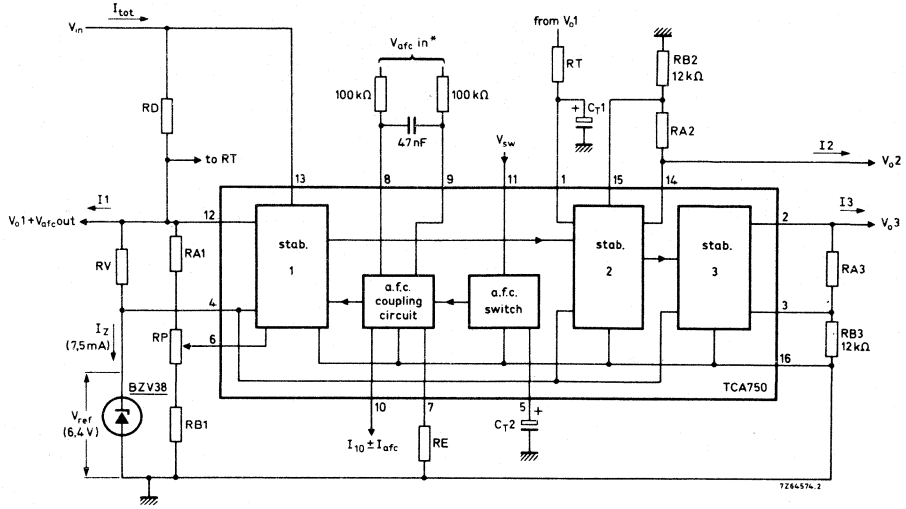


Fig. 2 Power derating curve.

* See derating curve Fig. 2.



* V_{afc}in is superimposed on a common-mode voltage (V_{com}) of 5 V to 17 V.

Fig. 3 Test circuit and multi-stabilizer peripheral components.

Note to power reduction resistor RD

For worst case conditions (maximum output currents of the three stabilizers and a high supply voltage V_{in}) the power dissipation (P_{tot}) must be reduced by the use of the external resistor RD.

$$\text{Power reduction} = \frac{(V_{in} - V_o1)^2}{RD}$$

The minimum permissible value of RD is derived by the formula

$$RD_{min} = \frac{V_{in\,max} - V_o1 - V_{afc}out}{I_{12} - I_{13\,min}}$$

where,

$I_{13\,min}$ = 4,5 mA (stand-by current I_s)

$I_{12} = I_Z + I_{RA1} + I1_{min}$

CHARACTERISTICS and APPLICATION INFORMATION

T_{amb} = 25 °C; see test circuit Fig. 3.

		note	min.	typ.	max.	
Supplies						
Input voltage	V_{in}	1	26,5	–	54	V
Input current	I_{tot}	2	–	–	31	mA
Output characteristics						
D.C. output resistance (all stabilizers)	R_{out}	–	–	1	–	Ω
Permissible output short-circuit duration						
stabilizer 1	t_{short}	–	continuous			
stabilizers 2 or 3		–	–	–	10	s
Stabilizer 1						
→ Output voltage range (adjustable)	V_o1	3	21	–	34	V
Output current	$I1$	4, 5	0	–	5	mA
Stabilizing time	t_{stab}	6	–	–	1	s
Output voltage temp. coefficient	$\Delta V_o1/\Delta T$	7, 8	–	40	–	ppm/°C
Line regulation	$\Delta V_o1/\Delta V_{in}$	8	–	10	–	ppm/V
A.F.C. coupling circuit						
A.F.C. input voltage (½ V_{afc} swing)	V_{afc} in	–	–	–	5	V
A.F.C. output voltage (½ V_{afc}lim swing)	V_{afc} lim	15, 16	–	–	0,9	V
A.F.C. output current threshold	I_{10}	15, 16	–	–	1,5	mA
A.F.C. output current swing	I_{afc} lim	15, 16	–	–	3,0	mA
A.F.C. off delay	t_d	–	–	2	–	s
Amplification factor	μ	–	–	–	5	
A.F.C. slope ($\Delta I_{afc}/\Delta V_{afc}$ in)	S	14	–	2,5	–	mA/V
Common-mode voltage	V_{com}	9	5	–	17	V
V_o1 change due to a.f.c. switching	ΔV_o1/afc	–	–	–	25	mV
Asymmetry of a.f.c. input (a.f.c. off)	± (I_g-I_g)	–	–	–	0,5	μA
A.F.C. switch operated by manual switch						
Input voltage (a.f.c. on)	V_{sw}	–	–0,5	–	+0,5	V
Positive input voltage (a.f.c. off)	$+V_{sw}$	–	0,8	–	6	V
Negative input voltage (a.f.c. off)	$-V_{sw}$	–	0,8	–	–	V
Positive input current (a.f.c. off)	$+I_{11}$	–	0,004	–	3	mA
Negative input current (a.f.c. off)	$-I_{11}$	–	0,8	–	2	mA
A.F.C. switch operated by pulse						
Positive trigger pulse peak current	$+I_{11}$ pulse	13				
pulse width = 10 μs		–	800	–	3000	μA
100 μs		–	80	–	3000	μA
1 ms		–	8	–	3000	μA
10 ms		–	4	–	3000	μA
Negative trigger pulse peak current	$-I_{11}$ pulse	–	0,8	–	2	mA
Negative trigger pulse width		–	10	–	–	μs

		note	min.	typ.	max.		
Stabilizer 2							
Output voltage range (adjustable)	V_o2	10	8	–	21	V	←
Output current	$I2$	5	0	–	5,5	mA	
Output voltage temp. coefficient	$\Delta V_o2/\Delta T$	7, 8	–	45	–	ppm/°C	
Switch-on delay time	$t_{d\,on}$	11	0	–	6	s	
Switching voltage	$V_{1\text{-}16}$	–	0,8	–	1	V	
Stabilizer 3							
Output voltage range (adjustable)	V_o3	12	8	–	29	V	←
Output current	$I3$	5	0	–	5,5	mA	
Output voltage temp. coefficient	$\Delta V_o3/\Delta T$	7, 8	–	45	–	ppm/°C	

Notes

1. The V_{in} range depends on the value of V_o1 (see Fig. 4).
2. At $I1 = 5$ mA, $I2 = I3 = 5{,}5$ mA, $I_{10} = 0$.
3. Adjustable by means of RA1, RB1 and RP.
4. If a higher level is required from the output of stabilizer 1, the reference diode supply may be obtained from the emitter of a power transistor connected to the output from stabilizer 3 (see Fig. 8). In this case, the current available from stabilizer 1 is increased to 12,5 mA (bleeder current $I_{RA1} = 2$ mA).
5. At $T_{amb} = 60$ °C maximum with all stabilizers at rated currents.
6. With V_o1 within 0,05% of its steady value.
7. Temperature coefficient at T_{amb} from 10 °C to 60 °C with V_{in} constant, and using metal film bleed resistors having a temperature coefficient of $\leqslant 50$ ppm/°C.
8. With all stabilizer output currents constant and within the specified limits.
9. Common-mode voltage = voltage between pins 8 and 16, and 9 and 16 of the I.C.
10. V_o2 depends on the value of V_o1 (see Fig. 6); adjustable with RA2.
11. Adjustable by means of RT and C_T1. The delay time is limited by the leakage current of C_T1.
12. V_o3 depends on the value of V_o1 (see Fig. 7); adjustable with RA3.
13. The delay time after triggering depends on the value of C_T2.
14. With RE = 10 kΩ and $T_{amb} = 25$ °C.
15. V_{afc} out at V_{afc} in after limiting.
16. With RE = 10 kΩ; RA1 = 12 kΩ.

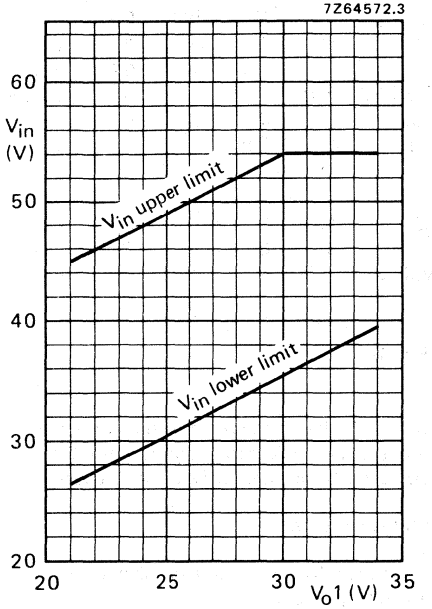


Fig. 4 Range of values for V_o1.

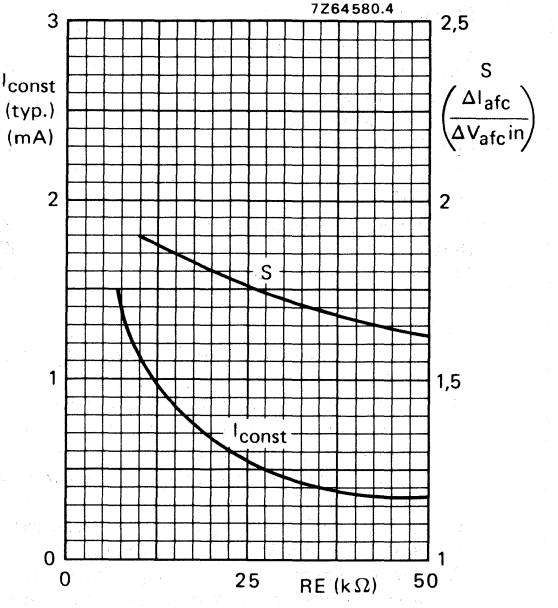


Fig. 5 Determination of I_{10} and S-factor (S = a.f.c. slope) from RE.

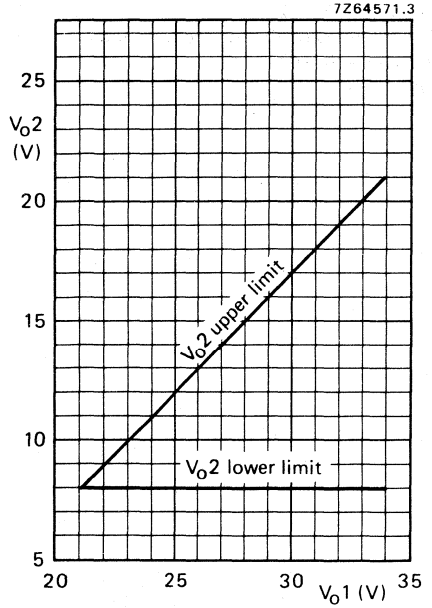


Fig. 6 Range of values for V_o2.

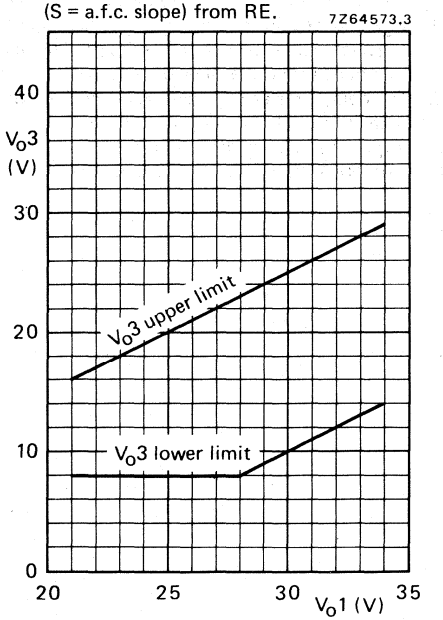


Fig. 7 Range of values for V_o3.

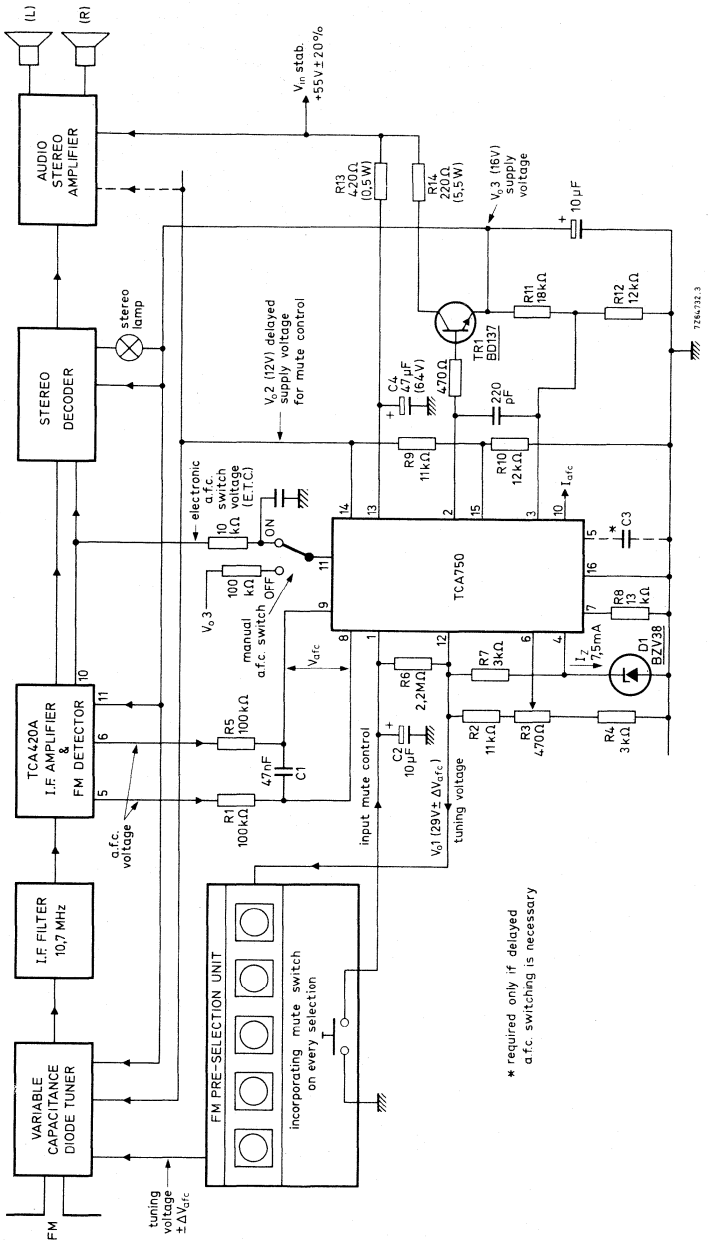


Fig. 8 Hi-fi radio receiver with electronic tuning using TCA750.

DOUBLE BALANCED MODULATOR/DEMODULATOR

The TDA0820 is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

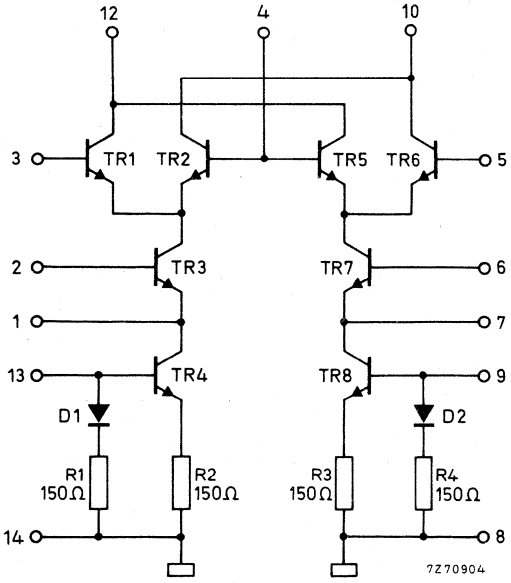


Fig. 1 Circuit diagram.

PACKAGE OUTLINE

14-lead 4-side; plastic (SOT-43).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{10-8}; V_{10-14}; V_{12-8}; V_{12-14}	0 to 13,2	V
Voltages (each transistor)			
Collector-substrate voltage (open base) and emitter)	V_{CSO}	max. 15	V
Collector-base voltage (open emitter)	V_{CBO}	max. 12	V
Collector-emitter voltage (open base)	V_{CEO}	max. 10	V
Emitter-base voltage (open collector)	V_{EBO}	max. 5	V
Currents (each transistor)			
Emitter current	I_E	max. 10	mA
Base current	I_B	max. 10	mA
Total power dissipation when mounted on a printed-circuit board	P_{tot}	max. 250	mW
Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	= 220	K/W

CHARACTERISTICS

$V_{10-8} = V_{10-14} = V_{12-8} = V_{12-14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply current	$I_{10} + I_{12}$	typ.	2,5	mA
		<	3	mA
Input signals				
carrier signal (r.m.s. value)	$V_{3-4(rms)}$; $V_{5-4(rms)}$	<	100	mV
video signal; negative modulated (peak-to-peak value)	$V_{6-2(p-p)}$	≤	1,4	V
Output signal at top sync over 75 Ω (peak-to-peak value)	$V_{10-12(p-p)}$	>	22	mV
Carrier suppression in balanced condition	V_{10-12}	>	38	dB
Differential phase		<	6°	
Differential gain		<	15	%
Distortion of video signal		<	−38	dB

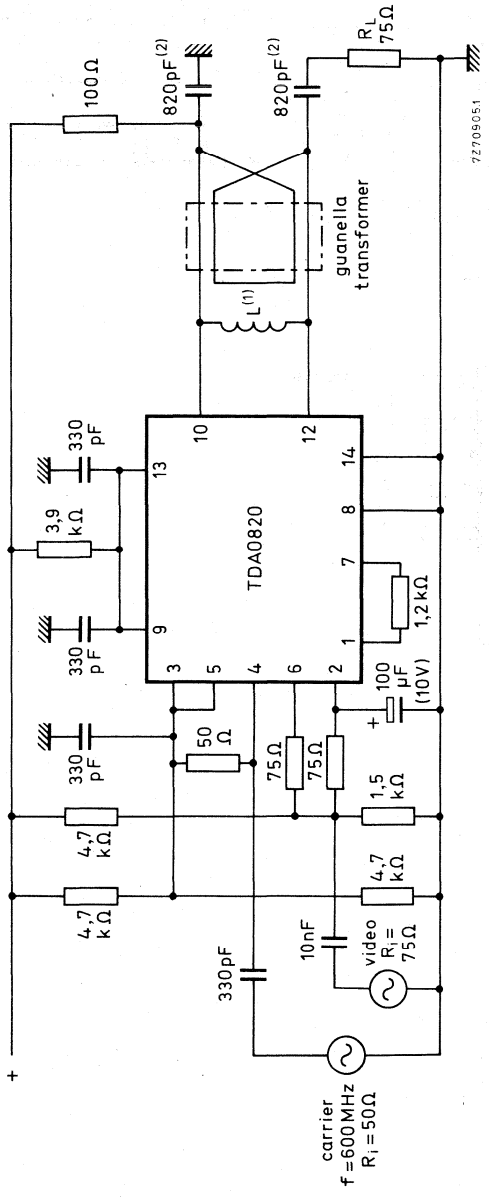
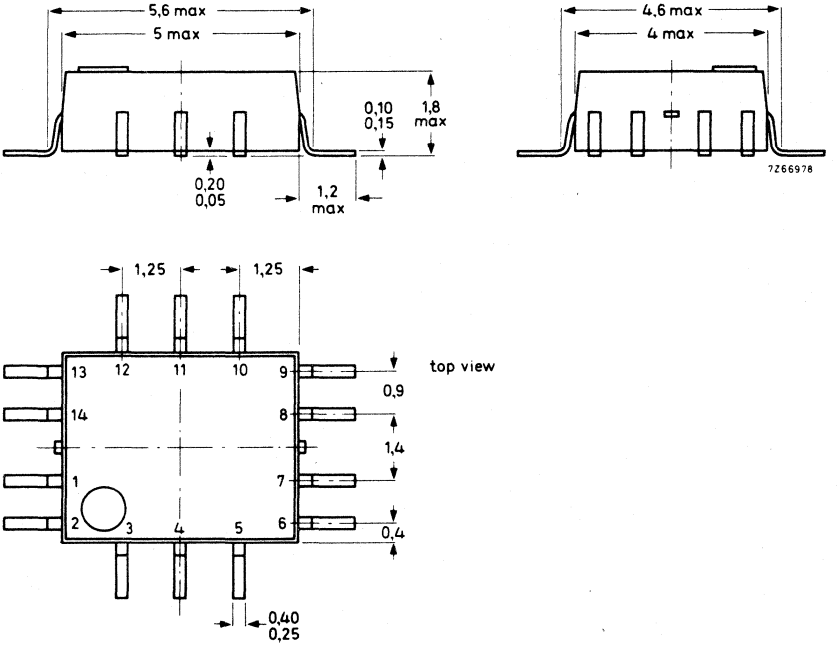


Fig. 2 Test circuit.

(1) L = air coil; 3 turns; ϕ 3 mm.
(2) U.H.F. decoupling capacitor 2212 669 98003.

14-LEAD 4-SIDE; PLASTIC (SOT-43)

Dimensions in mm



12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131B).

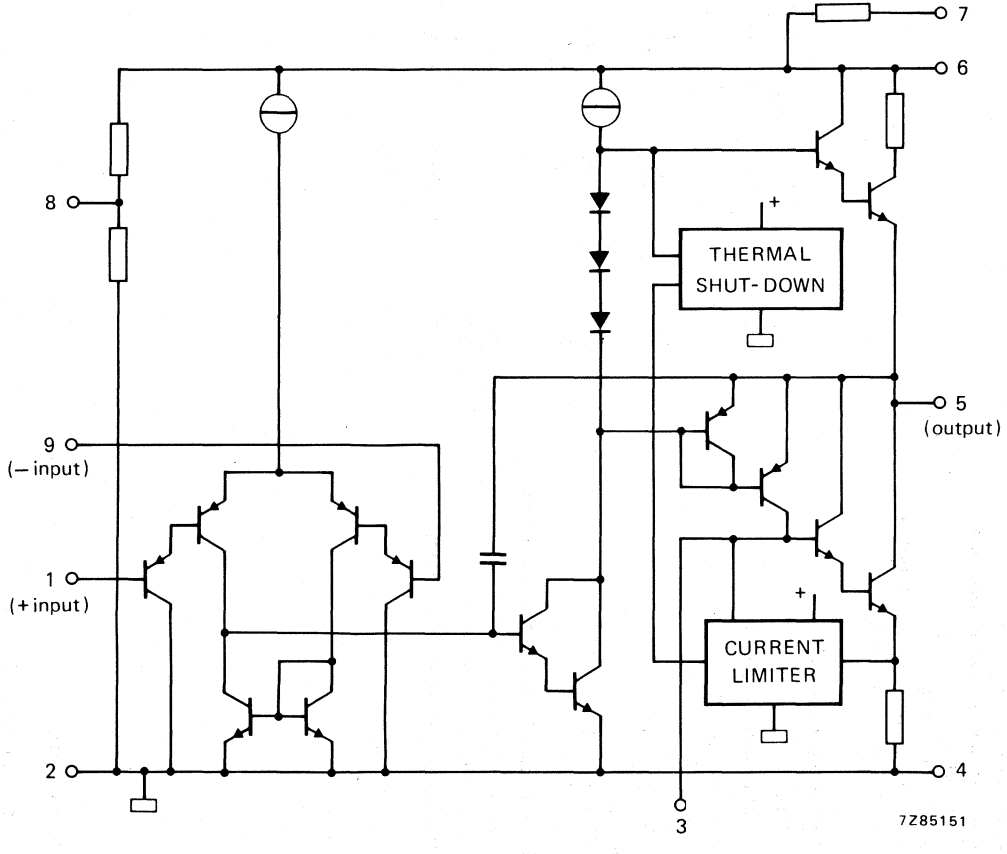


Fig. 1 Simplified internal circuit diagram.

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

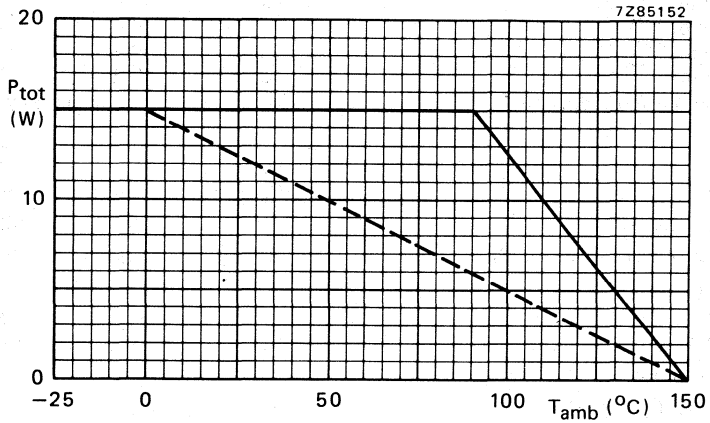


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −3 dB; d_{tot} = 0,7 %	B		20 Hz to 20 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ.	72 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

DEVELOPMENT SAMPLE DATA

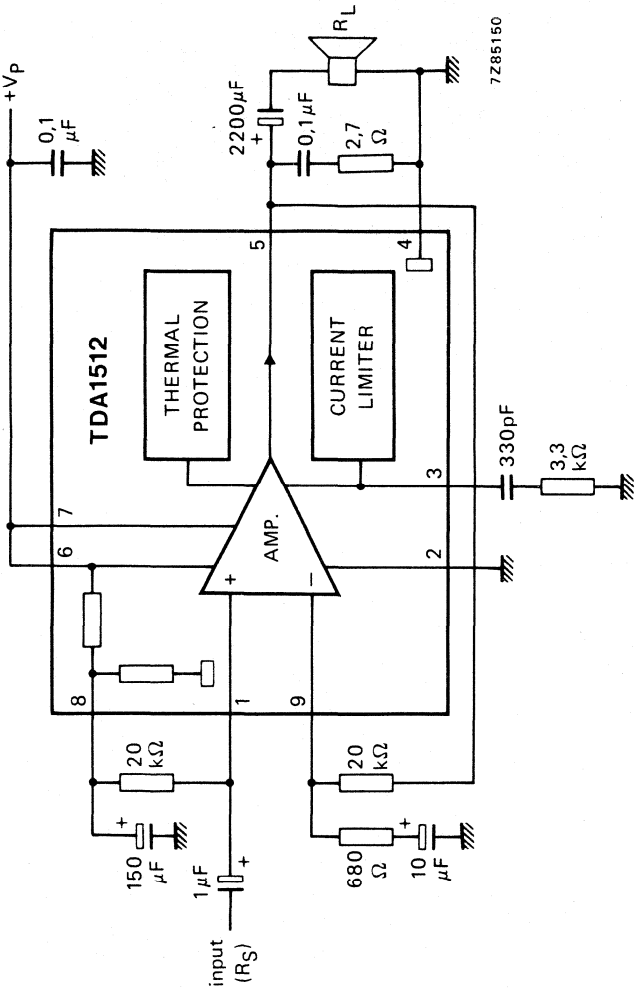


Fig. 3 Test circuit.

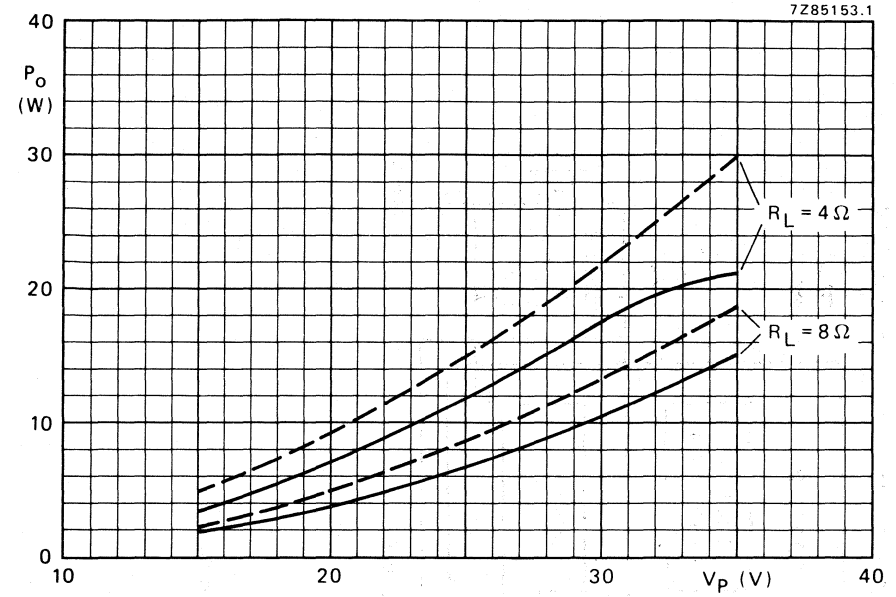


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

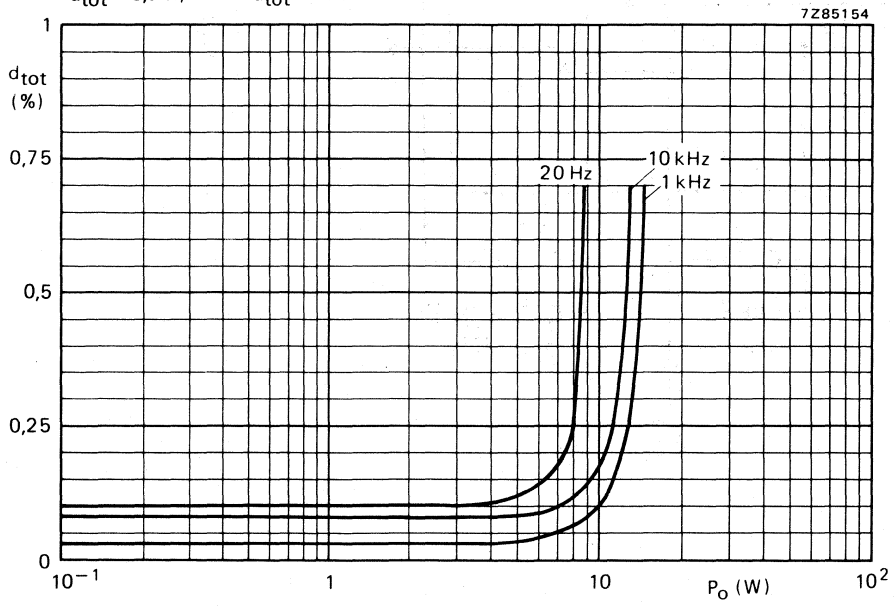


Fig. 5 Total harmonic distortion as a function of the output power.

CHROMINANCE COMBINATION

The TDA2510 is an integrated chrominance amplifier circuit for colour television receivers incorporating the following functions:

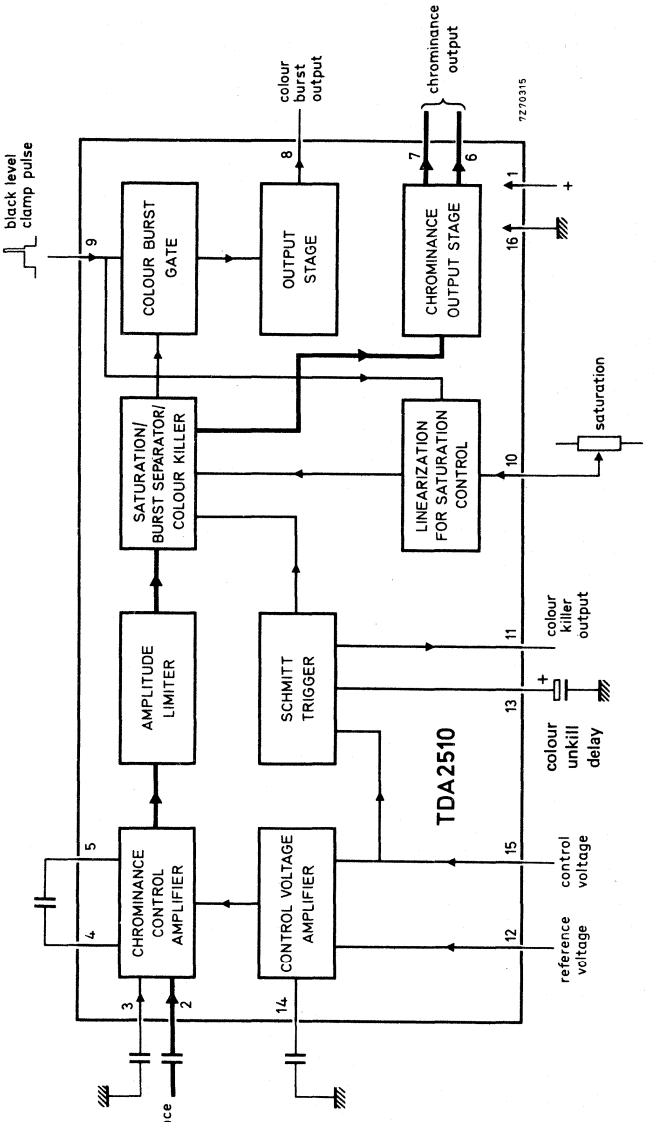
- chrominance amplifier with a.c.c.
- control voltage amplifier
- burst separator
- colour killer and colour killer voltage detector
- linear electronic potentiometer for saturation control
- Schmitt trigger for colour killer
- chrominance delay line driver stage
- colour burst output stage

QUICK REFERENCE DATA				
Supply voltage	V_{1-16}	typ.	12	V
Input signal (colour bars) peak-to-peak value	$V_{2-16(p-p)}$	typ.	100	mV
Output signal (colour bars) peak-to-peak value	$V_{7-16(p-p)}$	typ.	0,5	V
Burst signal output peak-to-peak value	$V_{8-16(p-p)}$	typ.	0,5	V

PACKAGE OUTLINES

TDA2510 : 16-lead DIL; plastic (SOT-38).
TDA2510Q : 16-lead QIL; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage (pin 1)	V_{1-16}	max.	15	V
Power dissipation				
Total power dissipation	P_{tot}	max.	500	mW
Temperatures				
Storage temperature	T_{stg}		−20 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C

Chrominance input signal				
Input voltage (symmetrical or asymmetrical) colour bars (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	100	mV
Input voltage range	V_{2-16}		10 to 200	mV
Input impedance	$\lvert Z_{2-16} \rvert$	>	2	kΩ
Burst signal output (emitter follower)				
D.C. voltage	V_{8-16}	typ.	9	V
Output signal (peak-to-peak value)	$V_{8-16(p-p)}$	typ.	0,5	V [1]
Limiting level of output signal (peak-to-peak value)	$V_{8-16(p-p)}$	typ.	1,5	V
Chrominance output signal (without burst)				
D.C. voltage	V_{6-16}	typ.	7	V
Output signal (colour bars) at nominal saturation (see note 2) and maximum contrast (peak-to-peak value)	$V_{6-16(p-p)}$	typ.	0,5	V
Signal-to-noise ratio	S/N	>	50	dB
Saturation control range			+6 to −50	dB
Phase angle compared to burst output at nom. saturation	$\Delta\varphi_B$	<	±5°	
Phase angle shift during saturation control range +6 to −50 dB	$\Delta\varphi_C$	<	±5°	
Collector current of output transistor	I_7	<	20	mA

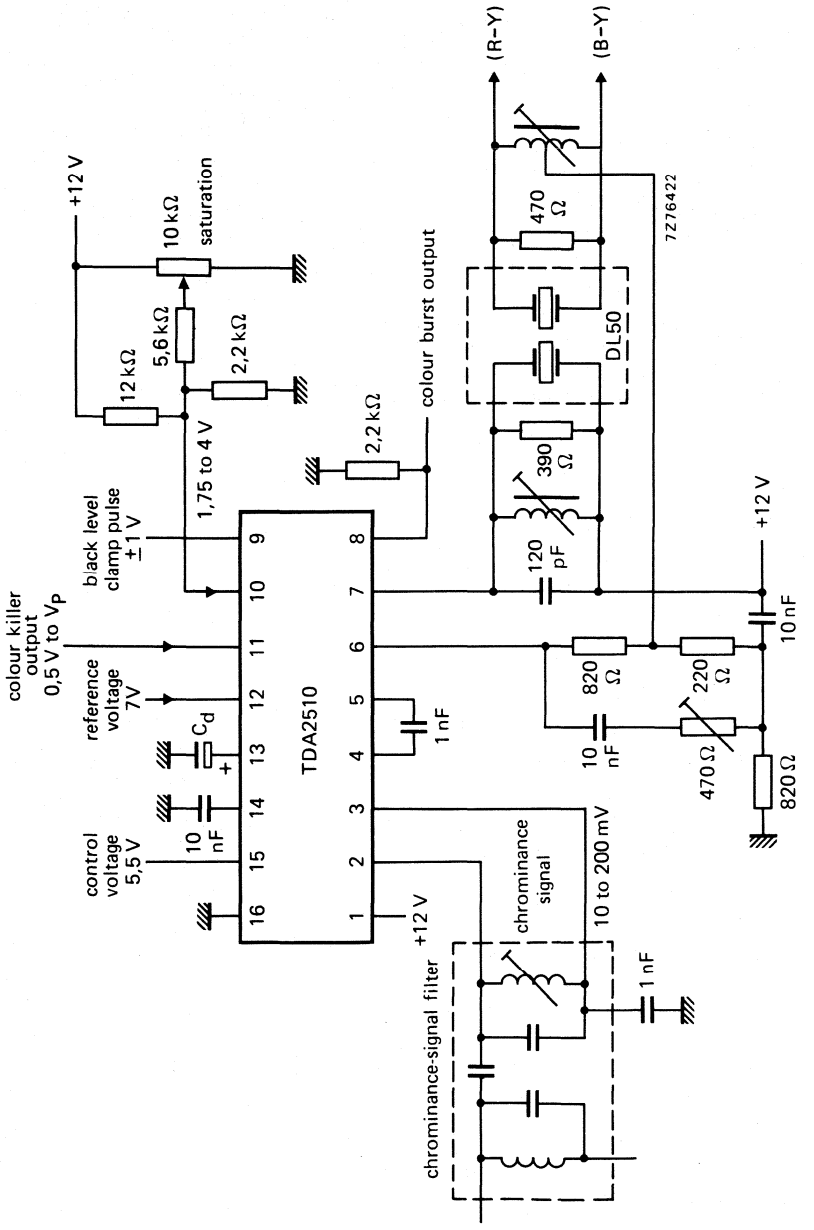
[1]) Kept constant by a.c.c. circuit.

[2]) Nominal saturation is defined as maximum saturation −6 dB.

CHARACTERISTICS (continued)

Collector voltage of output transistor at $P_{tot\ max}$ = 100 mW	V_{7-16}	<	20	V
Control voltage amplifier input				
Reference voltage	V_{12-16}	typ.	7	V
Control voltage	V_{12-15}	typ.	V_{12-16}-1,5	V
Input impedance	$\|Z_{15-16}\|$	>	500	kΩ
Linearization for saturation input				
Linear part of control curve	V_{10-16}		1,75 to 4	V
Threshold voltage for 50 dB suppression	V_{10-16}	>	1,6	V
		typ.	1,75	V
Adjustment voltage behaviour for higher chrominance output voltage		positive-going		
Input impedance	$\|Z_{9-16}\|$	typ.	10	kΩ
Colour killer input at pin 15				
Input voltage for : colour on	V_{15-16}	<	5,7	V
for : colour off	V_{15-16}	>	6,0	V
Signal suppression at colour off		>	50	dB
Colour killer output				
Switching voltage for : colour on	V_{11-16}	typ.	V_{1-16}	V
for : colour off	V_{11-16}	<	0,5	V
Internal resistance	R_i	typ.	10	kΩ
Collector current of output transistor	I_{11}	<	10	mA
Burst gating and blanking pulse				
Burst gating and blanking pulse (positive or negative)	$\pm V_{9-16}$		1 to 4	V
Input impedance	$\|Z_{9-16}\|$	typ.	1	kΩ
Colour killer				
Colour unkill delay; depends on C_d (see circuit on page 5)	t_d	typ.	24	ms/μF

APPLICATION INFORMATION



COLOUR DEMODULATOR COMBINATION

The TDA2520 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

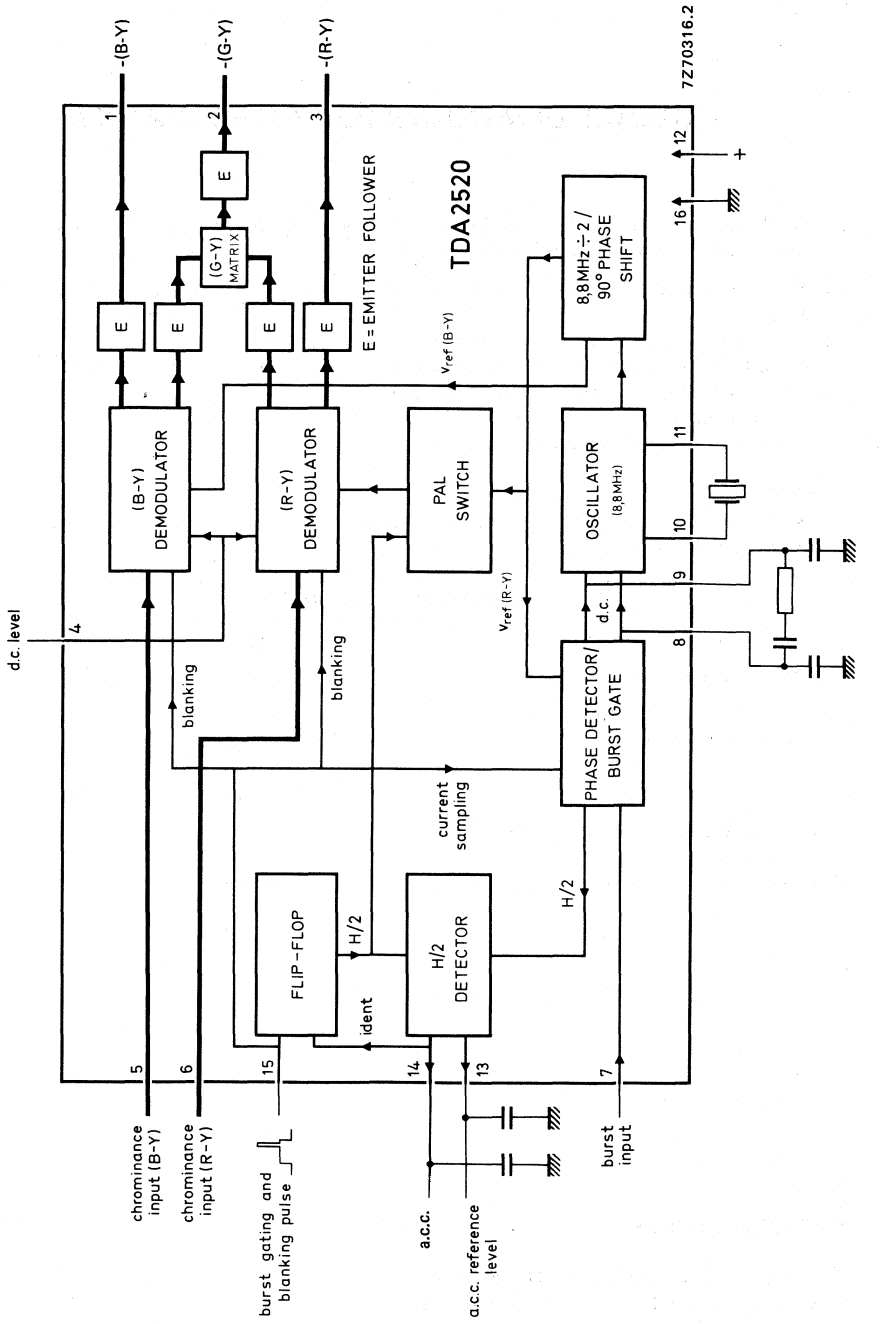
- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a stage to obtain chrominance signal control (a.c.c.) and an a.c.c. reference level
- a colour killer and identification signal detector
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch
- PAL flip-flop
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier-signals at the outputs.

QUICK REFERENCE DATA					
Supply voltage		V_{12-16}	typ.	12	V
Supply current		I_{12}	typ.	40	mA
Colour difference output signals peak-to-peak values	-(R-Y)	$V_{3-16(p-p)}$	>	2,4	V
	-(G-Y)	$V_{2-16(p-p)}$	>	1,35	V
	-(B-Y)	$V_{1-16(p-p)}$	>	3	V
Impedance of colour difference signal outputs			typ.	250	Ω

PACKAGE OUTLINES

TDA2520 : 16-lead DIL ; plastic (SOT-38).
TDA2520Q: 16-lead QIL ; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage					
Supply voltage		V_{12-16}	max.	14	V
Power dissipation					
Total power dissipation		P_{tot}	max.	600	mW
Temperatures					
Storage temperature		T_{stg}		−20 to +125	°C
Operating ambient temperature		T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{12-16} = 12 V; T_{amb} = 25 °C

Demodulator part

Ratio of demodulated signals					
	B-Y/R-Y:	$\frac{V_{1-16}}{V_{3-16}}$	typ.	1,78	
	G-Y/R-Y:	$\frac{V_{2-16}}{V_{3-16}}$	typ.	0,85	1)
	G-Y/R-Y:	$\frac{V_{2-16}}{V_{3-16}}$	typ.	0,17	2)
Colour difference output signals 3)					
peak-to-peak values	−(R-Y)	$V_{3-16(p-p)}$	>	2,4	V
	−(G-Y)	$V_{2-16(p-p)}$	>	1,35	V
	−(B-Y)	$V_{1-16(p-p)}$	>	3	V
Impedance of colour difference signal outputs		$\lvert Z_{3-16}\rvert$	typ.	250	Ω
		$\lvert Z_{2-16}\rvert$	typ.	250	Ω
		$\lvert Z_{1-16}\rvert$	typ.	250	Ω
H/2 ripple at R-Y output (peak-to-peak value)			<	10	mV
Blanking and keying pulse					
burst keying: active for		V_{15-16}	>	7,5	V
inactive for		V_{15-16}	<	6,5	V
blanking: active for		V_{15-16}	>	2	V
inactive for		V_{15-16}	<	1	V

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) The d.c. level of the colour difference outputs can be adjusted from 6 to 10 V at pin 4.

CHARACTERISTICS (continued)

Reference part

Colour burst (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	0,5 V
Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency		<	±5°
Overall holding range with typical crystal	Δf	typ.	±500 Hz
A.C.C. reference output voltage	V_{13-16}	typ.	7 V
A.C.C. voltage at 0,5 V peak-to-peak burst			
at correct phase	V_{14-16}	typ.	5,5 V
with zero burst	V_{14-16}	typ.	7,0 V
Oscillator input resistance	R_{11-16}	typ.	270 Ω
Oscillator input capacitance	C_{11-16}	see note	
Oscillator output resistance	R_{10-16}	typ.	200 Ω

Note : to be established.

COLOUR DEMODULATOR COMBINATION

The TDA2522 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

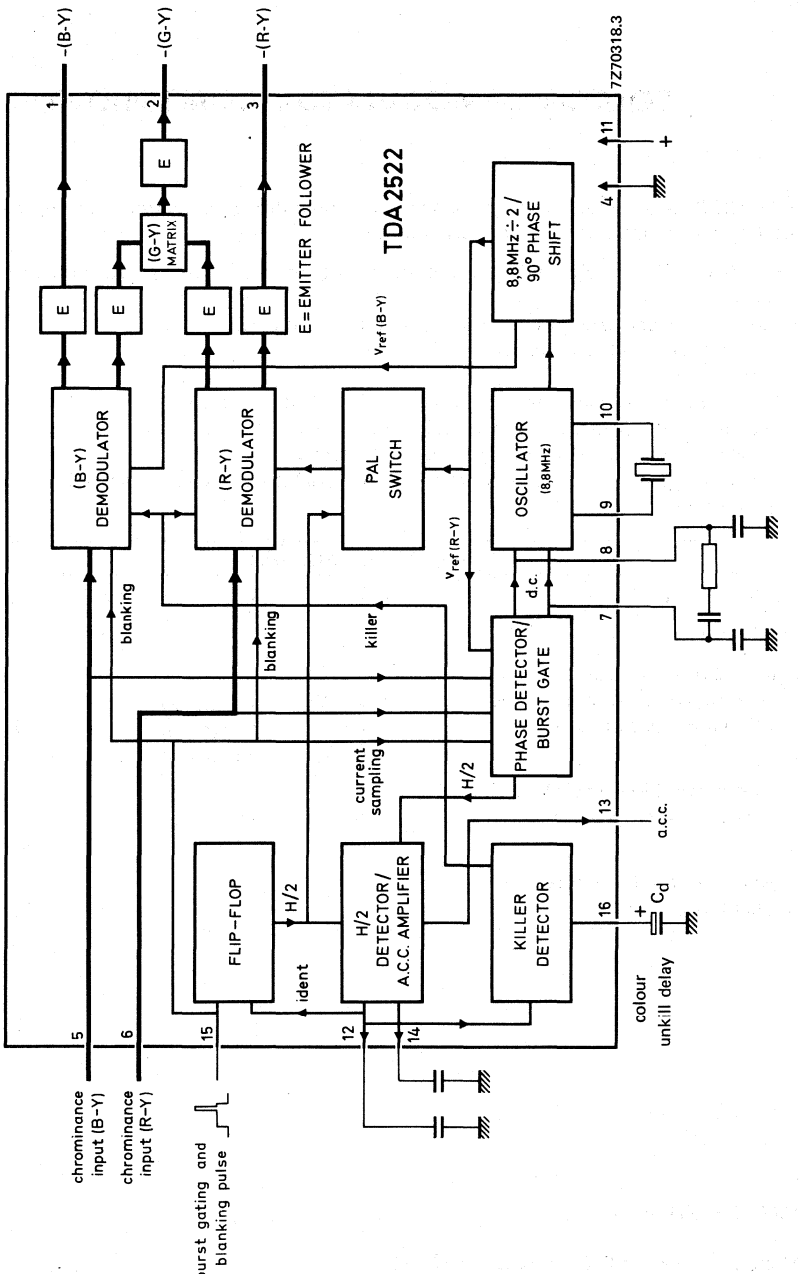
- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a.c.c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

QUICK REFERENCE DATA					
Supply voltage		V_{11-4}	typ.	12	V
Supply current		I_{11}	typ.	40	mA
Colour difference output signals peak-to-peak values; for the following input signals	-(R-Y)	$V_{3-4(p-p)}$	>	2,4	V
	-(G-Y)	$V_{2-4(p-p)}$	>	1,35	V
	-(B-Y)	$V_{1-4(p-p)}$	>	3	V
Chrominance input signal (including burst) peak-to-peak value	R-Y	$V_{6-4(p-p)}$		500	mV
	B-Y	$V_{5-4(p-p)}$		350	mV
Impedance of colour difference signal outputs			typ.	250	Ω

PACKAGE OUTLINES

TDA2522 : 16-lead DIL ; plastic (SOT-38).
TDA2522Q: 16-lead QIL ; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-4}	max.	14	V
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature	T_{stg}	−20 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +60		°C

CHARACTERISTICS at V_{11-4} = 12 V; T_{amb} = 25 °C

Demodulator part

Ratio of demodulated signals					
	B-Y/R-Y:	$\frac{V_{1-4}}{V_{3-4}}$	typ.	1,78	
	G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,85	1)
	G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,17	2)
Colour difference output signals					
peak-to-peak values; for the following input signals	−(R-Y)	$V_{3-4(p-p)}$	>	2,4	V
	−(G-Y)	$V_{2-4(p-p)}$	>	1,35	V
	−(B-Y)	$V_{1-4(p-p)}$	>	3	V
Chrominance input signal (including burst) peak-to-peak value; note 3	R-Y	$V_{6-4(p-p)}$		500	mV
	B-Y	$V_{5-4(p-p)}$		350	mV
Impedance of colour difference signal outputs		$\lvert Z_{3-4}\rvert$	typ.	250	Ω
		$\lvert Z_{2-4}\rvert$	typ.	250	Ω
		$\lvert Z_{1-4}\rvert$	typ.	250	Ω
H/2 ripple at R-Y output (peak-to-peak value)			<	10	mV
Blanking and keying pulse					
burst keying: active for		V_{15-4}	>	7,5	V
inactive for		V_{15-4}	<	6,5	V
blanking: active for		V_{15-4}	>	2	V
inactive for		V_{15-4}	<	1	V

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) Colour bar with 75% saturation.

CHARACTERISTICS (continued)

Reference part

Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency		<	±5°		
Overall holding range with typical crystal	Δf	typ.	±500	Hz	
Burst signal input at keying pulse width of 4 µs (peak-to-peak value)	$V_{5-6(p-p)}$	typ.	0,25	V	1)
Oscillator input resistance	R_{10-4}	typ.	270	Ω	
Oscillator input capacitance	C_{10-4}	typ.	note 2	pF	
Oscillator output resistance	R_{9-4}	typ.	200	Ω	
A.C.C. reference voltage	V_{12-4}	typ.	7	V	
A.C.C. voltage at 0,25 V peak-to-peak burst					
at correct phase:	V_{14-4}	typ.	5,5	V	
with zero burst:	V_{14-4}	typ.	7,0	V	
A.C.C. amplifier output voltage range at $\pm I_{13} < 200$ µA	V_{13-4}		0,5 to 5	V	

Colour killer

Via pin 14					
Colour off	V_{14-4}	>	6	V	
Colour on	V_{14-4}	<	5,6	V	
Alternatively via pin 16					
Colour off	V_{16-4}	>	7	V	
Colour on	V_{16-4}	<	5	V	
Colour unkill delay	t_d	typ.	20	ms/µF	3)

1) The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

2) To be established.

3) The delay depends on the value of C_d.

COLOUR DEMODULATOR COMBINATION

The TDA2523 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions:

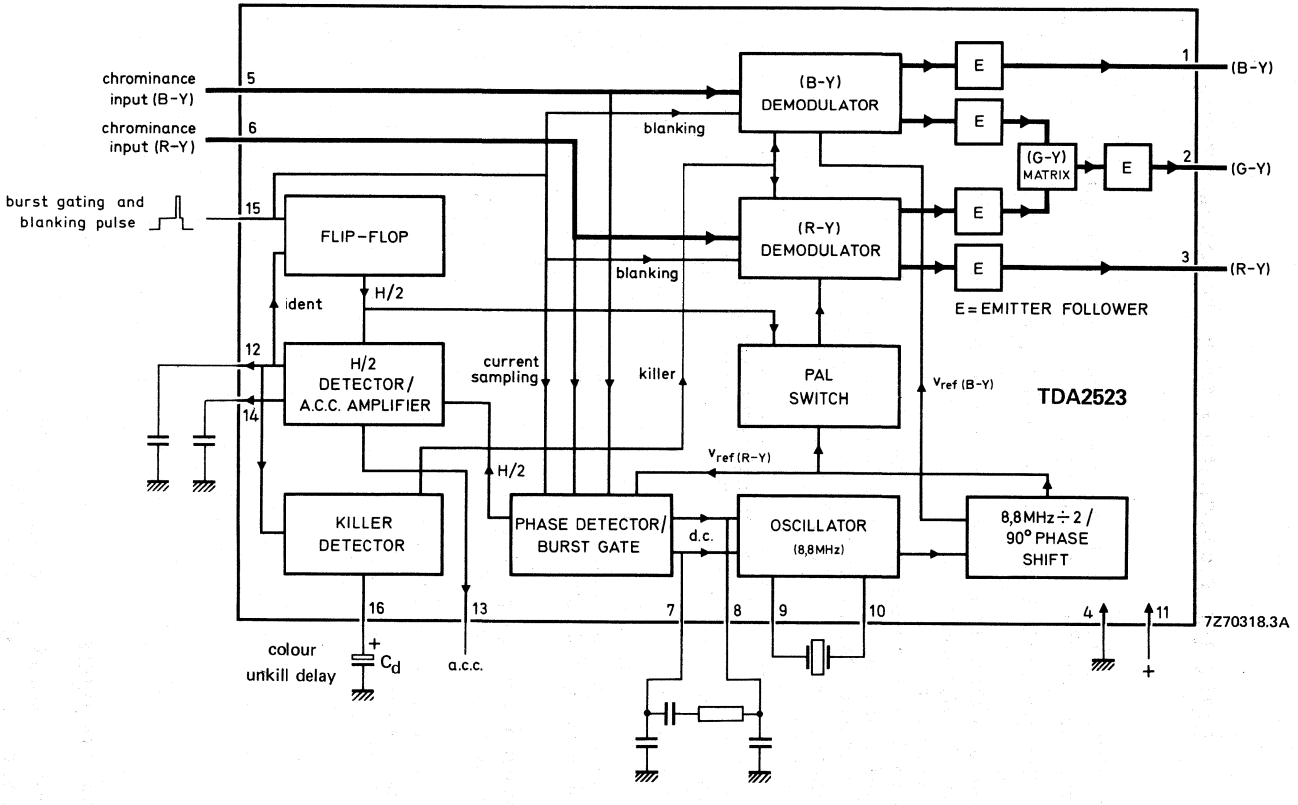
- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a.c.c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

QUICK REFERENCE DATA					
Supply voltage		V_{11-4}	typ.	12	V
Supply current		I_{11}	typ.	40	mA
Colour difference output signals peak-to-peak values; for the following input signals	(R-Y)	$V_{3-4(p-p)}$	>	2,4	V
	(G-Y)	$V_{2-4(p-p)}$	>	1,35	V
	(B-Y)	$V_{1-4(p-p)}$	>	3	V
Chrominance input signal (including burst) peak-to-peak value	R-Y	$V_{6-4(p-p)}$		500	mV
	B-Y	$V_{5-4(p-p)}$		350	mV
Impedance of colour difference signal outputs			typ.	250	Ω

PACKAGE OUTLINES

TDA2523 : 16-lead DIL ; plastic (SOT-38).
TDA2523Q: 16-lead QIL ; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-4}	max.	14	V
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature	T_{stg}		−20 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_{11-4} = 12 V; T_{amb} = 25 °C

Demodulator part

Ratio of demodulated signals					
	B-Y/R-Y:	$\frac{V_{1-4}}{V_{3-4}}$	typ.	1,78	
	G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,85	1)
	G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,17	2)
Colour difference output signals peak-to-peak values; for the following input signals	(R-Y)	$V_{3-4(p-p)}$	>	2,4	V
	(G-Y)	$V_{2-4(p-p)}$	>	1,35	V
	(B-Y)	$V_{1-4(p-p)}$	>	3	V
Chrominance input signal (including burst) peak-to-peak value; note 3	R-Y	$V_{6-4(p-p)}$		500	mV
	B-Y	$V_{5-4(p-p)}$		350	mV
Impedance of colour difference signal outputs		$\lvert Z_{3-4}\rvert$	typ.	250	Ω
		$\lvert Z_{2-4}\rvert$	typ.	250	Ω
		$\lvert Z_{1-4}\rvert$	typ.	250	Ω
H/2 ripple at R-Y output (peak-to-peak value)			<	10	mV
Blanking and keying pulse					
burst keying: active for		V_{15-4}	>	7,5	V
inactive for		V_{15-4}	<	6,5	V
blanking: active for		V_{15-4}	>	2	V
inactive for		V_{15-4}	<	1	V

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) Colour bar with 75% saturation.

CHARACTERISTICS (continued)

Reference part

Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency		<	±5°		
Overall holding range with typical crystal	Δf	typ.	±500	Hz	
Burst signal input at keying pulse width of 4 µs (peak-to-peak value)	$V_{5-6(p-p)}$	typ.	0,25	V	1)
Oscillator input resistance	R_{10-4}	typ.	270	Ω	
Oscillator input capacitance	C_{10-4}	typ.	note 2	pF	
Oscillator output resistance	R_{9-4}	typ.	200	Ω	
A.C.C. reference voltage	V_{12-4}	typ.	7	V	
A.C.C. voltage at 0,25 V peak-to-peak burst					
at correct phase:	V_{14-4}	typ.	5,5	V	
with zero burst:	V_{14-4}	typ.	7,0	V	
A.C.C. amplifier output voltage range at $\pm I_{13} < 200$ µA	V_{13-4}		0,5 to 5	V	

Colour killer

Via pin 14					
Colour off	V_{14-4}	>	6	V	
Colour on	V_{14-4}	<	5,6	V	
Alternatively via pin 16					
Colour off	V_{16-4}	>	7	V	
Colour on	V_{16-4}	<	5	V	
Colour unkill delay	t_d	typ.	20	ms/µF	3)

1) The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

2) To be established.

3) The delay depends on the value of C_d.

RGB MATRIX PREAMPLIFIER

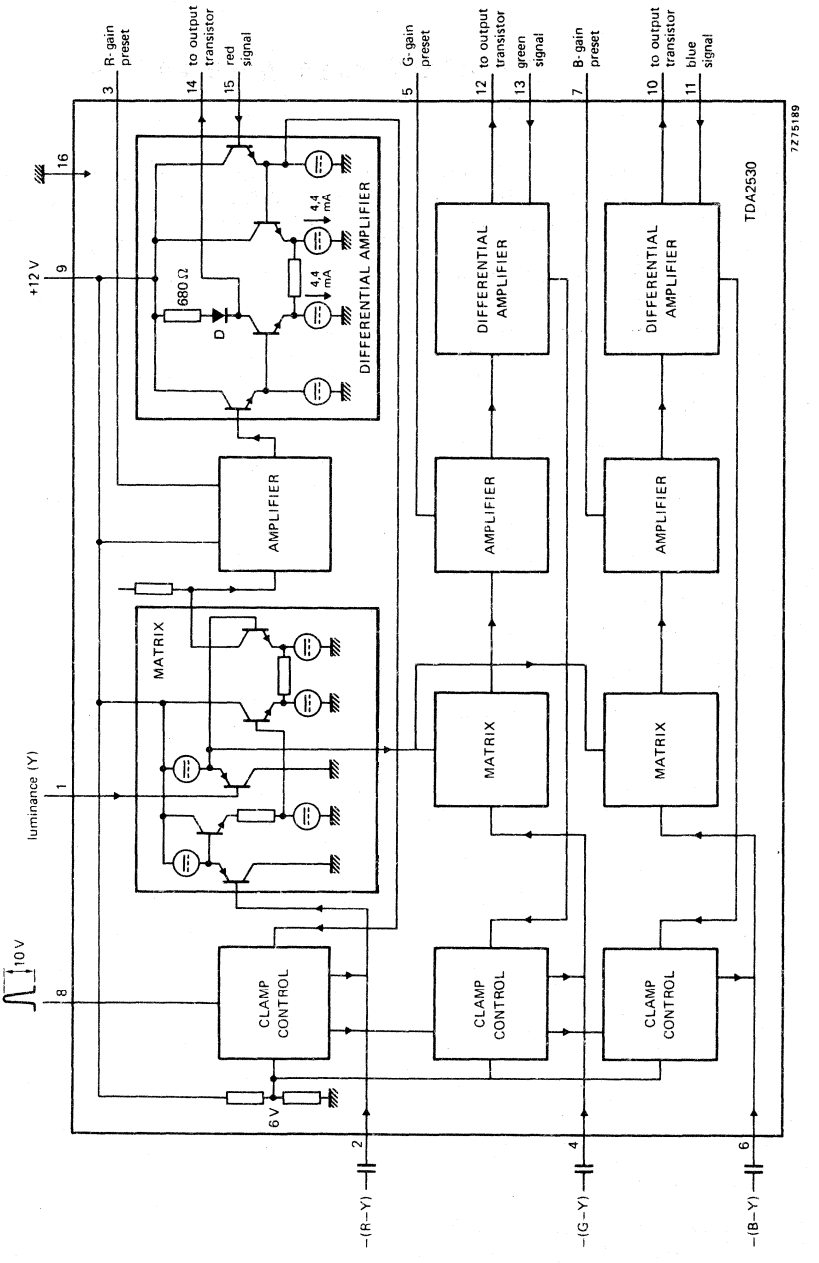
The TDA2530 is an integrated RGB matrix preamplifier for colour television receivers, incorporating a matrix preamplifier for RGB cathode drive of the picture tube with clamping circuits. The three channels have the same layout to ensure identical frequency behaviour.
This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

QUICK REFERENCE DATA			
Supply voltage	V_{9-16}	typ.	12 V
Operating ambient temperature range	T_{amb}		−20 to +60 °C
Luminance input resistance	R_{1-16}	>	100 kΩ
Input current of colour difference inputs	I_2, I_4, I_6	typ.	2 μA
during clamping	I_2, I_4, I_6		−0,2 to +0,2 mA
Clamping pulse input current	$-I_8$	<	20 μA
Gain of RGB preamplifiers	G	typ.	0 dB
Gain d.c. adjustment range	ΔG	typ.	±3 dB
Gain of error amplifier (conductance)		typ.	20 mA/V
Input current of feedback inputs	I_{11}, I_{13}, I_{15}	typ.	2 μA
Output current swing	I_{10}, I_{12}, I_{14}		−4,4 to +4,4 mA

PACKAGE OUTLINES

TDA2530 : 16-lead DIL; plastic (SOT-38).
TDA2530Q : 16-lead QIL; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage (pin 9)	V_P (V_{9-16})	max.	15 V
Pin 1	V_{1-16}		0 to V_P
Pins 3, 5 and 7	$V_{3;5;7-16}$		0 to V_P
Pins 2, 4 and 6	$V_{2;4;6-16}$		0 to V_P
Pin 8	V_{8-16}	max.	V_P
Pin 10	V_{10-16}	V_{11-16}	to V_P + 3 V
Pin 12	V_{12-16}	V_{13-16}	to V_P + 3 V
Pin 14	V_{14-16}	V_{15-16}	to V_P + 3 V
Pins 11, 13 and 15	$V_{11;13;15-16}$		0,3 V_P to V_P

Current

Pin 8	$-I_8$	max.	1 mA

Power dissipation

Total power dissipation	P_{tot}	max.	1 W

Temperatures

Storage temperature	T_{stg}	−20 to +125 °C
Operating ambient temperature	T_{amb}	−20 to +60 °C

CHARACTERISTICS at V_P = 12 V; V_{1-16} = 1,5 V; T_{amb} = 25 °C; measured in circuit on page 5.

Current consumption	I_9	typ.	50 mA
Luminance input			
Black level	V_{1-16}	typ.	1,5 V
Black-to-white input voltage (peak-to-peak value)	$V_{1-16(p-p)}$	typ.	1,0 V
Input resistance	R_{1-16}	>	100 kΩ
Colour difference input			
Input signals (peak-to-peak values) R-Y [1]	$V_{2-16(p-p)}$	typ.	1,4 V
G-Y [1]	$V_{4-16(p-p)}$	typ.	0,82 V
B-Y [1]	$V_{6-16(p-p)}$	typ.	1,78 V
Input currents (source resistance 300 Ω max.)	I_2, I_4, I_6	typ.	2 μA
		<	4 μA
Input currents during clamping	I_2, I_4, I_6		−0,2 to +0,2 mA

[1]) This prescribed order is not mandatory, as all three channels are identical.

CHARACTERISTICS (continued)

Clamp pulse input for d.c. feedback

Input voltage for clamping: on level	V_{8-16}		6,5 to 12	V
off level	V_{8-16}		0 to 5,5	V [1]
Input current for clamping: on level	I_8	<	1	μA
off level	$-I_8$	<	20	μA

Feedback input

D.C. level during clamping	$V_{11;13;15-16}$	typ.	0,5 V_P	

Gain adjustment for colour drive

Adjustment voltage range	$V_{3;5;7-16}$		0 to 10	V
Adjustment voltage for nominal gain	$V_{3;5;7-16}$	typ.	5	V
Nominal gain between colour difference inputs, luminance input and colour feedback inputs (pins 11, 13 and 15)	G	typ.	0	dB [2]
Adjustment range of nominal gain at $\Delta V_{3;5;7-16} = \pm 5$ V	ΔG	>	±3	dB

Differential amplifier

Input current of feedback inputs	I_{11}, I_{13}, I_{15}	typ.	2	μA
Gain of error amplifier (conductance)		typ.	20	mA/V
Output current swing	I_{10}, I_{12}, I_{14}		−4,4 to +4,4	mA
Integrated load resistance	$R_{10;12;14-9}$	typ.	680	Ω [3]
Output bias voltage (see application information)	$V_{10;12;14-16}$	typ.	8	V [3]

APPLICATION INFORMATION (see circuit on page 5)

Clamping level (V_{cl}) of video output stages, with set clamping level potentiometers in their mid-positions:

$$V_{cl} = V_P \left(1 + \frac{R1}{R2} - \frac{R1}{R3}\right)$$

Gain of video output stages: $G = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4}$

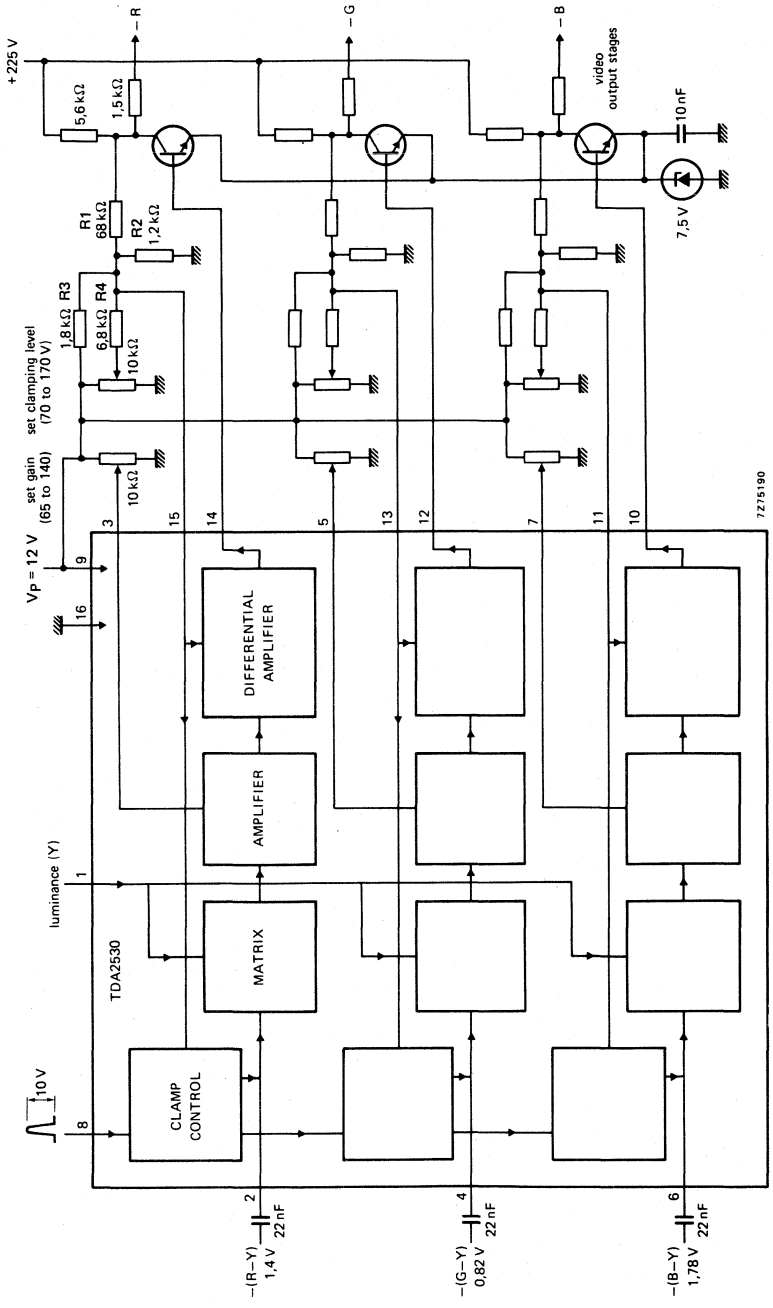
---

[1]) Switching from clamping on to off occurs at about 6 V.

[2]) Error signal is assumed to be negligible.

[3]) The fact that the load resistors have series diodes (D; see block diagram on page 2), means that the resistors can be ignored when $V_{10;12;14} \geq V_P$.
In that case, external load resistors must be chosen such that the nominal current will be 4,4 mA.

APPLICATION INFORMATION



RGB MATRIX PREAMPLIFIER

The TDA2532 is an integrated matrix preamplifier for use in conjunction with discrete video amplifiers to provide RGB drive to the cathodes of a colour television picture tube. The integrated circuit incorporates:

- matrix circuits;
- gain control stages, operated by d.c. setting;
- preamplifiers with feedback and integral black-level clamps;
- facilities for video blanking during data display.

The three channels have the same layout to ensure identical frequency behaviour. The integrated circuit has been designed to be driven by the integrated colour demodulator combination type TDA2522.

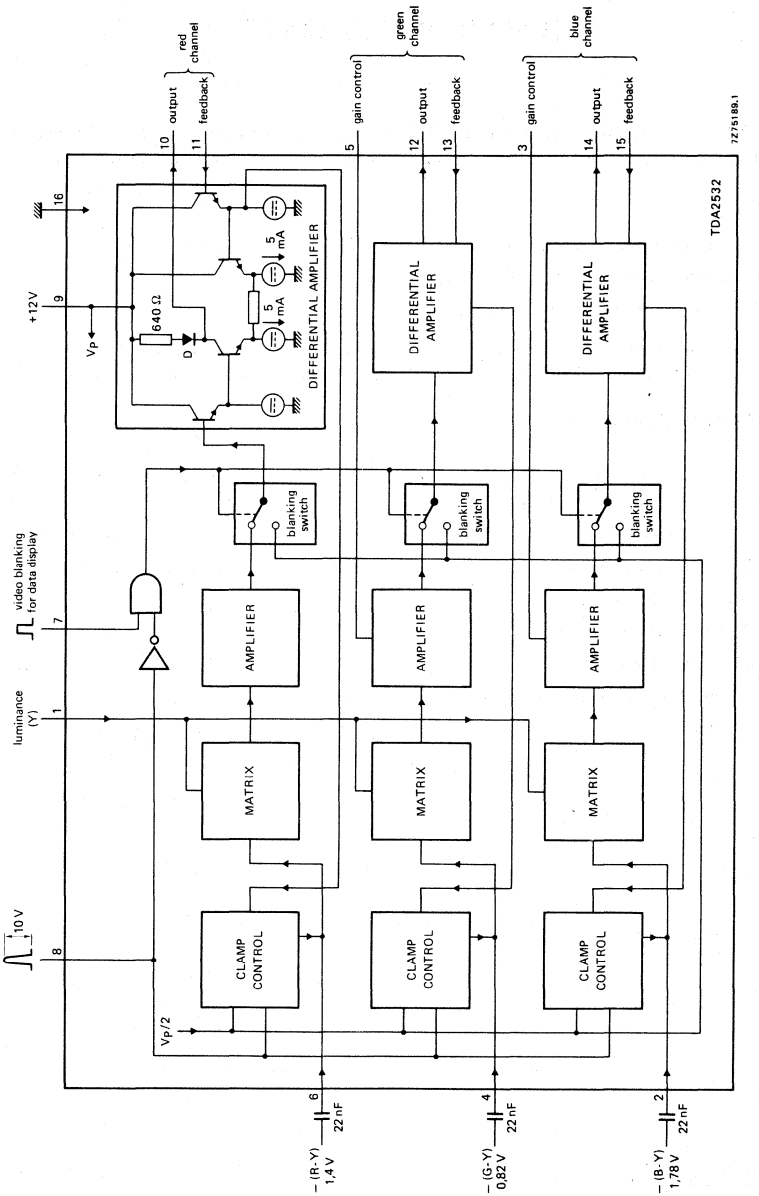
QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12	V
Operating ambient temperature range	T_{amb}		−25 to + 60	°C
Luminance input resistance	$R_{1\text{-}16}$	>	100	kΩ
Input current of colour difference inputs	I_2, I_4, I_6	typ.	1	μA
Clamping pulse input current	$-I_8$	<	60	μA
Gain of RGB preamplifiers	G	typ.	0	dB
Gain d.c. adjustment range	ΔG	>	± 40	%
Gain of error amplifier (transconductance)		typ.	20	mA/V
Output current swing	I_{10},I_{12}, I_{14}	typ.	± 3,5	mA

PACKAGE OUTLINES

TDA2532: 16-lead DIL; plastic (SOT-38).
TDA2532Q: 16-lead QIL; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P (V9-16)	max.	13,2 V
Pin 1	V_{1-16}		0 to V_P
Pins 3, 5	$V_{3;\,5-16}$		0 to V_P
Pins 2, 4 and 6	$V_{2;\,4;\,6-16}$		0 to V_P
Pin 7	V_{7-16}		−0,5 V to V_P
Pin 8	V_{8-16}	max.	V_P
Pin 10	V_{10-16}		V_{11-16} to V_P + 3 V
Pin 12	V_{12-16}		V_{13-16} to V_P + 3 V
Pin 14	V_{14-16}		V_{15-16} to V_P + 3 V
Pins 11, 13 and 15	$V_{11;\,13;\,15-16}$		0,3 V_P to V_P
Pin 8	$-I_8$	max.	1 mA
Total power dissipation	P_{tot}	max.	1,1 W
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 60 °C

CHARACTERISTICS

At V_P = 12 V; V_{1-16} = 1,5 V; T_{amb} = 25 °C; measured in circuit on page 6.

Current consumption	I_9	typ.	60 mA
Luminance input			
Black level	V_{1-16}	typ.	1,5 V
Black-to-white input voltage (peak-to-peak value)	$V_{1-16\,(p-p)}$	typ.	1,0 V
Input resistance	R_{1-16}	>	100 kΩ
Colour difference input			
Input signals (peak-to-peak values) R-Y	$V_{6-16\,(p-p)}$	typ.	1,4 V
for 100% saturated colour bars G-Y	$V_{4-16\,(p-p)}$	typ.	0,82 V
B-Y	$V_{2-16\,(p-p)}$	typ.	1,78 V
Input currents (source resistance 300 Ω max.)	I_2, I_4, I_6	typ.	1 μA
		<	3 μA

CHARACTERISTICS (continued)

Clamp pulse input			
Input voltage for clamping			
on level	$V_{8\text{-}16}$		7,5 to 12 V
off level	$V_{8\text{-}16}$		0 to 6,5 V*
Input voltage to enable video blanking input	$V_{8\text{-}16}$	<	1 V
Input voltage to disable video blanking input	$V_{8\text{-}16}$		2 to 12 V
Input current for clamping			
on level	I_8	<	1 μA
off level	$-I_8$	<	60 μA
Clamp pulse duration	t_{clamp}	>	3,5 μs
Video blanking input			
Input voltage for blanking			
on level	$V_{7\text{-}16}$	>	1,5 V
off level	$V_{7\text{-}16}$	<	0,5 V
Feedback input			
D.C. level during clamping	$V_{11;\ 13;\ 15\text{-}16}$		6 to 6,2 V
Gain adjustment for colour drive			
Adjustment voltage range	$V_{3;\ 5\text{-}16}$		0 to 10 V
Adjustment voltage for nominal gain	$V_{3;\ 5\text{-}16}$	typ.	5 V
Nominal gain between colour difference inputs, luminance input and colour feedback inputs (pins 11, 13 and 15)	G	typ.	0 dB**
Adjustment range of nominal gain at $\Delta V_{3;\ 5\text{-}16} = \pm 5$ V	ΔG	>	± 40 %
Differential amplifier			
Gain of error amplifier (transconductance)		typ.	20 mA/V
Output current swing	I_{10}, I_{12}, I_{14}	⩾	± 3,5 mA
Integrated load resistance	$R_{10;\ 12;\ 14\text{-}9}$	typ.	640 Ω▲
Output bias voltage (see application information)	$V_{10;\ 12;\ 14\text{-}16}$	typ.	8 V▲

* Switching from clamping on to off occurs at about 7 V.

** Error signal is assumed to be negligible.

▲ The fact that the load resistors have series diodes (D; see block diagram on page 2), means that the resistors can be ignored when $V_{10;\ 12;\ 14} \geqslant V_P$. In that case, external load resistors must be chosen such that the nominal current will be 3,5 mA.

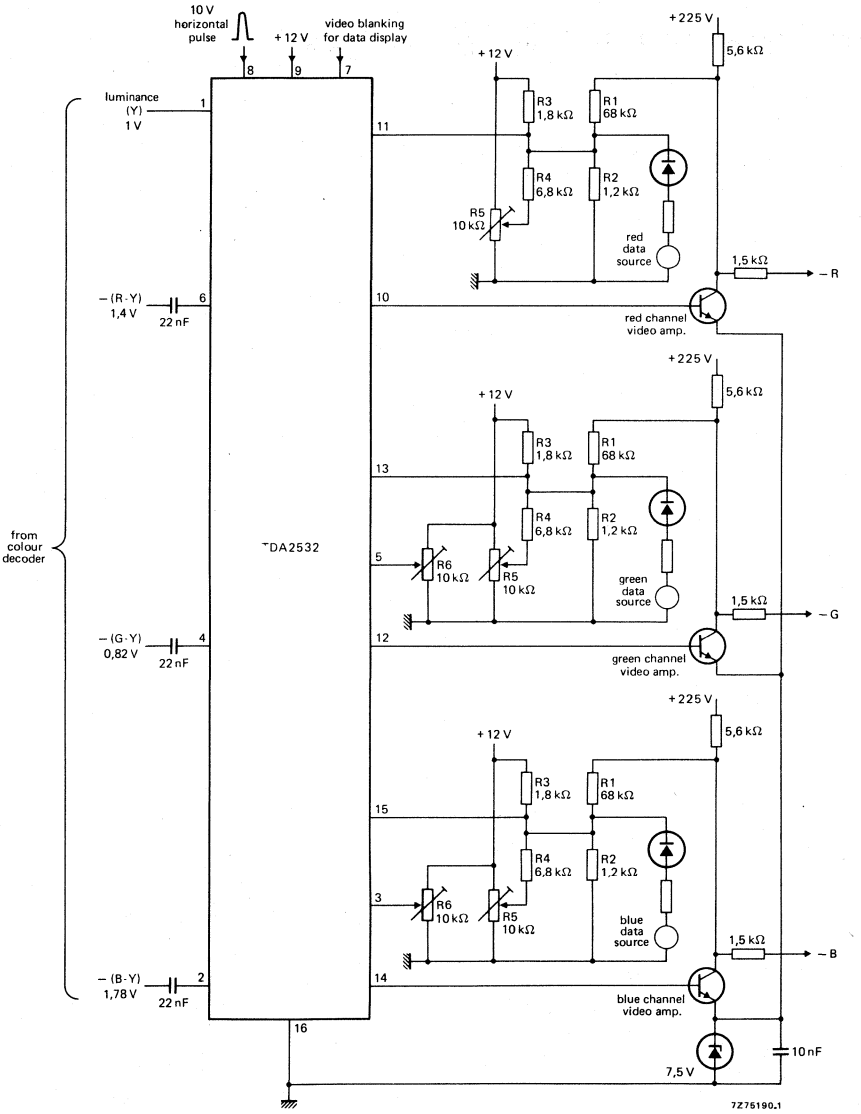
APPLICATION INFORMATION (see circuit on page 6)

Clamping level (V_{cl}) of video output stages, with set clamping level potentiometers in their mid-positions:

$$V_{cl} = 0{,}5\ V_P\ (1 + \frac{R1}{R2} - \frac{R1}{R3}).$$

Gain of video output stages: $G = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4 + 0{,}25\ R5}$.

APPLICATION INFORMATION



R5 = clamping level adjustment (70 V to 170 V); R6 = gain adjustment (65 to 140).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input voltage at f = 38,9 MHz (r.m.s. value)	$V_{1\text{-}16\ (rms)}$	typ.	100 μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,7 V
I.F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10 V

PACKAGE OUTLINES

TDA2540 : 16-lead DIL; plastic (SOT-38).
TDA2540Q: 16-lead QIL; plastic (SOT-58).

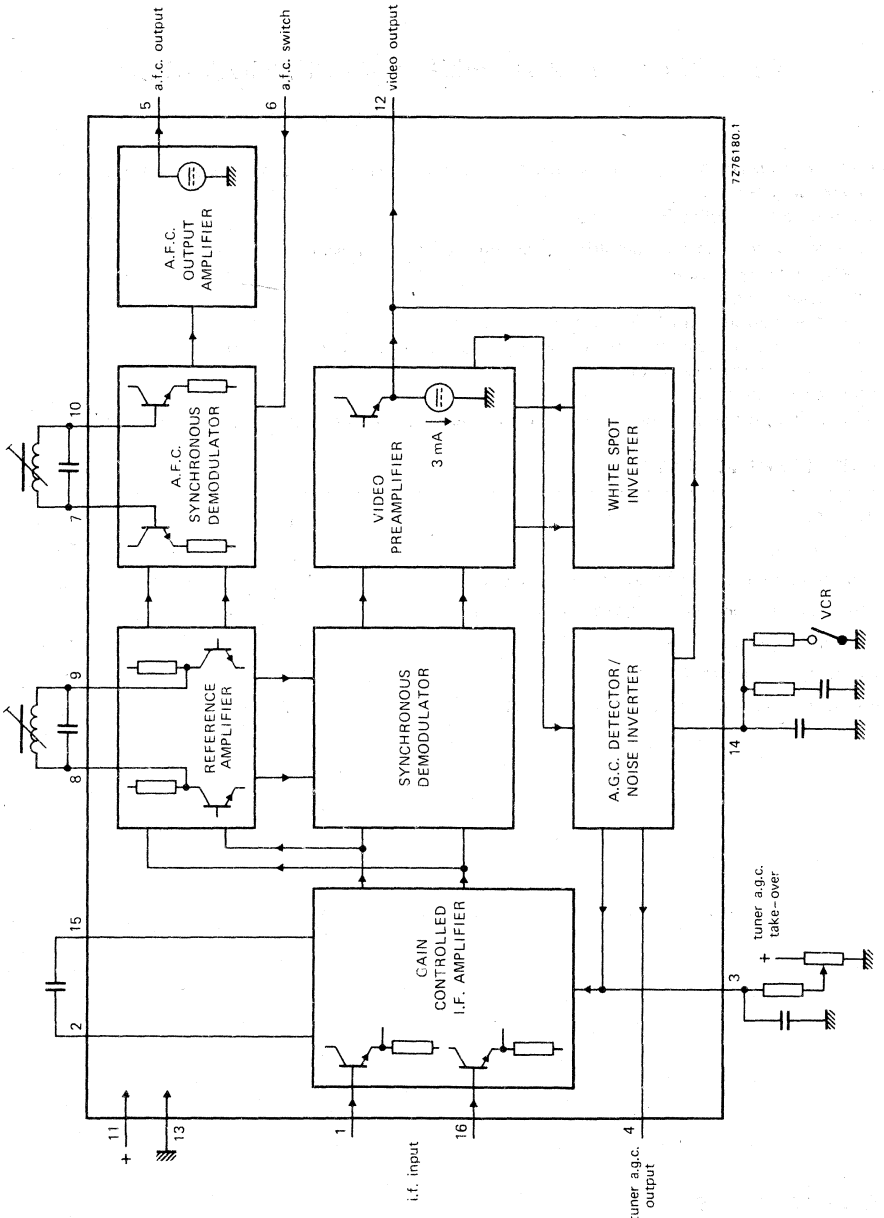


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13,2 V
Tuner a.g.c. voltage	V_{4-13}	max.	12 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 60 °C

CHARACTERISTICS (measured in Fig. 5)

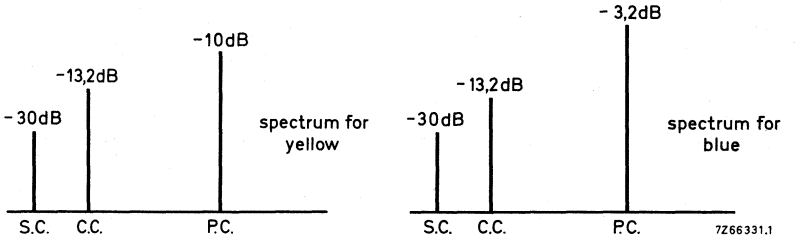
Supply voltage range	V_{11-13}	typ.	12 V 10,2 to 13,2 V
The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V; f = 38,9 MHz			
I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1-16(rms)}$	typ. <	100 μV 150 μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	2 kΩ in parallel with 2 pF
Zero-signal output level	V_{12-13}	typ.	6 ± 0,3 V*
Top sync output level	V_{12-13}	typ.	3,07 V 2,9 to 3,2 V
I.F. voltage gain control range	G_v	typ.	64 dB
Bandwidth of video amplifier (3 dB)	B	typ.	6 MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB**
Differential gain	dG	typ. <	4 % 10 %
Differential phase	$d\varphi$	typ. <	2° 10°

* So-called 'projected zero point', e.g. with switched demodulator.

** $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*	>	46 dB
	typ.	60 dB
yellow*	>	46 dB
	typ.	50 dB
at 3,3 MHz**	>	46 dB
	typ.	54 dB



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

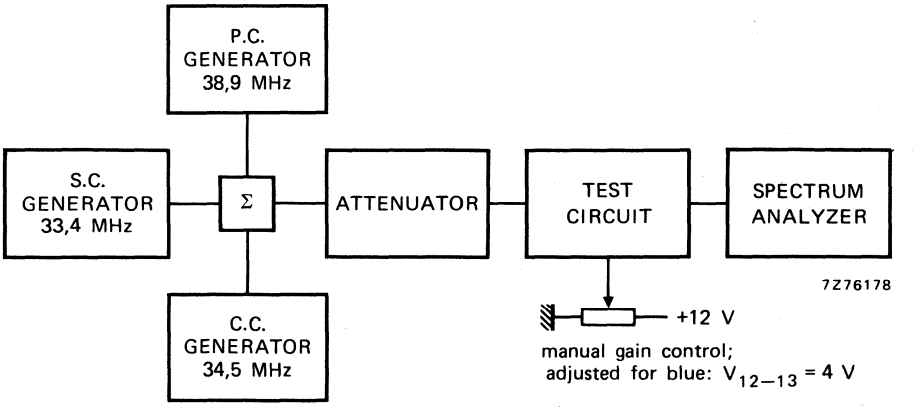


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB. ** $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

Carrier signal at video output		typ.	4 mV
		<	30 mV
2nd harmonic of carrier at video output		typ.	20 mV
		<	30 mV
White spot inverter threshold level (Fig. 4)		typ.	6,6 V
White spot insertion level (Fig. 4)		typ.	4,7 V
Noise inverter threshold level (Fig. 4)		typ.	1,8 V
Noise insertion level (Fig. 4)		typ.	3,8 V
External video switch (VCR) switches off the output at:	V_{14-13}	<	1,1 V

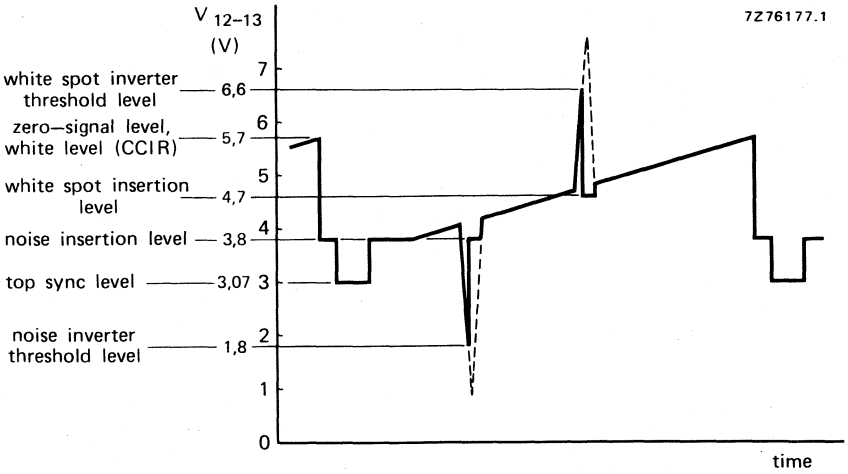


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		10 to 0 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 5 V; V_{4-13} = 12 V	I_4	<	15 μA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	>	10 V
		typ.	11 V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ.	100 kHz
		<	200 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V
			4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3,2 V
A.F.C. switches off at:	V_{6-13}	<	1,5 V

APPLICATION INFORMATION

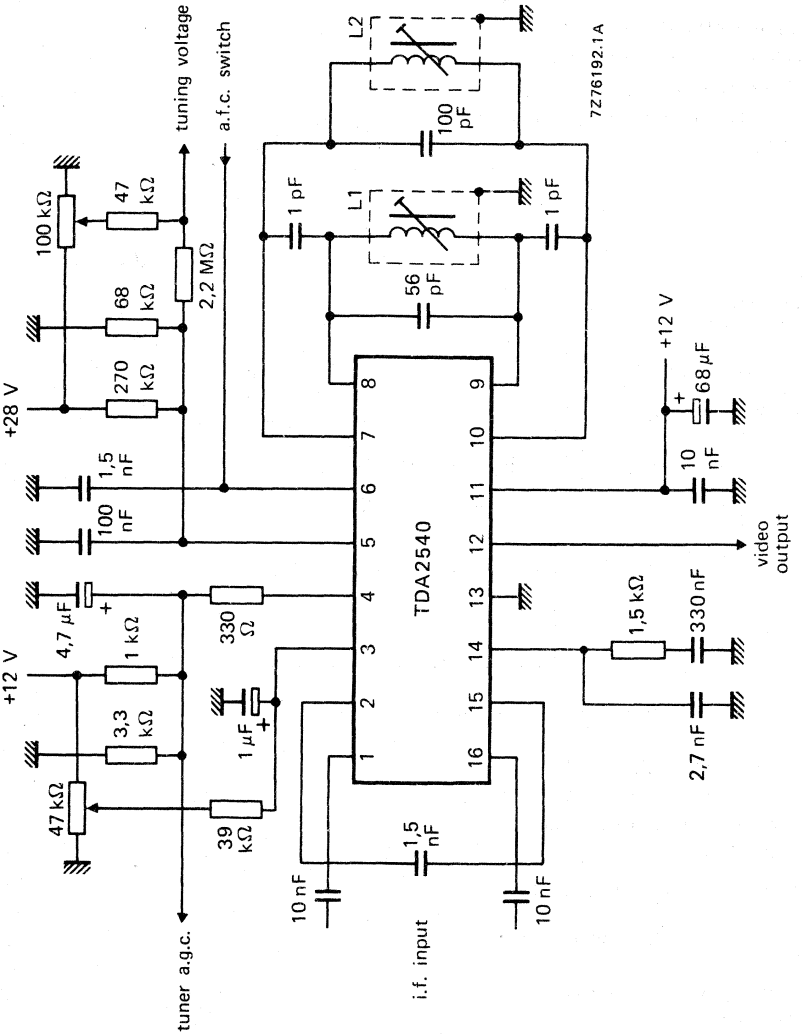


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 38,9 MHz.

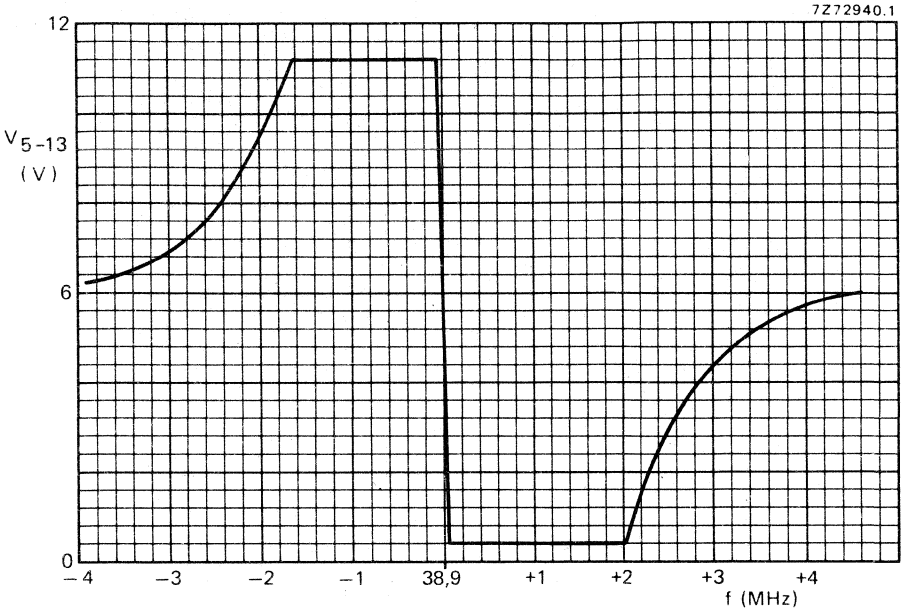


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

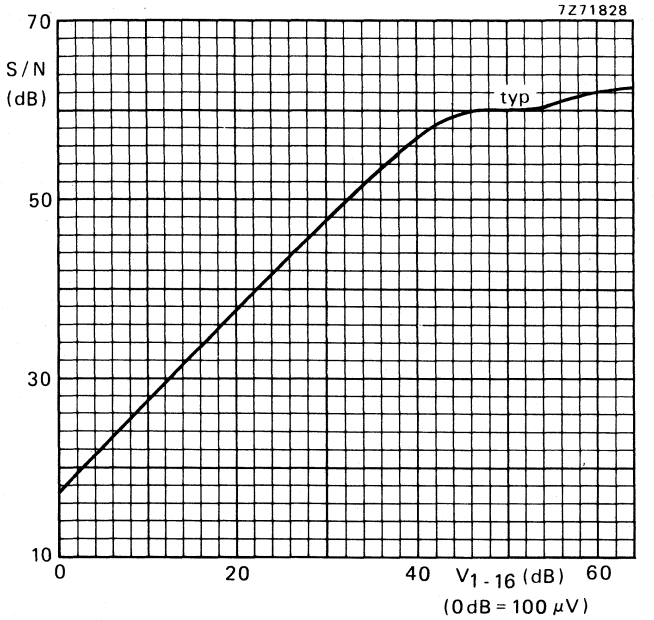


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2541 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

QUICK REFERENCE DATA

Supply voltage	V_{11-13}	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input voltage at f = 38,9 MHz (r.m.s. value)	$V_{1-16(rms)}$	typ.	100 μV
Video output voltage (white at 10% of top sync)	$V_{12(p-p)}$	typ.	2,7 V
I.F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB
A.F.C. output voltage swing for Δf = 100 kHz	ΔV_{5-13}	typ.	10 V

PACKAGE OUTLINES

TDA2541 : 16-lead DIL; plastic (SOT-38).
TDA2541Q: 16-lead QIL; plastic (SOT-58).

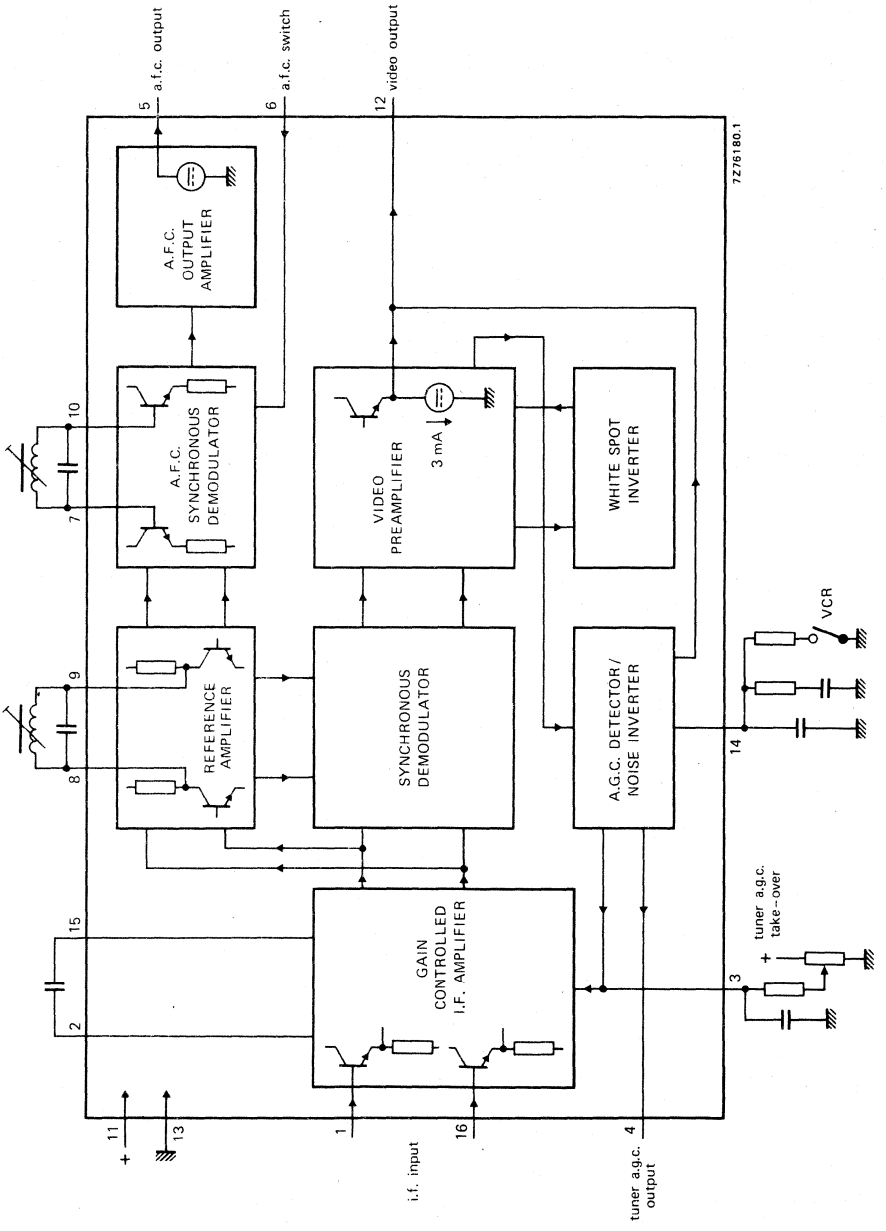


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2 V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 60 °C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ.	12 V
			10,2 to 13,2 V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

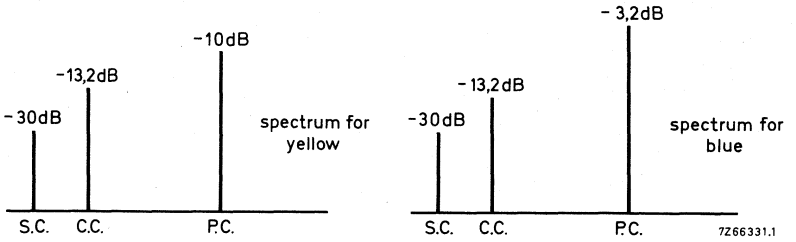
I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100 μV
		<	150 μV
Differential input impedance	$\lvert Z_{1\text{-}16} \rvert$	typ.	2 kΩ in parallel with 2 pF
Zero-signal output level	$V_{12\text{-}13}$	typ.	6 ± 0,3 V*
Top sync output level	$V_{12\text{-}13}$	typ.	3,07 V
			2,9 to 3,2 V
I.F. voltage gain control range	G_v	typ.	64 dB
Bandwidth of video amplifier (3 dB)	B	typ.	6 MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB**
Differential gain	dG	typ.	4 %
		<	10 %
Differential phase	dφ	typ.	2°
		<	10°

* So-called 'projected zero point', e.g. with switched demodulator.

** $$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at B = 5 MHz}}.$$

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*	>	46 dB
	typ.	60 dB
yellow*	>	46 dB
	typ.	50 dB
at 3,3 MHz**	>	46 dB
	typ.	54 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

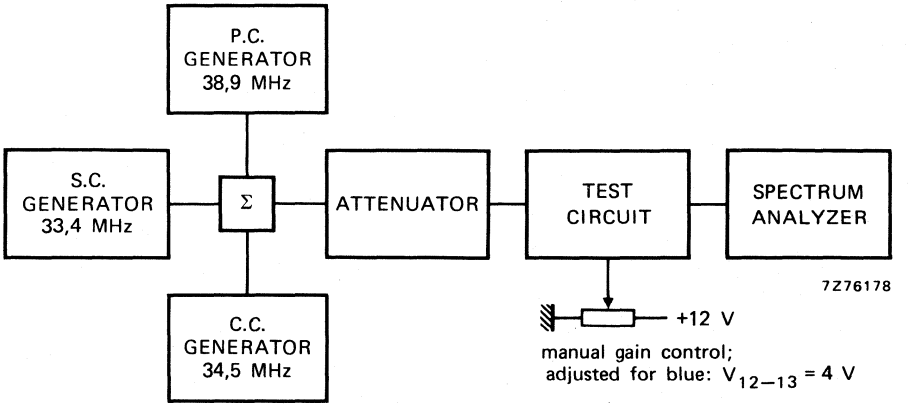


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB.

** $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

Carrier signal at video output		typ.	4 mV
		<	30 mV
2nd harmonic of carrier at video output		typ.	20 mV
		<	30 mV
White spot inverter threshold level (Fig. 4)		typ.	6,6 V
White spot insertion level (Fig. 4)		typ.	4,7 V
Noise inverter threshold level (Fig. 4)		typ.	1,8 V
Noise insertion level (Fig. 4)		typ.	3,8 V
External video switch (VCR) switches off the output at:	V_{14-13}	<	1,1 V

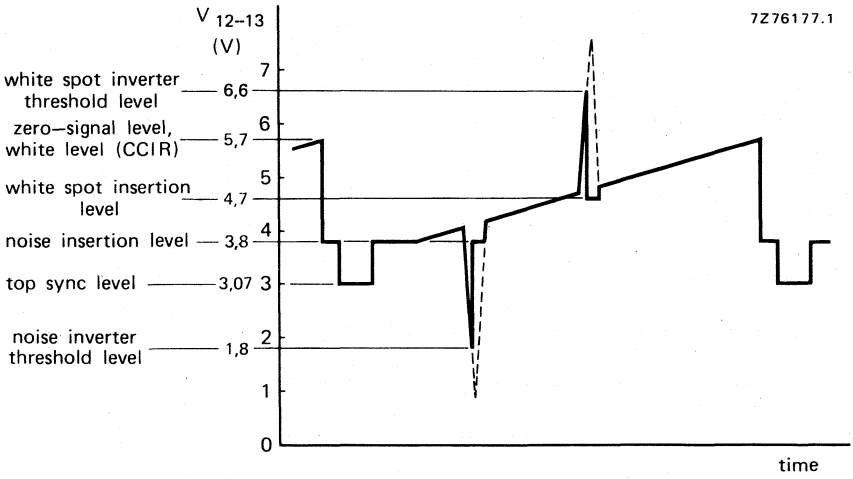


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 10 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 11 V; V_{4-13} = 12 V	I_4	<	15 μA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	>	10 V
		typ.	11 V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ.	100 kHz
		<	200 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V
			4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3,2 V
A.F.C. switches off at:	V_{6-13}	<	1,5 V

APPLICATION INFORMATION

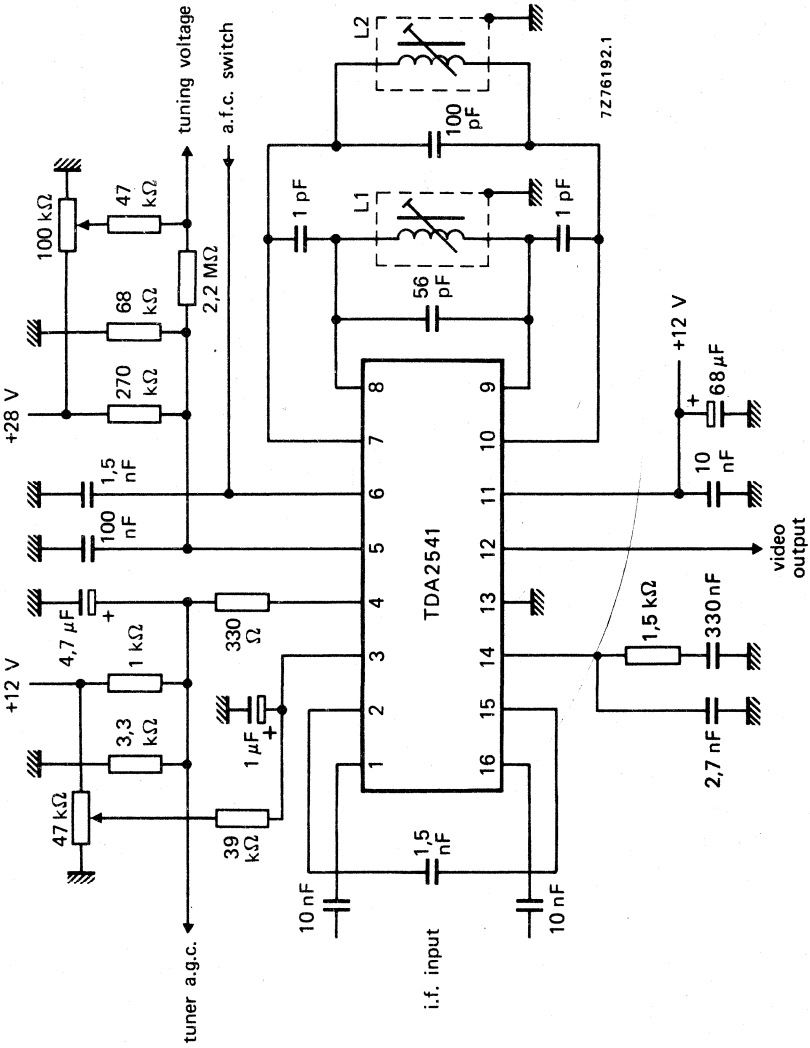
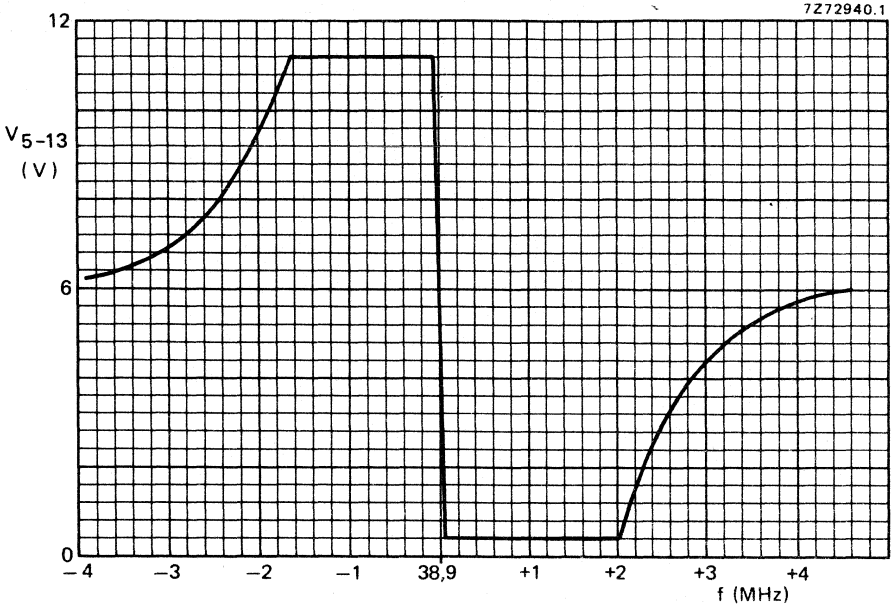


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f_O = 38,9 MHz.



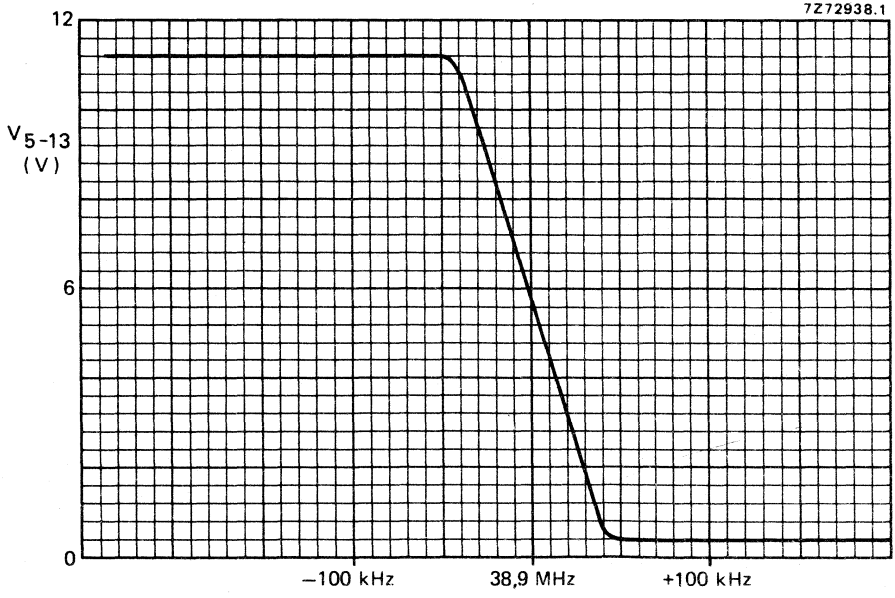


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

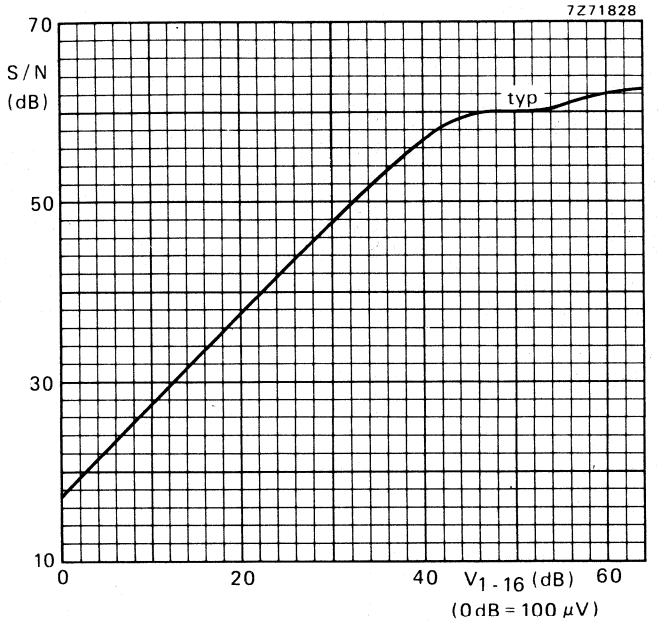


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2542 is an i.f. amplifier and demodulator circuit for E and L standards in colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- video preamplifier
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit
- tuner a.g.c. output (p-n-p tuners)

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input voltage at f = 32,7 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100 μV
Video output voltage (peak-to-peak value)	$V_{12(p\text{-}p)}$	typ.	3 V
I.F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10 V

PACKAGE OUTLINES

TDA2542 : 16-lead DIL; plastic (SOT-38).
TDA2542Q: 16-lead QIL; plastic (SOT-58).

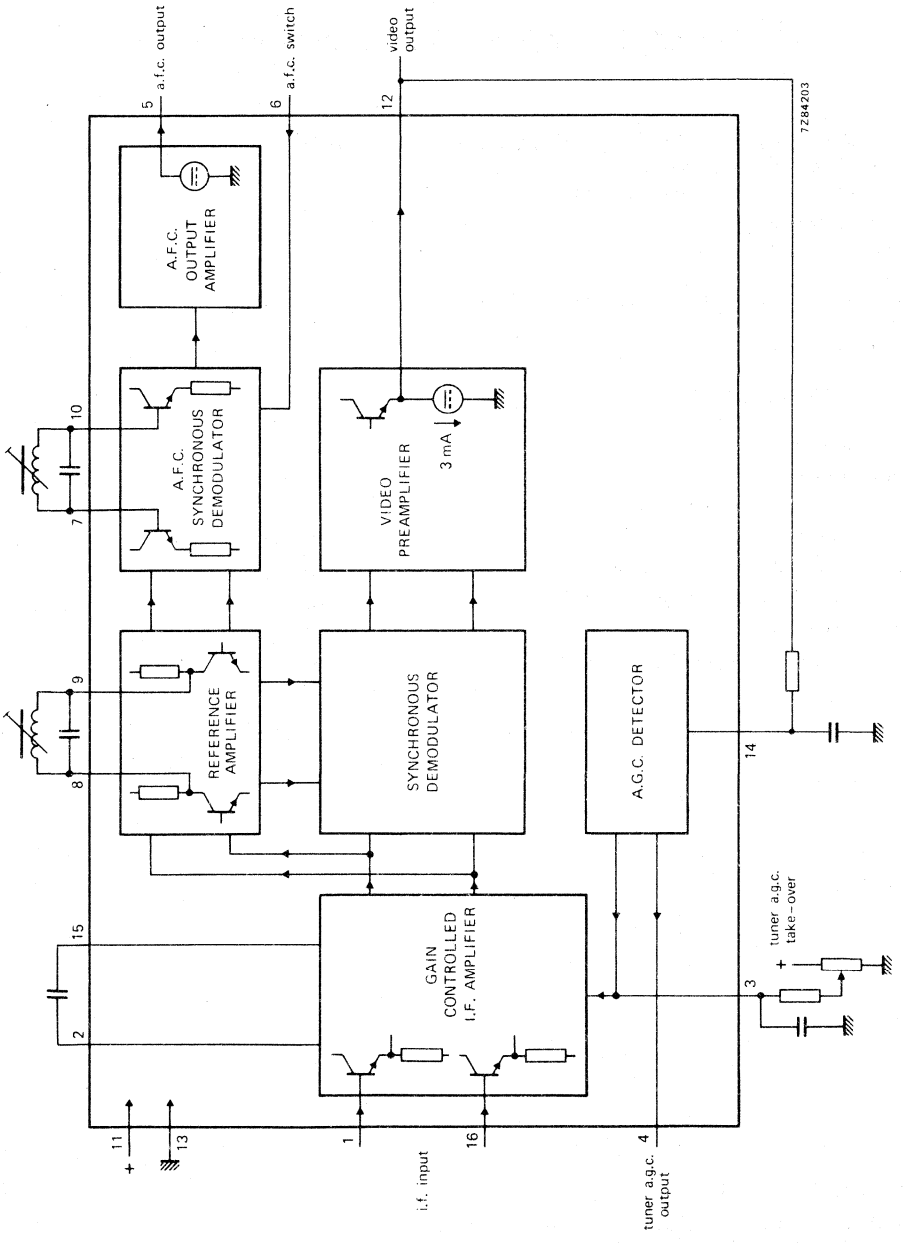


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13,8	V
Tuner a.g.c. voltage	V_{4-13}	max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 60	°C

CHARACTERISTICS (measured in Fig. 2)

Supply voltage range	V_{11-13}	typ.	12	V
			10,2 to 13,8	V

The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V; f = 32,7 MHz

I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1-16(rms)}$	typ.	100	μV
		<	150	μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	2 kΩ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ.	2,9	V
Maximum video output voltage (peak-to-peak value)	$V_{12(p-p)}$	>	4	V
Video output voltage variation at 50 dB input voltage variation	ΔV_{12-13}	<	0,5	dB
I.F. voltage gain control range	G_v	typ.	64	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB*
Differential gain	dG	typ.	4	%
		<	10	%
Differential phase	$d\varphi$	typ.	2°	
		<	10°	

* $S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.

CHARACTERISTICS (continued)

Carrier signal at video output		typ. <	4 mV 30 mV
2nd harmonic of carrier at video output		typ. <	20 mV 30 mV
Tuner a.g.c. output current range	I_4		0 to 10 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 3 V; V_{4-13} = 12 V	I_4	<	15 μA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	> typ.	10 V 11 V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ. <	100 kHz 200 kHz
A.F.C. switches on at:	V_{6-13}	>	3,2 V
A.F.C. switches off at:	V_{6-13}	<	1,5 V
A.G.C. detector reference voltage	V_{14-13}	typ.	3,9 V

APPLICATION INFORMATION

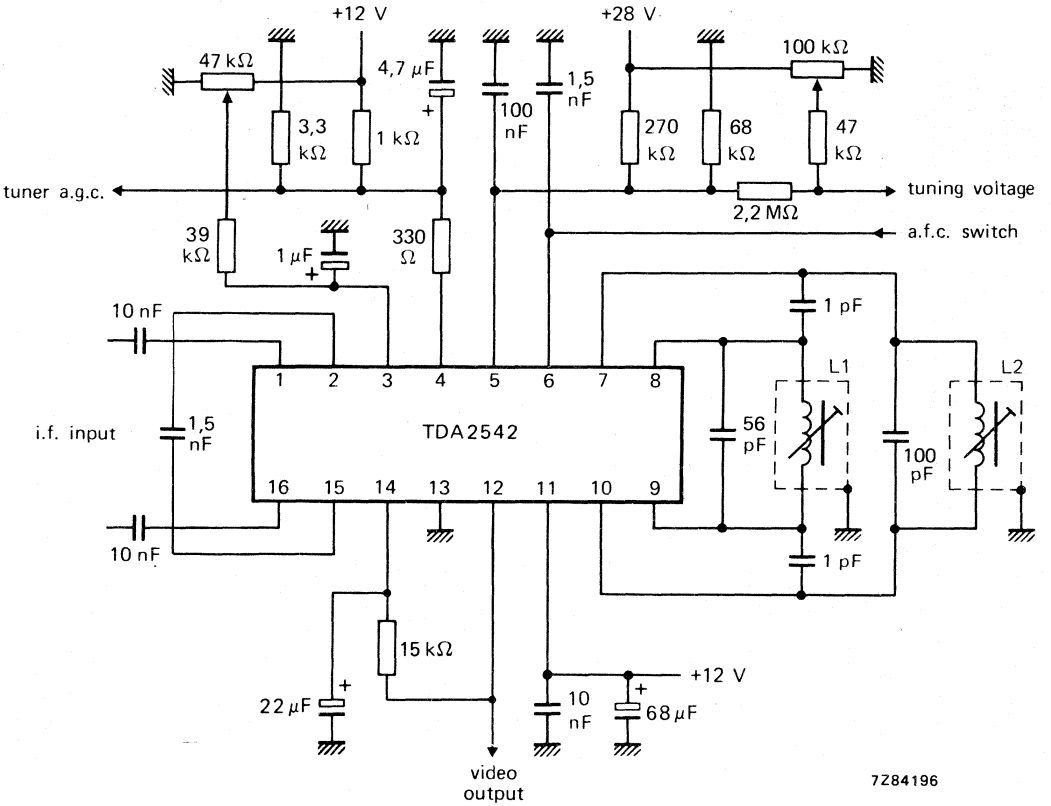


Fig. 2 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 32,7 MHz.

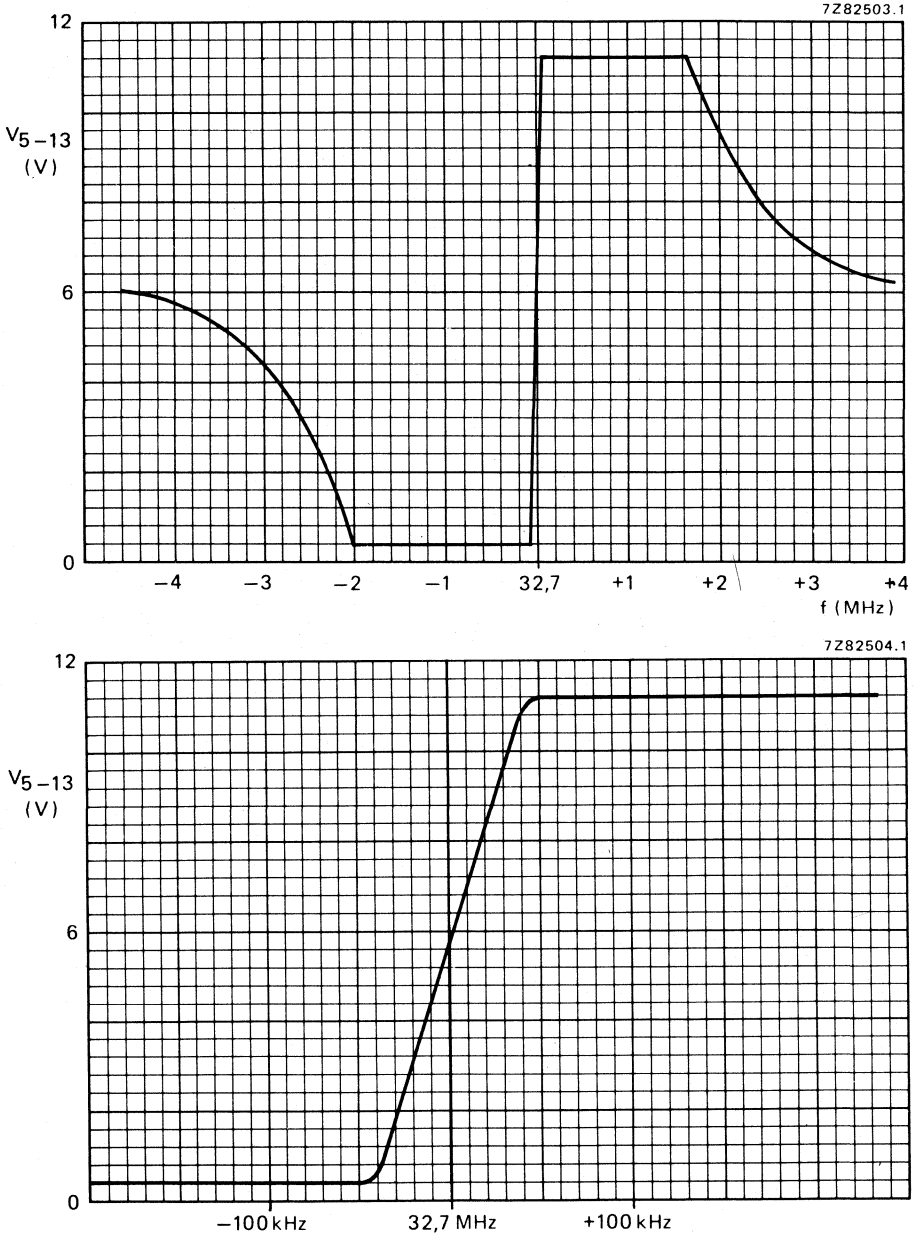


Fig. 3 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

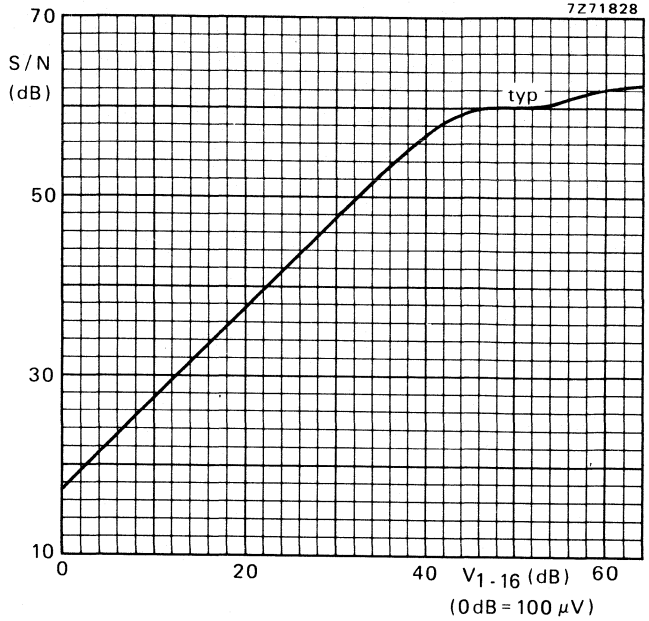


Fig. 4 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2544 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- low-level synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with balanced output
- a.g.c. circuit with noise gating
- tuner a.g.c. output for control of MOS tuners
- external video switch

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input sensitivity at f = 45,75 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	150 μV
Video output voltage (white at 12,5% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,6 V
I.F. voltage gain control range	G_v	typ.	63 dB
Signal-to-noise ratio V_i = 10 mV	S/N	typ.	58 dB
A.F.C. sensitivity		typ.	80 mV/kHz

PACKAGE OUTLINES

TDA2544 16-lead DIL; plastic (SOT-38).

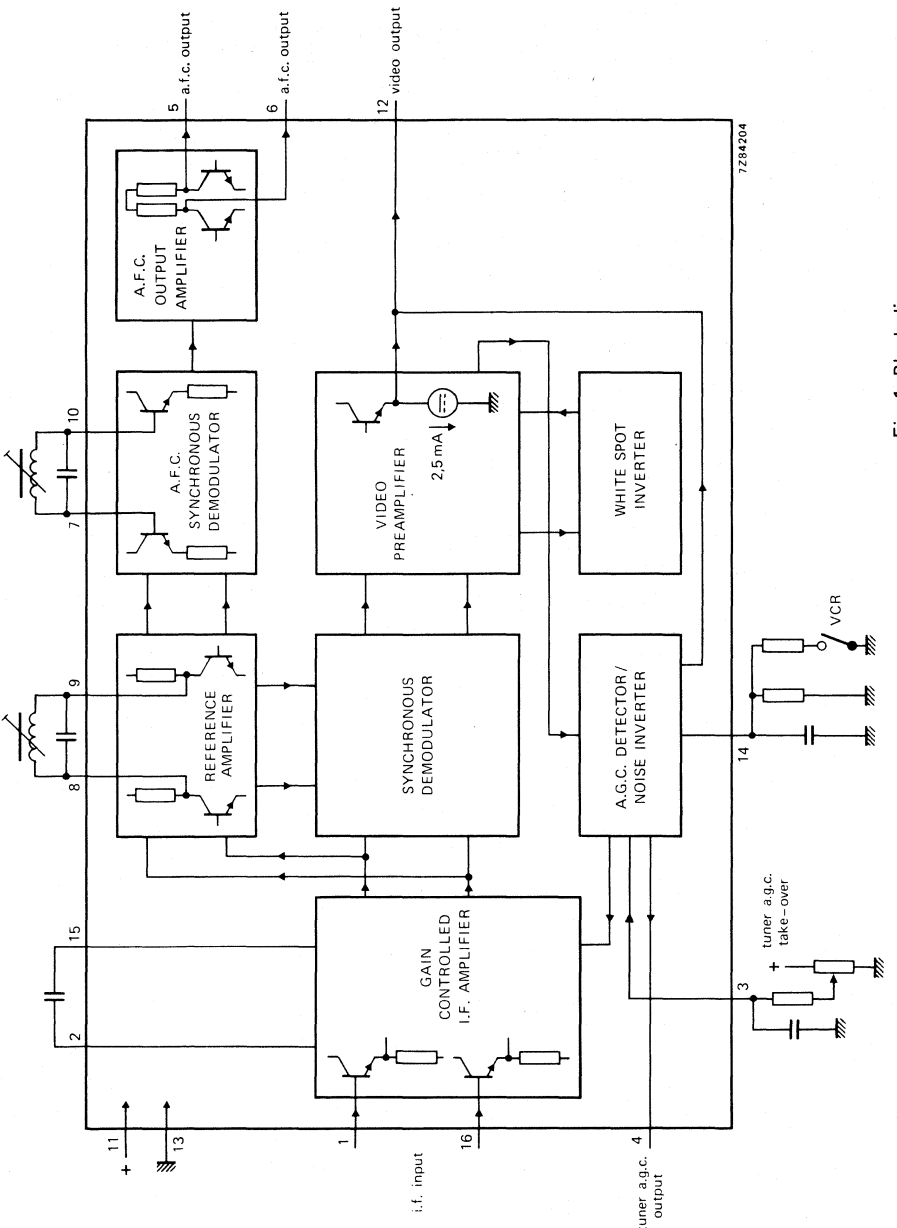


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13,8	V
Tuner a.g.c. voltage	V_{4-13}	max.	12	V
Total power dissipation	P_{tot}	max.	1,2	W
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS (measured in Fig. 5)

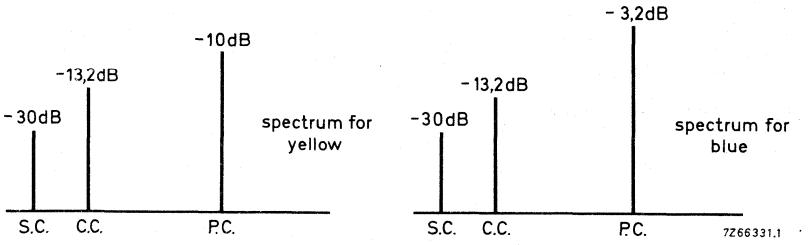
Supply voltage range	V_{11-13}	typ.	12	V
			10,2 to 13,8	V
The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V				
I.F. input voltage for onset of a.g.c. (r.m.s. value) at f = 45,75 MHz	$V_{1-16(rms)}$	typ.	150	μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	3 kΩ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ.	5,5	V*
Top sync output level	V_{12-13}	typ.	2,5	V
I.F. voltage gain control range	G_v	typ.	63	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ.	4	%
		<	10	%
Differential phase	$d\varphi$	typ.	2°	
		<	10°	

* So-called 'projected zero point', e.g. with switched demodulator.

** $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.

CHARACTERISTICS (continued)

Intermodulation at 0,9 MHz: blue*	typ.	50	dB
yellow*	typ.	46	dB
at 2,6 MHz**	typ.	49	dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

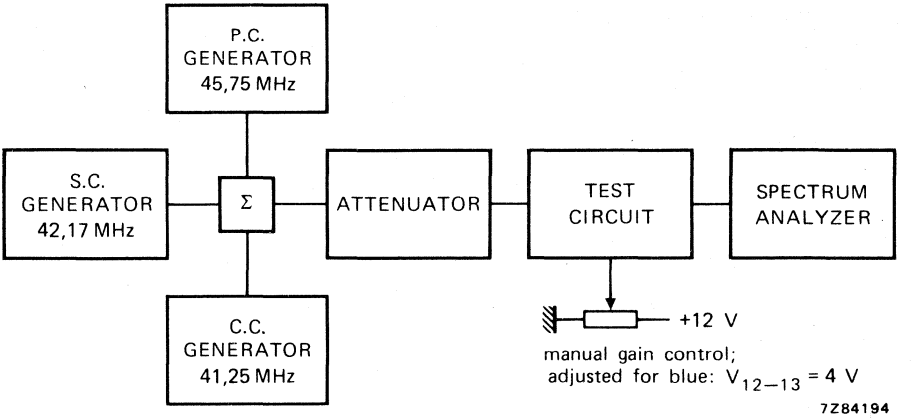


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 3{,}6 \text{ MHz}}{V_o \text{ at } 0{,}9 \text{ MHz}} + 3{,}6 \text{ dB}$. ** $20 \log \frac{V_o \text{ at } 3{,}6 \text{ MHz}}{V_o \text{ at } 2{,}6 \text{ MHz}}$.

Carrier signal at video output		<	30 mV
2nd harmonic of carrier at video output		<	30 mV
White spot inverter threshold level (Fig. 4)		typ.	6,4 V
White spot insertion level (Fig. 4)		typ.	4,1 V
Noise inverter threshold level (Fig. 4)		typ.	1,6 V
Noise insertion level (Fig. 4)		typ.	3,3 V
External video switch (VCR) switches off the output at	V_{14-13}	<	1,0 V

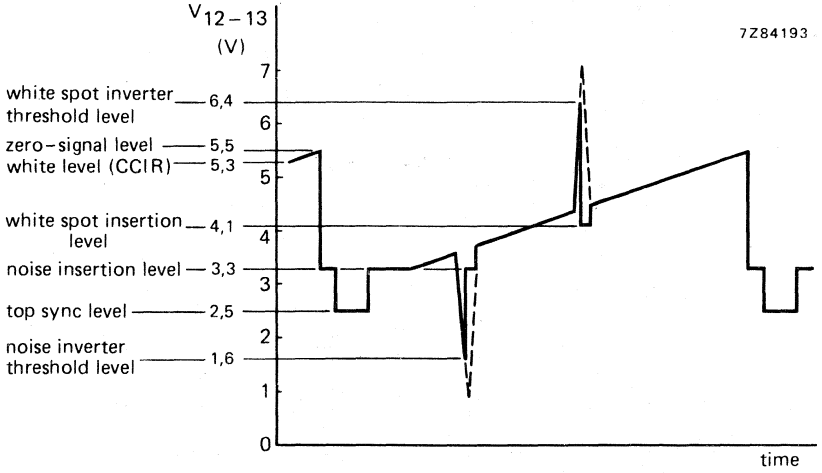


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 0,3 mA
Tuner a.g.c. output voltage at I_4 = 0,3 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 3 V; V_{4-13} = 12 V	I_4	<	10 μA
A.F.C. output voltage (d.c. value)	$V_{5;6-13}$	typ.	6,8 V
A.F.C. output offset voltage	$\lvert V_{5-6} \rvert$	<	1,5 V
Maximum a.f.c. output voltage	$V_{5;6-13}$	>	11,6 V
Minimum a.f.c. output voltage	$V_{5;6-13}$	<	2,8 V
A.F.C. sensitivity		typ.	80 mV/kHz

DEVELOPMENT SAMPLE DATA

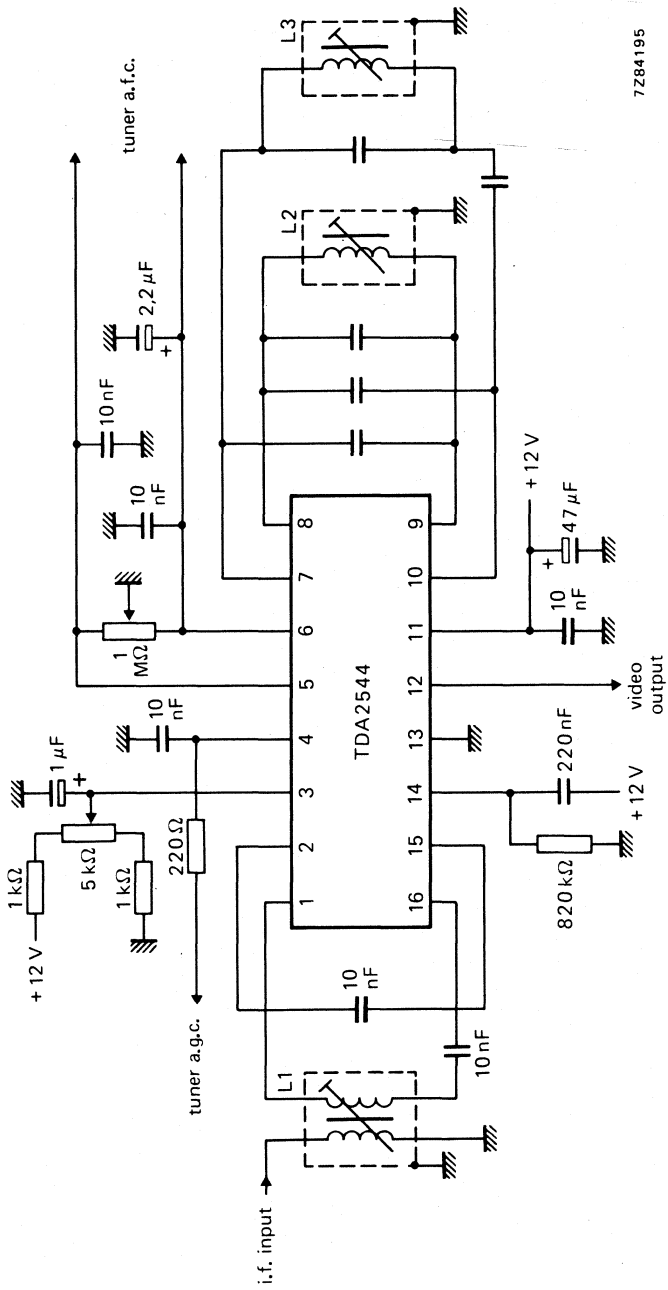


Fig. 5 Typical application diagram.

APPLICATION INFORMATION

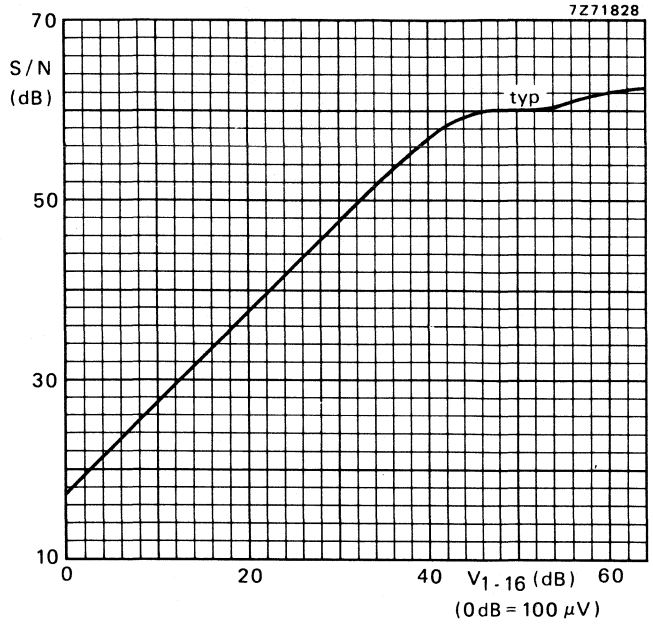


Fig. 6 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

DEVELOPMENT SAMPLE DATA

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is a monolithic integrated circuit for use in decoding systems of colour television receivers. The circuit consists of a luminance and chrominance amplifier. The luminance amplifier has a low input impedance so that matching of the luminance delay line is very easy.
It also incorporates the following functions:

- d.c. contrast control;
- d.c. brightness control;
- black level clamp;
- blanking;
- additional video output with positive-going sync.

The chrominance amplifier comprises:

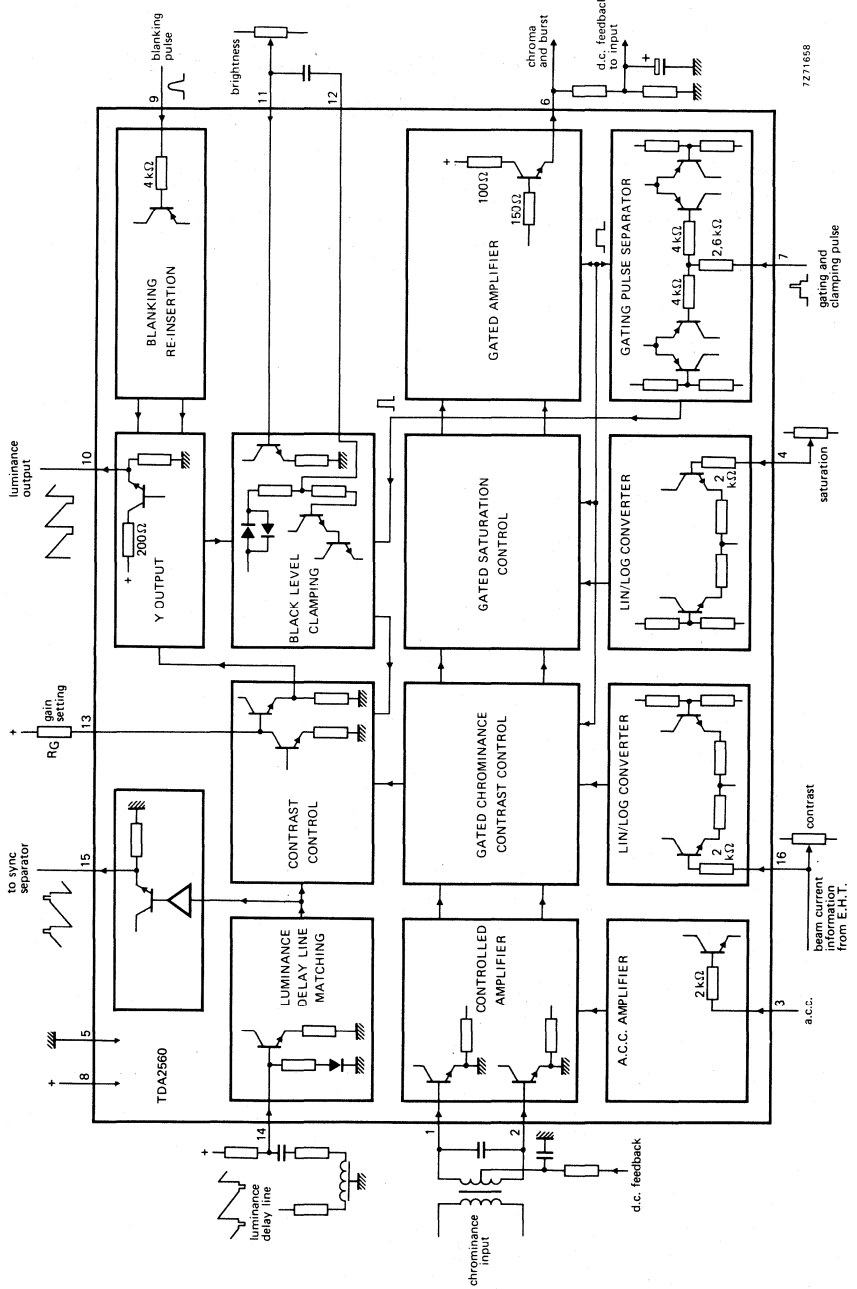
- gain controlled amplifier;
- chrominance gain control tracked with contrast control;
- separate d.c. saturation control;
- combined chroma and burst output, burst signal amplitude not affected by contrast and saturation control;
- the delay line can be driven directly by the IC.

QUICK REFERENCE DATA				
Supply voltage	V_{8-5}	typ.	12	V
Supply current	I_8	typ.	45	mA
Luminance signal input current (black-to-white value)	I_{14}	typ.	0,2	mA
Chrominance input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Luminance output signal at nominal contrast (black-to-white value)	V_{10-5}	typ.	3	V
Chrominance output signal at nominal contrast and saturation and 1,25 V peak-to-peak burst output (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2,5	V
Contrast control range		>	20	dB
Saturation control range		>	20	dB

PACKAGE OUTLINES

TDA2560 : 16-lead DIL ; plastic (SOT-38).
TDA2560Q: 16-lead QIL ; plastic (SOT-58).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage				
Supply voltage	V_{8-5}	max.	14	V
Power dissipation				
Total power dissipation	P_{tot}	max.	930	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +65	°C

CHARACTERISTICS measured in the circuit on page 7

Supply voltage range	V_{8-5}	typ.	12	V
			10 to 14	V
Supply current	I_8	typ.	45	mA[1])
Allowable hum on supply line (peak-to-peak value)	$V_{8-5(p-p)}$	<	100	mV

The following data are measured at V_{8-5} = 12 V; T_{amb} = 25 °C; R_G = 2,7 kΩ

Luminance amplifier

Input signal current; black-to-white value	I_{14}	typ.	0,2	mA
Input bias current	I_{14}	typ.	0,25	mA
Input impedance	$\|Z_{14-5}\|$	typ.	150	Ω[2])
Gain (pin 13)	see note 1 on page 5			
Contrast control range		>	20	dB
Contrast control voltage range	V_{16-5} (see control curve on page 6)			
Contrast control current	I_{16}	<	8	μA
Black level range	V_{10-5}		1 to 3	V
Brightness control voltage range	V_{11-5}	typ.	1 to 3	V
Brightness control current	I_{11}	<	20	μA[3])
Black level stability when changing temperature		typ.	0,1	mV/°C
Black level stability when changing contrast	see page 9 (pin 10)			
Bandwidth (−3 dB)	B	>	5	MHz[4])

[1]) At a load on pin 6 of 1,5 kΩ, and no load on pins 10 and 15.

[2]) At an input bias current of 0,25 mA.

[3]) At V_{11-5} > 4 V.

[4]) At nominal contrast (max. contrast setting −3 dB).

CHARACTERISTICS (continued)

Output voltage (black-to-white value)	V_{10-5}	typ.	3	V
Output voltage (additional; positive-going sync) peak-to-peak value	$V_{15-5(p-p)}$	typ.	3,4	V[1])
Black level clamp pulse (see note 2 on page 5)				
on level	V_{7-5}		7 to V_{8-5}	V
off level	V_{7-5}	<	5	V
Blanking pulse (see note 3 on page 5)				
for 0 V on pin 10: on level	V_{9-5}		2,5 to 4,5	V
off level	V_{9-5}	<	1,5	V
for 1,5 V on pin 10: on level	V_{9-5}		6 to V_{8-5}	V
off level	V_{9-5}	<	4,5	V
Chrominance amplifier 2)				
Input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Chrominance output signal at nominal contrast and saturation setting (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2	V3)
Maximum chrominance output signal	V_{6-5}		4,6	V
Bandwidth (−3 dB)	B	typ.	6	MHz
Ratio of burst and chrominance at nominal contrast and saturation	see notes 4 and 5 on page 5			
A.C.C. starting voltage (see note 6 on page 5)	V_{3-5}	typ.	1,2	V
A.C.C. range		>	30	dB
Tracking between luminance and chrominance with contrast control (10 dB control)		typ.	±1	dB
Saturation control range		>	20	dB
Saturation control voltage range	V_{4-5} (see control curve on page 6)			
Gating pulse for chrominance amplifier				
on level	V_{7-5}		2,3 to 5	V
off level	V_{7-5}	<	1	V
width	t_7	>	8	µs
Signal-to-noise ratio at nominal input voltage	S/N	>	46	dB
Phase shift between burst and chrominance		<	5^o	

1) For I_{14} = 0,2 mA (black-to-white value).

2) All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio is 1:2.

3) At a burst signal of 1 V peak-to-peak; see also notes 4 and 5 on page 5.

NOTES

1. The gain of the luminance amplifier can be adjusted, by setting the gain of the contrast control circuit by selection of discrete resistor R_G (see also circuit on page 7). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is now the spread of the ratio of the delay line matching resistors and the resistor R_G). At R_G = 2,7 kΩ the output voltage at nominal contrast (maximum −3 dB) is 3 V black-to-white for an input current of 0,2 mA black-to-white.

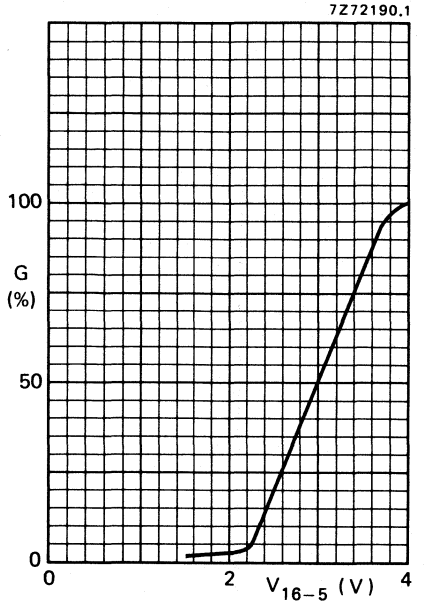
2. This pulse (pin 7) is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a +7 V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2,3 V and switches it back to normal setting when the pulse falls below 1 V.

3. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the +2,5 V level the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level a fixed level of typ. +1,5 V is inserted in the output signal. This level can be used for clamping purposes.

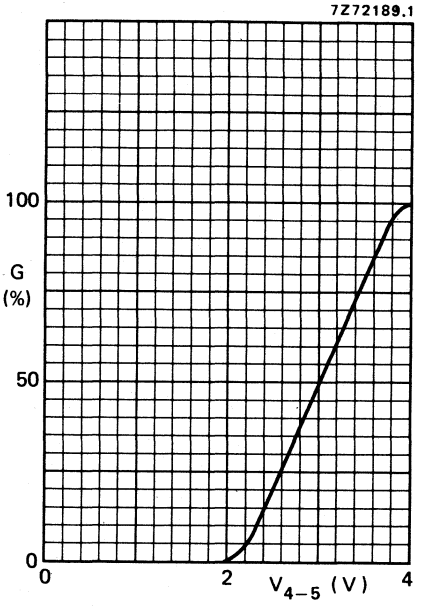
4. The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the a.c.c. circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically identical to that at the input.

5. Nominal contrast is specified as maximum contrast −3 dB. Nominal saturation is specified as maximum saturation −6 dB.

6. A negative-going control voltage gives a decrease in gain.

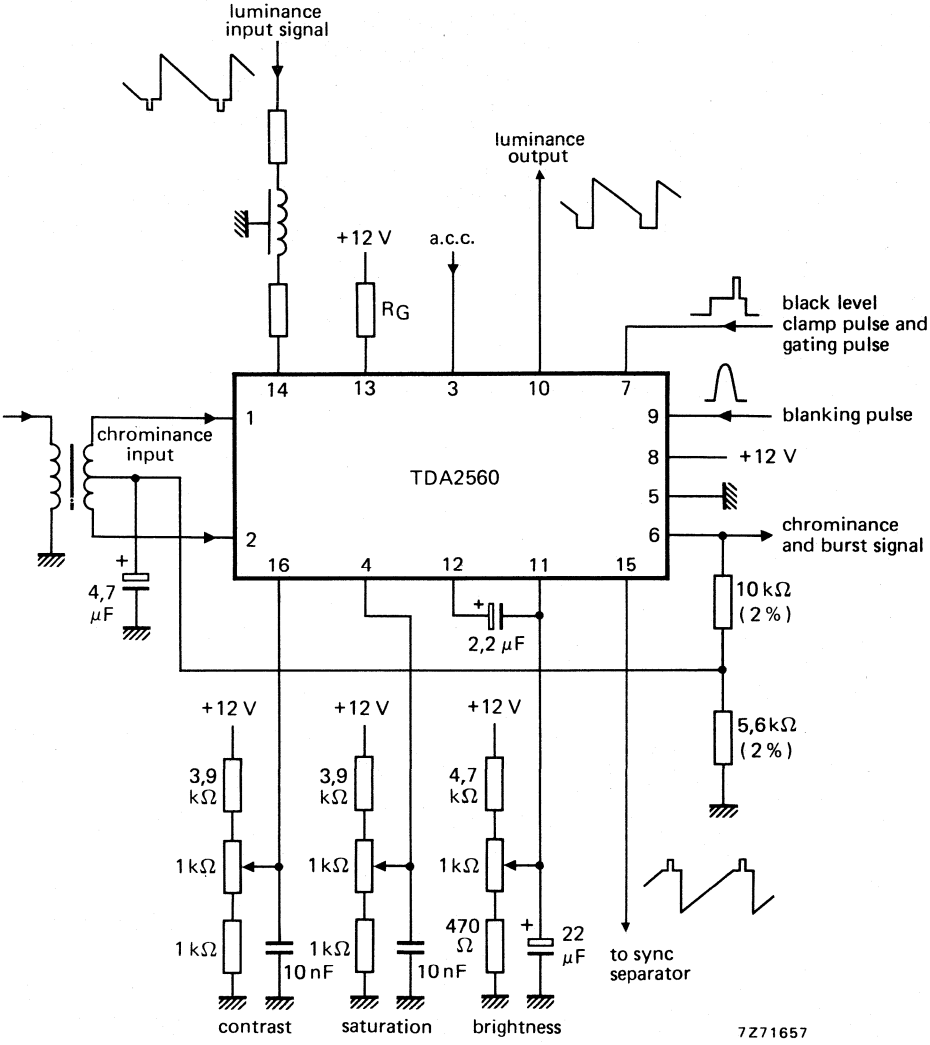


Contrast control of luminance and chrominance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Balanced chrominance input signal (in conjunction with pin 2)

   This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3 V.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio of input signal is 1 : 2.

2. Chrominance signal input (see pin 1)

3. A.C.C. input

   A negative-going potential, starting at +1,2 V, gives a 40 dB range of a.c.c. Maximum gain reduction is achieved at an input voltage of 500 mV.

4. Chrominance saturation control

   A control range of +6 dB to >−14 dB is provided over a range of d.c. potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. Negative supply (earth)

6. Chrominance signal output

   For nominal settings of saturation and contrast controls (max. −6 dB for saturation, and max. −3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The a.c.c. circuit of the TDA2522 will hold constant the colour burst amplitude at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide d.c. negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input

   A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 µs, at the actuating level of 2,3 V.

APPLICATION INFORMATION (continued)

8. +12 V power supply

Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform

This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2, 5 V level, the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level, a fixed level of about 1, 5 V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output

An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required.
The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current I_{14} of 0, 25 mA during black level the amplifier is compensated so that no black level shift more than 10 mV occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100 mV/mA.

11. Brightness control

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. Black level clamp capacitor

13. Luminance gain setting resistor

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. Nominal luminance output amplitude is then 3 V black-to-white at pin 10 when this resistor is 2, 7 kΩ and the input current is 0, 2 mA black-to-white. Maximum and minimum values of this resistor are 3, 9 kΩ and 1, 8 kΩ.

14. Luminance signal input

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0, 2 mA black-to-white. The luminance signal may be coupled to pin 14 via a d.c. blocking capacitor and, in addition, a resistor employed to give a d.c. current into pin 14 at black level of about 0, 25 mA. Alternatively d.c. coupling from a signal source such as the TDA2540 and TDA2541 may be employed.

APPLICATION INFORMATION (continued)

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3, 4 V peak-to-peak when the luminance signal input is 0, 2 mA black-to-white.

16. Contrast control

With 3 V on this pin the gain of the luminance channel is such that 0, 2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2, 7 kΩ is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives −17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

HORIZONTAL SYNCHRONIZATION AND VERTICAL 625 DIVIDER SYSTEM

The TDA2571A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2571A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,25 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (625 divider system), without delay after channel change.

QUICK REFERENCE DATA

Supply voltage				
horizontal	V_{12-11}	typ.	12	V
vertical	V_{16-11}	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2-11(p-p)}$		0,07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8-11(p-p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1-11(p-p)}$	typ.	11	V
Burst-key output pulse (peak-to-peak value)	$V_{13-11(p-p)}$	typ.	11	V

PACKAGE OUTLINES

TDA2571A: 16 lead DIL; plastic (SOT-38).
TDA2571AQ: 16-lead QIL; plastic (SOT-58).

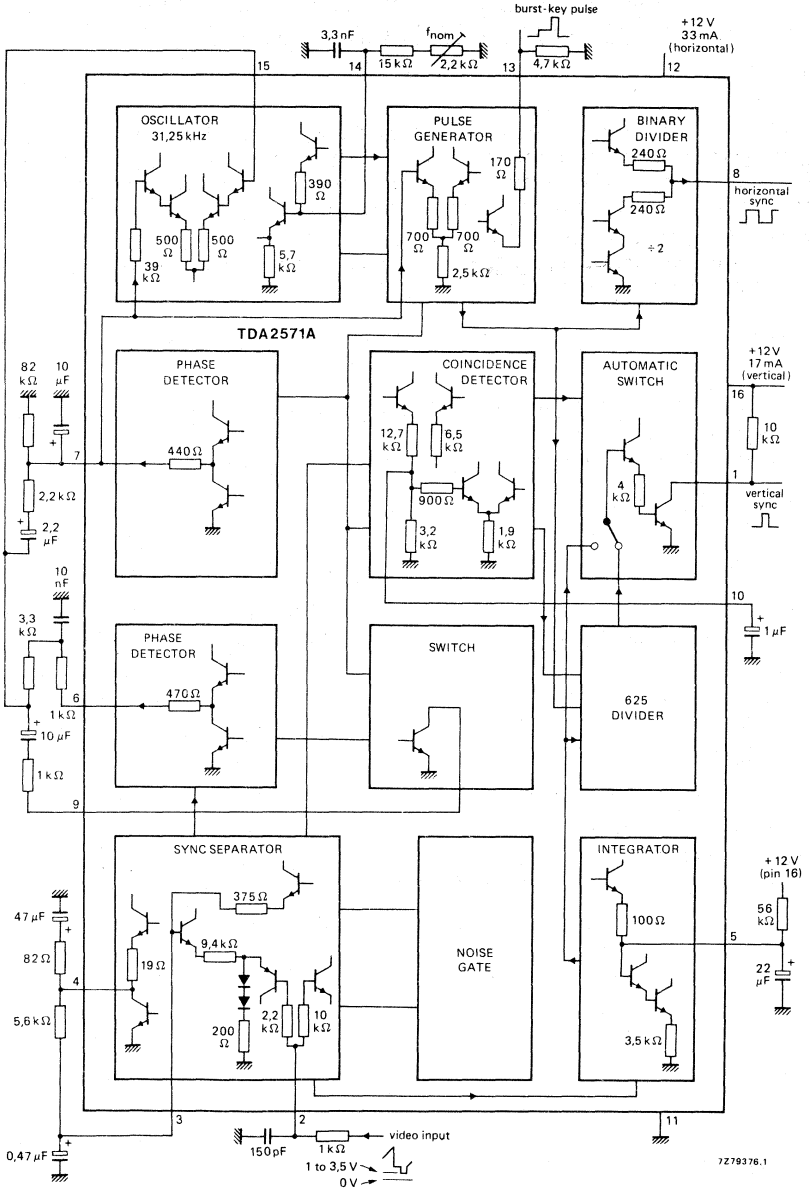


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Sypply voltage			
horizontal	V_{12-11}	max.	13,2 V
vertical	V_{16-11}	max.	13,2 V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−25 to + 130 °C
Operating ambient temperature	T_{amb}		−25 to + 65 °C

CHARACTERISTICS

At V_{12-11} = 12 V; V_{16-11} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Supply voltage range (pins 12 and 16)	V_{12-11}; V_{16-11}	typ.	12 V
			10 to 13,2 V
Current consumption	$I_{12} + I_{16}$	typ.	50 mA
		<	75 mA
Sync separator and noise gate			
Sync pulse amplitude (negative going) peak-to-peak value	$V_{2-11(p-p)}$		0,07 to 1 V*
Top-sync level	V_{2-11}		1,0 to 3,5 V
Slicing level		typ.	50 %**
Slicing level noise gating	V_{2-11}	typ.	0,7 V
Phase locked loop			
Holding range	Δf	typ.	± 1000 Hz
Catching range	Δf	typ.	± 900 Hz
Control sensitivity of horizontal PLL		typ.	2000 Hz/μs
Control sensitivity of phase detector		typ.	1,2 V/μs
Delay between sync input and detector output (pin 6)	t_d	typ.	0,4 μs
Phase modulation due to hum on the supply line		typ.	2,0 μs/V▲

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

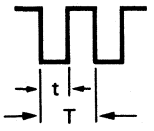
** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 μs/V(p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

CHARACTERISTICS (continued)

Horizontal oscillator				
Frequency; free running	f_o	typ.	31,250	kHz
Frequency at output pin 8	f_8	typ.	15,625	kHz
Spread of frequency without spread of external components	Δf_o	<	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	K^{-1}
Change of frequency when V_{12-11} drops to 6 V	Δf_o	<	10	%
Change of frequency when V_{12-11} increases from 10 to 13,2 V	Δf_o	<	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8-11(p-p)}$	>	10	V
Output resistance	R_{8-11}	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p-p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	%*
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	µs**
Burst-key pulse				
Output voltage (peak-to-peak value)	$V_{13-11(p-p)}$	>	10	V
Duration of upper part of output pulse	t_p	typ.	3,6	µs**
Duration of lower part of output pulse	t_p	typ.	9,1	µs**
Amplitude of lower part of output pulse	$V_{13-11(p-p)}$	typ.	3	V**
Output resistance	R_{13-11}	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_d	typ.	0,9	µs**
Coincidence detector				
Voltage level of time constant switch	V_{10-11}	typ.	2,0	V
Voltage when the oscillator is in sync	V_{10-11}	typ.	0,4	V
Voltage when the oscillator is out-of-sync	V_{10-11}	typ.	2,5	V
Voltage during noise	V_{10-11}	typ.	1,0	V

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1\text{-}11(p\text{-}p)}$	>	10 V
Duration of output pulse during indirect synchronization	t_p	typ.	170 µs
Duration of output pulse during direct synchronization (coincidence detector high)	t_p	typ.	160 µs
Load resistor to pin 2	R_L	>	2 kΩ
Output voltage low with R_L = 2 kΩ	$V_{1\text{-}11}$	<	500 mV
Ratio between basic horizontal oscillator frequency and vertical pulse			625 *

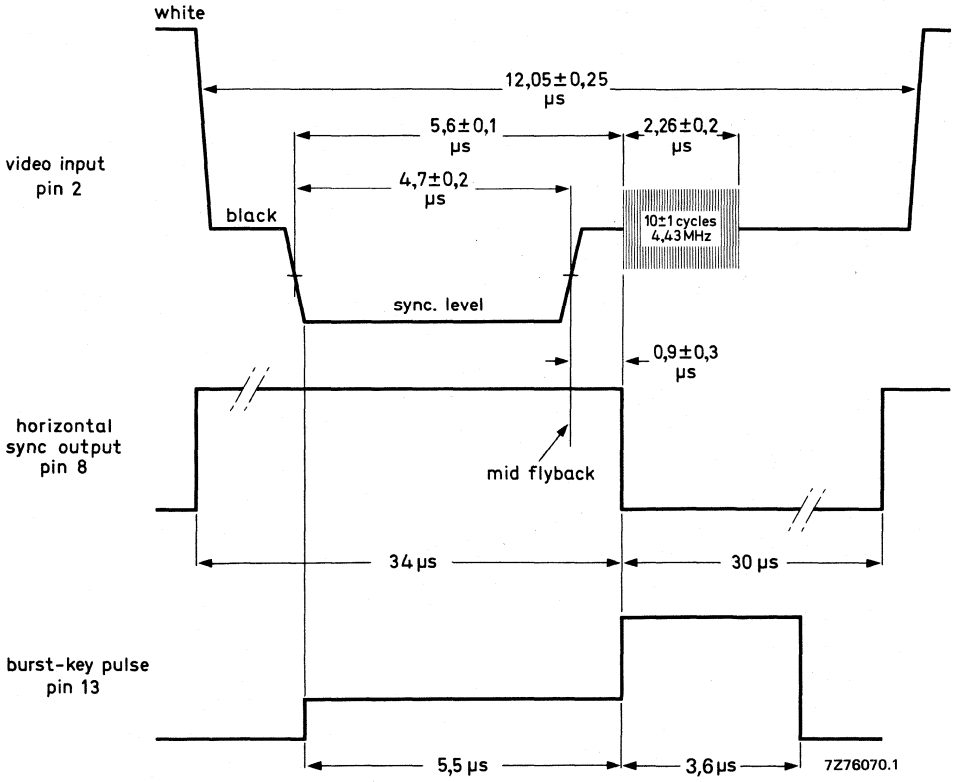


Fig. 2 Relationship between the video input signal to the TDA2571A and the horizontal sync and burst-key pulse output.

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 625 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2571A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; C = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:
    - when in-sync: 0,4 V
    - when out-of-sync: 2,0 V
    - during noise at input: 1,0 V

    When the output voltage $<$ 1,85 V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage $>$ 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs.The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

APPLICATION INFORMATION (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

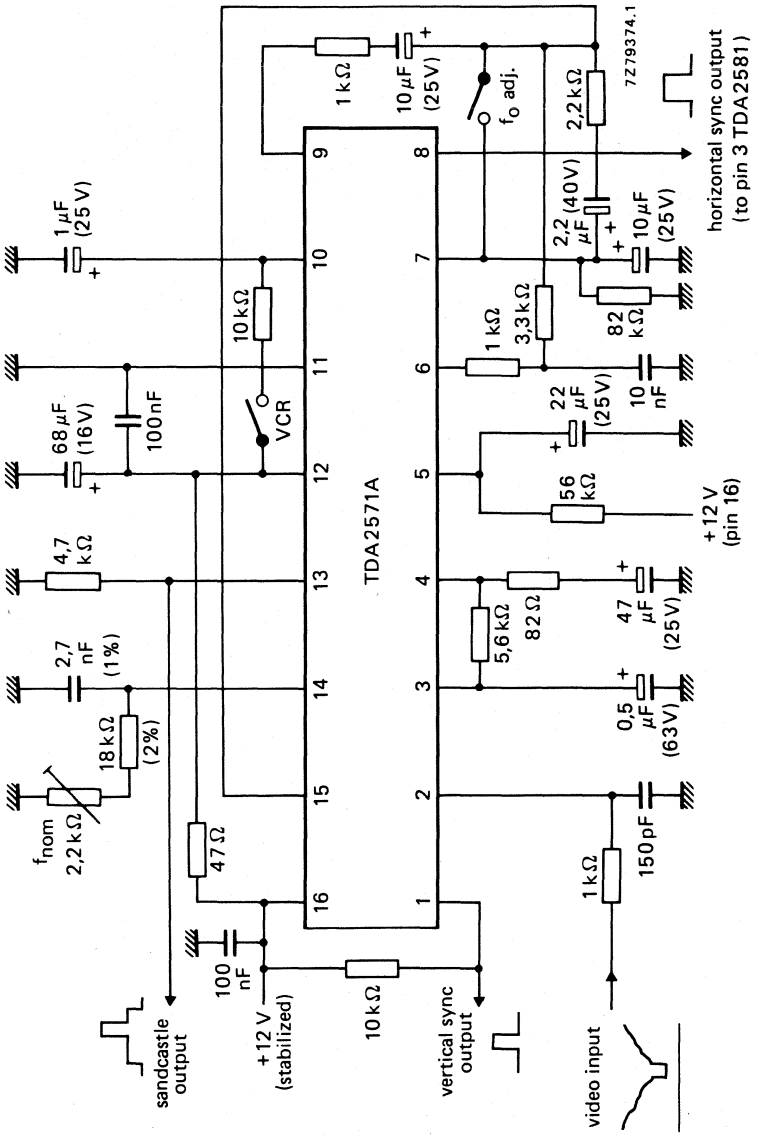


Fig. 3 Typical application circuit diagram; for combination of the TDA2571A with the TDA2581 see Fig. 4.

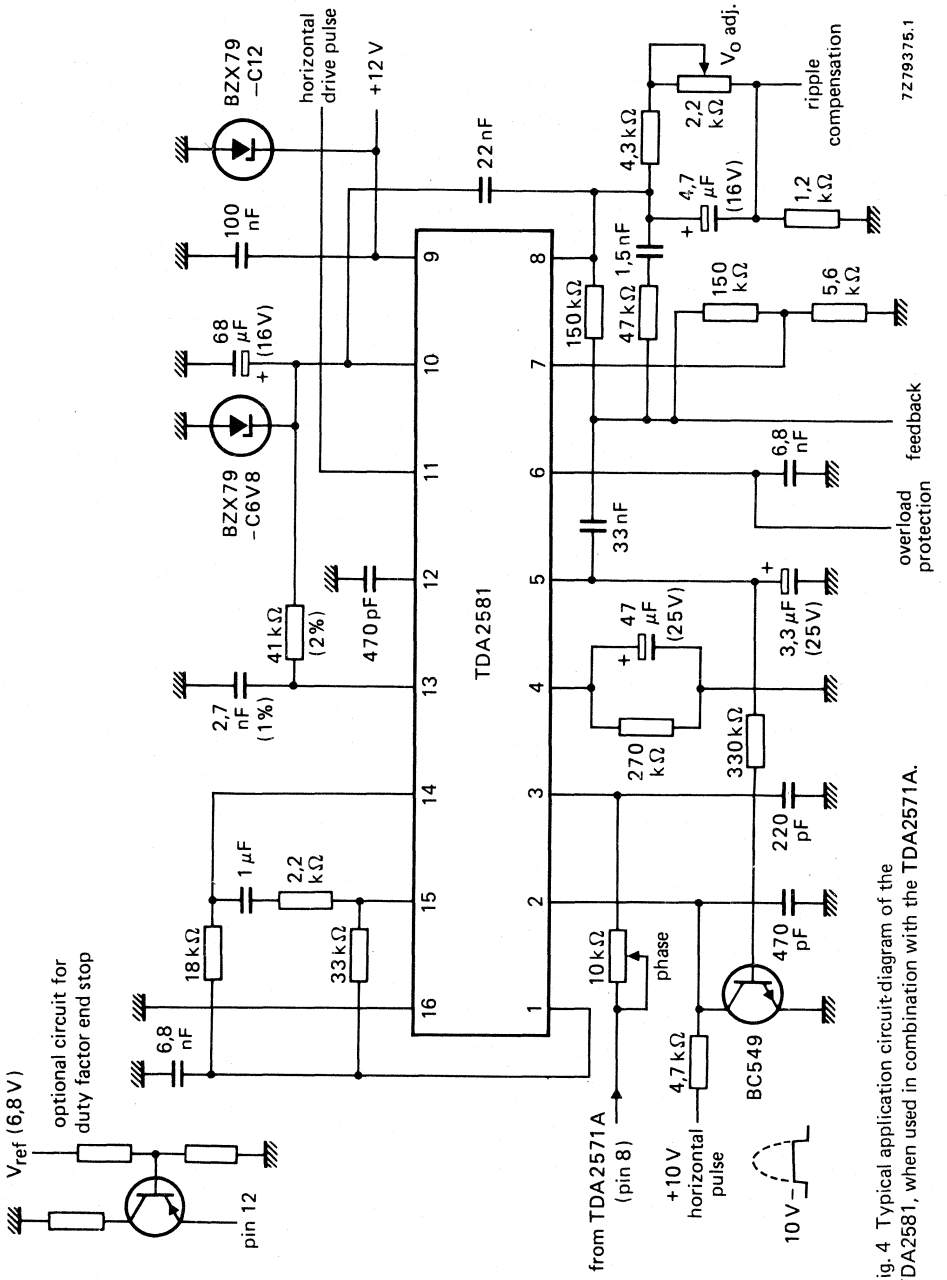


Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2571A.

HORIZONTAL OSCILLATOR COMBINATION WITH VERTICAL 525 DIVIDER SYSTEM

The TDA2573A is a horizontal oscillator combination intended to be used in various types of transistorized horizontal deflection circuits, e.g. switched-mode driven and power-pack system circuits.

The circuit is optimized for a horizontal and vertical frequency ratio of 525.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such way that the sync pulse is always sliced between top sync level and blanking level.
- Noise gate.
- Phase detector which compares the sync pulse with the oscillator voltage; this phase detector is gated.
- Phase detector which compares the line flyback pulse with the oscillator voltage.
- Horizontal oscillator (31,5 kHz).
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals).
- Burst key pulse generator (sandcastle pulse with three levels).
- Vertical sync pulse separator.
- Very stable vertical synchronization due to the 525 divider system, without delay after channel change.

QUICK REFERENCE DATA

Supply voltage	$V_{16\text{-}9}$	typ.	12 V
Supply current consumption	I_{16}	typ.	53 mA
Sync input voltage (peak-to-peak value)	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1 V
Slicing level		typ.	50 %
Control sensitivity sync to flyback		typ.	10 kHz/μs
Holding range	Δf	typ.	± 1000 Hz
Catching range	Δf	typ.	± 900 Hz
Horizontal output pulse (peak-to-peak value)	$V_{10\text{-}9(p\text{-}p)}$	typ.	11 V
Vertical output pulse; pin 2 (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	typ.	11 V
Sandcastle output pulse (peak-to-peak value)	$V_{14\text{-}9(p\text{-}p)}$	typ.	11 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

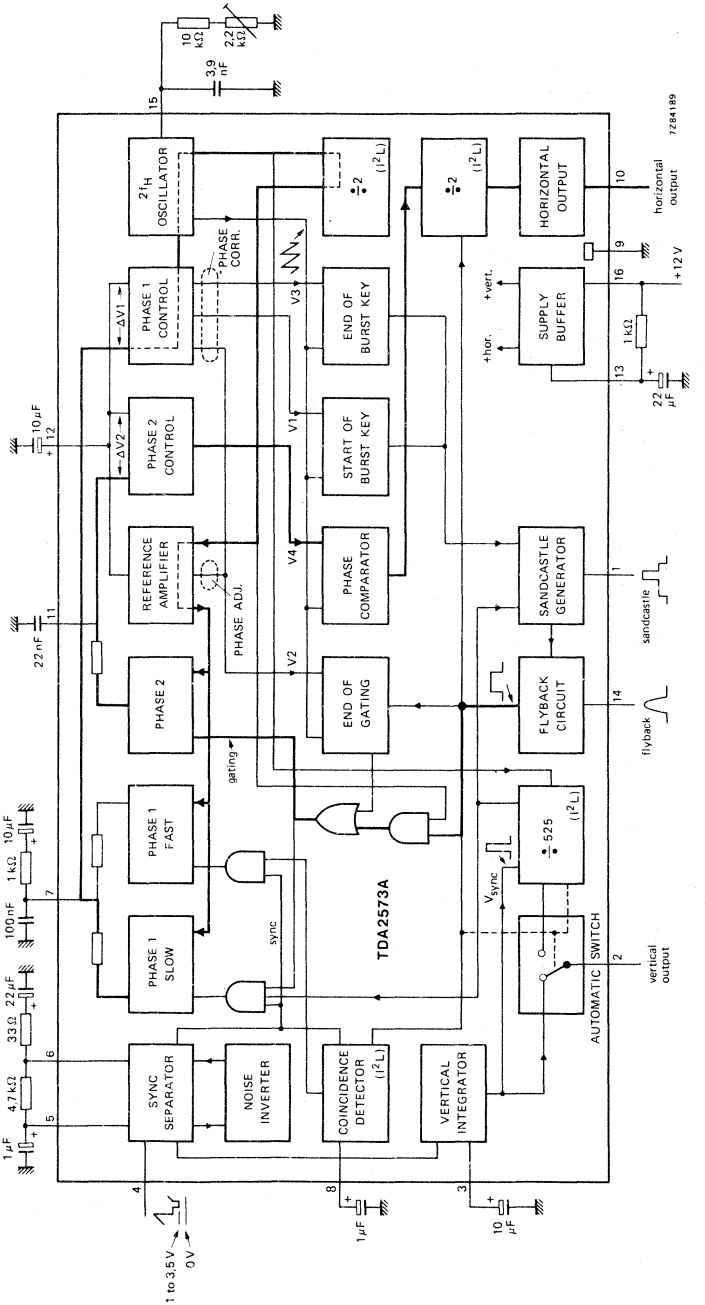


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{16\text{-}9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS

$V_{16\text{-}9}$ = 12 V; T_{amb} = 25 °C; measured in Fig. 2.

Supply voltage	$V_{16\text{-}9}$	typ.	12	V
			10 to 13,2	V
Supply current consumption	I_{16}	typ.	53	mA
		<	70	mA
Sync separator and noise gate				
Sync pulse amplitude (negative going) peak-to-peak value	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1	V*
Top-sync level	$V_{4\text{-}9}$		1,0 to 3,5	V
Slicing level noise gate	$V_{4\text{-}9}$	<	1	V
Delay between sync input and detector output (pin 7)		typ.	0,35	µs
First control loop (sync-to-oscillator)				
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity video				
with respect to oscillator		typ.	2,0	kHz/µs
with respect to sandcastle		typ.	10,0	kHz/µs
with respect to flyback pulse		typ.	10,0	kHz/µs
Phase modulation due to hum on the supply line (pin 16)		<	1,0	µs/V**
Second control loop (oscillator-to-flyback)				
Control sensitivity	$\Delta t_d/\Delta t_o$	typ.	250	▲
Control range	t_d	<	26	µs

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** This voltage is a peak-to-peak value.

▲ t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
t_o = delay between the rising edge of the flyback and the start of the current in $\varphi 1$ (I_7).

CHARACTERISTICS (continued)

Horizontal oscillator			
Frequency; free running	f_o	typ.	31,500 kHz
Frequency at output pin 10	f_{10}	typ.	15,750 kHz
Spread of frequency without spread of external components	Δf_o	<	4 %
Temperature coefficient	T	typ.	2,5 to 10^{-4}
Change of frequency when V_{16-9} increases from 10 to 13,2 V	Δf_o	<	0,5 %
Minimum supply voltage (+ hor. see Fig. 1)		typ.	7 V
Frequency deviation at min. supply voltage		<	10 %
Horizontal output (pin 10)			
Maximum supply voltage		<	13,2 V
Minimum output voltage at a current of 60 mA	V_{10-9}	<	700 mV
Maximum output current	I_{10}	<	60 mA
Duration of the output pulse	t_p		12 to 38 μs
Sandcastle pulse (pin 1)			
Output voltage during burst key pulse	V_{1-9}	>	10 V
Pulse duration	t_p	typ.	4,0 μs
Amplitude of second level of output pulse	V_{1-9}	typ.	4,5 V
Pulse duration	flyback pulse		
Amplitude of third level of output pulse	V_{1-9}	typ.	2,5 V
Pulse duration	t_p	typ.	1,34 μs*
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the burst key pulse	t_d	typ.	4,9 μs
Phase adjustment (pin 12)			
Voltage at pin 12	V_{12-9}	typ.	2,8 V
Control sensitivity		typ.	0,6 V/μs
Control range		typ.	± 1 μs
Coincidence detector (pin 8)			
Voltage level of time constant switch	V_{8-9}	typ.	2,1 V
Voltage when the oscillator is in sync	V_{8-9}	typ.	1,2 V
Voltage when the oscillator is out-of-sync	V_{8-9}	typ.	2,6 V
Voltage during noise	V_{8-9}	typ.	1,7 V

* During standard video signals.

Flyback input pulse (pin 14)			
Switching level	V_{14-9}	typ.	0,7 V
Input pulse	V_{14-9}	<	12 V
Input resistance		typ.	2,5 kΩ
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the flyback pulse	t_p	typ.	1,5 μs
Vertical outputs			
Output voltage (peak-to-peak value)	$V_{2-9(p-p)}$	>	10 V
Output current	I_2	<	5 mA
Output voltage low at I_2 = 5 mA	V_{2-9}	<	500 mV
Duration of output pulse during indirect synchronization	t_p	typ.	190 μs
Duration of output pulse during direct synchronization	t_p	typ.	190 μs
Ratio between basic horizontal oscillator frequency and vertical pulse			525 *

DEVELOPMENT SAMPLE DATA

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 2; the pulse of the divider circuit is switched off.

APPLICATION INFORMATION (see also Fig. 2)

The function is described against the corresponding pin number

1. Sandcastle output pulse

   This output pulse has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level for the line blanking is typ. 4,5 V with a pulse duration equal to the line flyback pulse. The third level (typ. 2,5 V) is used for frame blanking and has a pulse duration of typ. 1,34 ms (21 lines). This last pulse is only available with a standard video input signal. Under all other conditions, an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by means of an internal clamping circuit. The input current is typ. 2 mA.

2. Vertical output pulse

   This pulse is obtained from the divider circuit, the amplitude is in excess of 10 V peak-to-peak. This pulse has a duration of 190 μs when standard signals are received. The pulse is obtained from the vertical sync pulse integrator during non-standard signals and has a duration of about 190 μs. It has good stability and accuracy, so it is intended to be used for triggering the vertical oscillator.

3. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor with an internal resistor are required for the correct biasing of this circuit for various input conditions. A typical value for the capacitor is 10 μF.

4. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,1 to 1 V peak-to-peak. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 100 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 1 V (typ. 0,7 V), thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

5. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 6. The capacitor connected to pin 5 must be about 1 μF.

6. Black level detector output

   The black level of the input signal is detected on this pin. A capacitor of 22 μF in series with a resistor of 33 Ω has to be connected to this pin. A 4,7 kΩ resistor must be connected between pins 5 and 6.

7. Horizontal phase detector output and control oscillator input

   The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 7 and 12.
   The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out of sync. The result is a large catching range, and the phase detector is not gated in that condition. The output current is low when the oscillator is synchronized and the phase detector is gated. A good noise immunity is obtained in this case.

8. Coincidence detector output

   A 1 μF capacitor must be connected to his pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
   The following output voltages can occur:
   – when in-sync 1,2 V
   – when out-of-sync 2,6 V
   – during noise at the input 1,7 V

   When the output voltage $<$ 2,1 V, the phase detector output current is low and the phase detector is gated. A good noise immunity is obtained in this case. For a voltage $>$ 2,1 V, the output current of the phase detector is high and the phase detector is not gated. This results in a large catching range and a high dynamical steepness of the PLL. This latter condition is required during VCR-playback. It can be obtained by connecting pin 8 to the positive supply line via a resistor of 10 kΩ.
   The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

9. Negative supply (ground)

10. Horizontal output

    This is an open collector output. The collector resistor must be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The output stage is designed such that the line output transistor cannot be switched-on during flyback. Switching-on occurs directly after the flyback pulse to avoid linearity errors. The duty factor of the output pulse depends on the delay in the output stage (correction via the second control loop).

11. Control voltage second loop

    This voltage controls the start of the output pulse at pin 10 (positive-going edge). The capacitor connected to this pin must have a value of about 22 nF.

12. Reference voltage control loops

    The reference voltage must be decoupled by means of a capacitor of about 10 μF.
    It is possible to obtain a phase shift between video and flyback pulse by changing this reference voltage externally. The possible phase shift is $\pm$ 1 μs.
    The required voltage change is $\pm$ 0,6 V.

13. Decoupling internal power supply

    The IC has two power supply terminals. The main terminal (pin 16) supplies the output stages, the sync separator and the divider circuit. The specially decoupled supply terminal (pin 13) supplies the horizontal oscillator. This is to avoid coupling of the video signal into the oscillator part. The capacitor connected to pin 13 should have a value of about 22 μF. The resistor connected between pins 13 and 16 should have a value of about 1 kΩ.

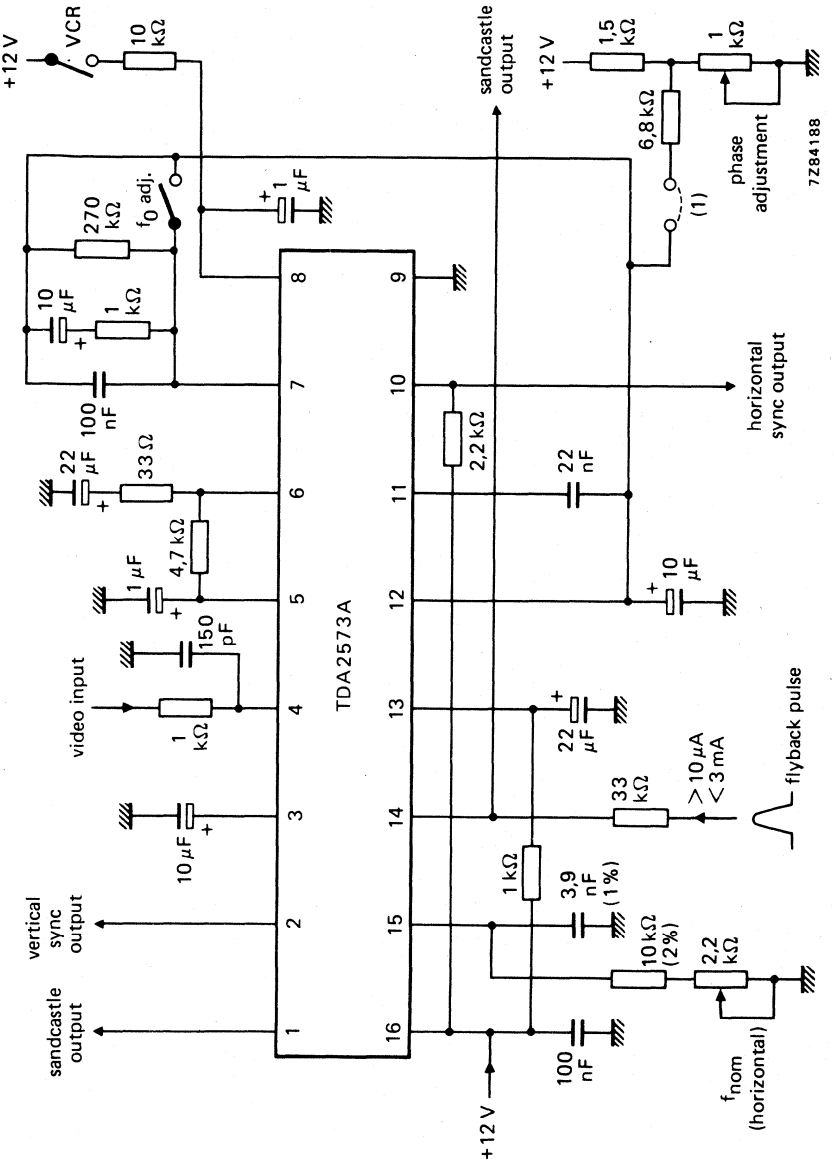
14. Flyback input pulse

    The flyback input pulse is required for the second phase control loop and for generating the line blanking pulse in the sandcastle output. The input current should be at least 10 μA and not exceed 3 mA.

15. RC-network horizontal oscillator

    Stable components should be chosen for a good frequency stability. A part of the total resistance must be variable for adjusting the frequency. This part should be as small as possible, because of poor stability of variable carbon resistors.
    The oscillator can be adjusted when pins 7 and 12 are short-circuited (see Fig. 2).

16. Positive supply: The supply voltage may vary between 10 V and 13,2 V. The current-draw is 53 mA (typical) and a range of 35 to 70 mA at 12 V.



(1) Optional circuit for phase adjustment.

Fig. 2 Application circuit diagram.

HORIZONTAL SYNCHRONIZATION AND VERTICAL 525 DIVIDER SYSTEM

The TDA2575A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2575A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 525.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,5 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (525 divider system), without delay after channel change.

QUICK REFERENCE DATA

Supply voltage				
horizontal	V_{12-11}	typ.	12	V
vertical	V_{16-11}	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2-11(p-p)}$		0,07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8-11(p-p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1-11(p-p)}$	typ.	11	V
Burst-key output pulse (peak-to-peak value)	$V_{13-11(p-p)}$	typ.	11	V

PACKAGE OUTLINES

TDA2575A : 16-lead DIL; plastic (SOT-38).
TDA2575AQ: 16-lead QIL; plastic (SOT-58).

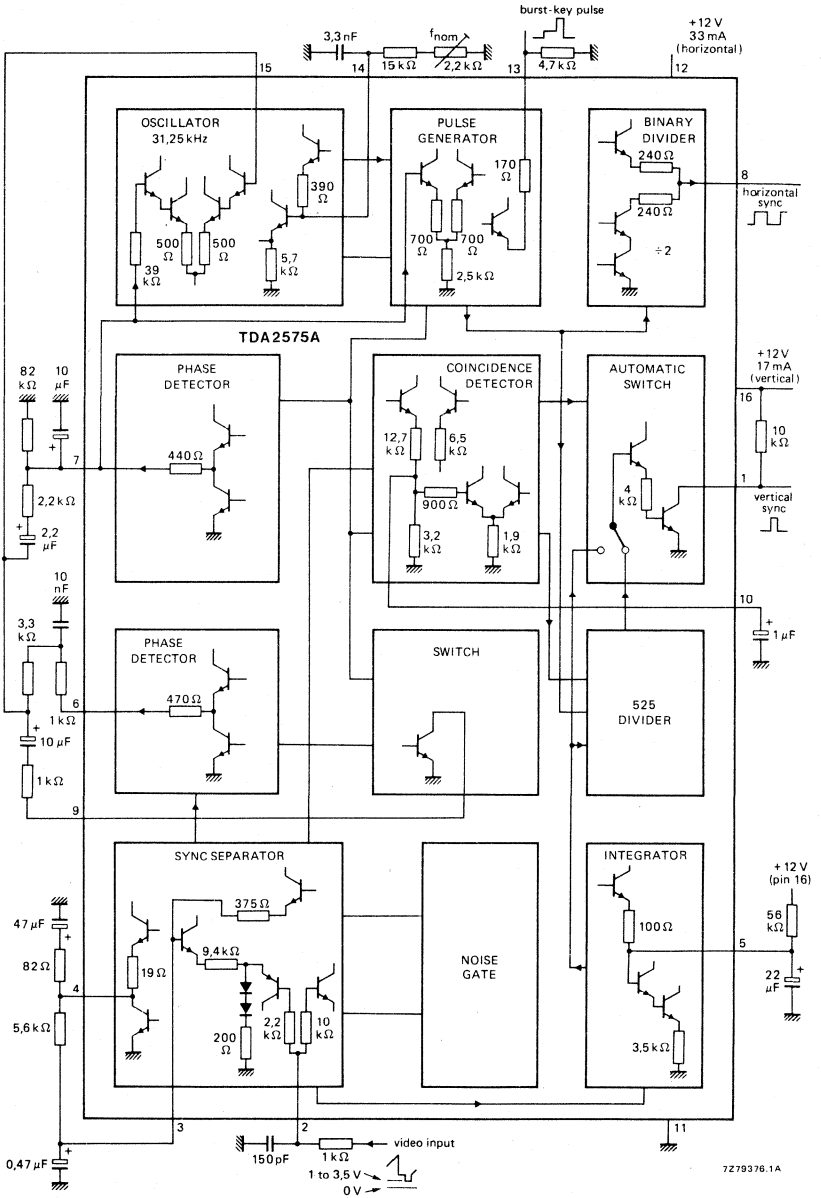


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
horizontal	V_{12-11}	max.	13,2	V
vertical	V_{16-11}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}	−25 to + 130		°C
Operating ambient temperature	T_{amb}	−25 to + 65		°C

CHARACTERISTICS

At V_{12-11} = 12 V; V_{16-11} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Supply voltage range (pins 12 and 16)	V_{12-11}; V_{16-11}	typ.	12	V
			10 to 13,2	V
Current consumption	$I_{12} + I_{16}$	typ.	50	mA
		<	75	mA
Sync separator and noise gate				
Sync pulse amplitude (negative going) peak-to-peak value	$V_{2-11(p-p)}$		0,07 to 1	V *
Top-sync level	V_{2-11}		1,0 to 3,5	V
Slicing level		typ.	50	% **
Slicing level noise gating	V_{2-11}	typ.	0,7	V
Phase locked loop				
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Control sensitivity of phase detector		typ.	1,2	V/μs
Delay between sync input and detector output (pin 6)	t_d	typ.	0,4	μs
Phase modulation due to hum on the supply line		typ.	2,0	μs/V ▲

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

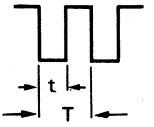
** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 μs/V (p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

CHARACTERISTICS (continued)

Horizontal oscillator				
Frequency; free running	f_o	typ.	31,500	kHz
Frequency at output pin 8	f_8	typ.	15,750	kHz
Spread of frequency without spread of external components	Δf_o	<	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	K^{-1}
Change of frequency when V_{12-11} drops to 6 V	Δf_o	<	10	%
Change of frequency when V_{12-11} increases from 10 to 13,2 V	Δf_o	<	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8-11(p-p)}$	>	10	V
Output resistance	R_{8-11}	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p-p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	% *
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	µs **
Burst-key pulse				
Output voltage (peak-to-peak value)	$V_{13-11(p-p)}$	>	10	V
Duration of upper part of output pulse	t_p	typ.	3,6	µs **
Duration of lower part of output pulse	t_p	typ.	9,1	µs **
Amplitude of lower part of output pulse	$V_{13-11(p-p)}$	typ.	3	V **
Output resistance	R_{13-11}	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_d	typ.	0,9	µs **
Coincidence detector				
Voltage level of time constant switch	V_{10-11}	typ.	2,0	V
Voltage when the oscillator is in sync	V_{10-11}	typ.	0,4	V
Voltage when the oscillator is out-of-sync	V_{10-11}	typ.	2,5	V
Voltage during noise	V_{10-11}	typ.	1,0	V

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1-11(p-p)}$	>	10 V
Duration of output pulse during indirect synchronization	t_p	typ.	170 µs
Duration of output pulse during direct synchronization (coincidence detector high)	t_p	typ.	190 µs
Load resistor to pin 2	R_L	>	2 kΩ
Output voltage low with R_L = 2 kΩ	V_{1-11}	<	500 mV
Ratio between basic horizontal oscillator frequency and vertical pulse			525 *

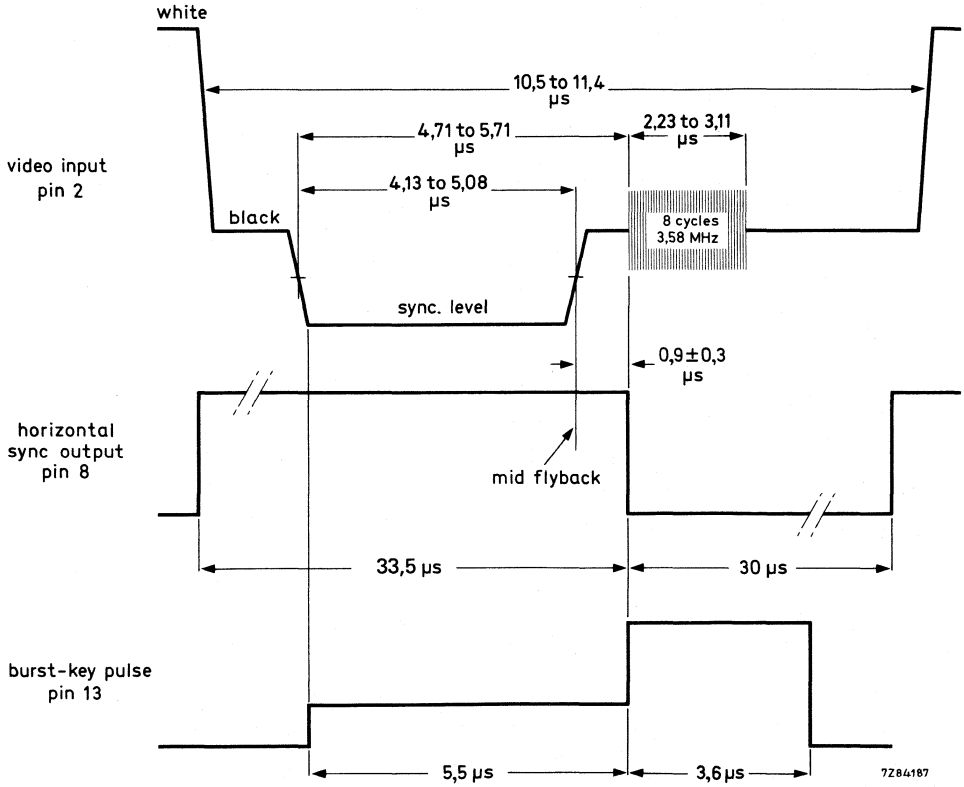


Fig. 2 Relationship between the video input signal to the TDA2575A and the horizontal sync and burst-key pulse output.

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 525 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2575A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; c = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:
    - when in-sync: 0,4 V
    - when out-of-sync: 2,0 V
    - during noise at input: 1,0 V

    When the output voltage $<$ 1,85 V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage $>$ 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

APPLICATION INFORMATION (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

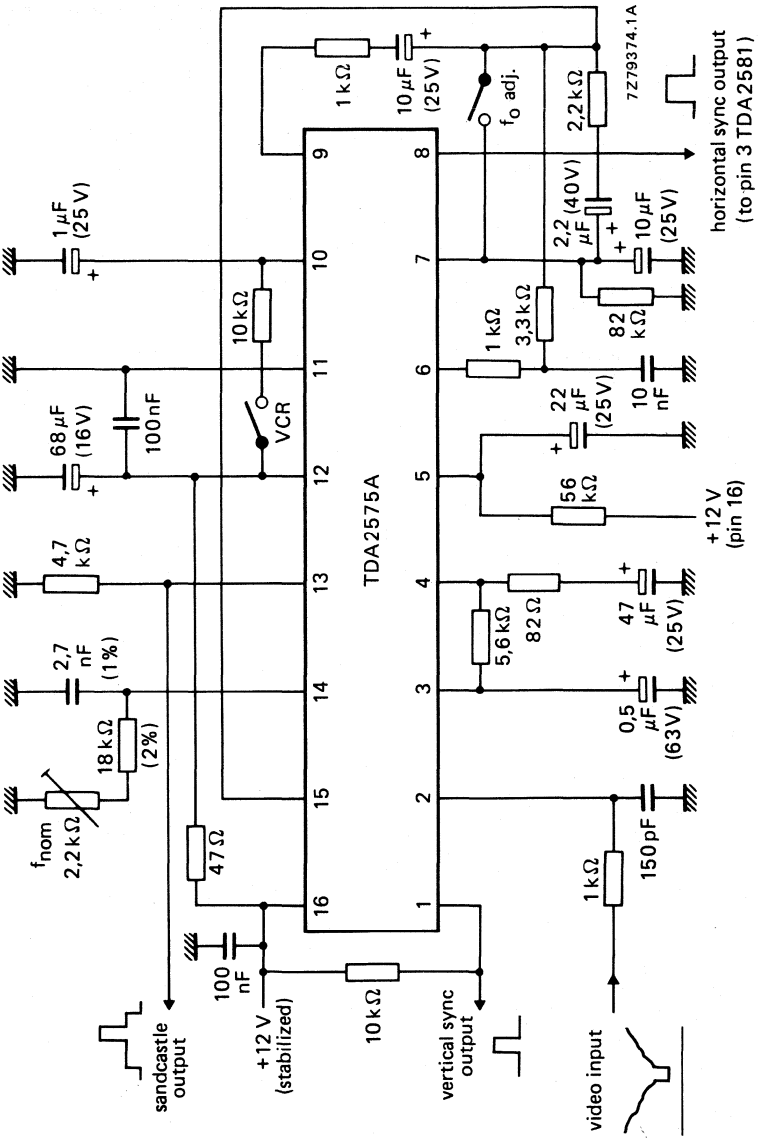


Fig. 3 Typical application circuit diagram; for combination of the TDA2575A with the TDA2581 see Fig. 4.

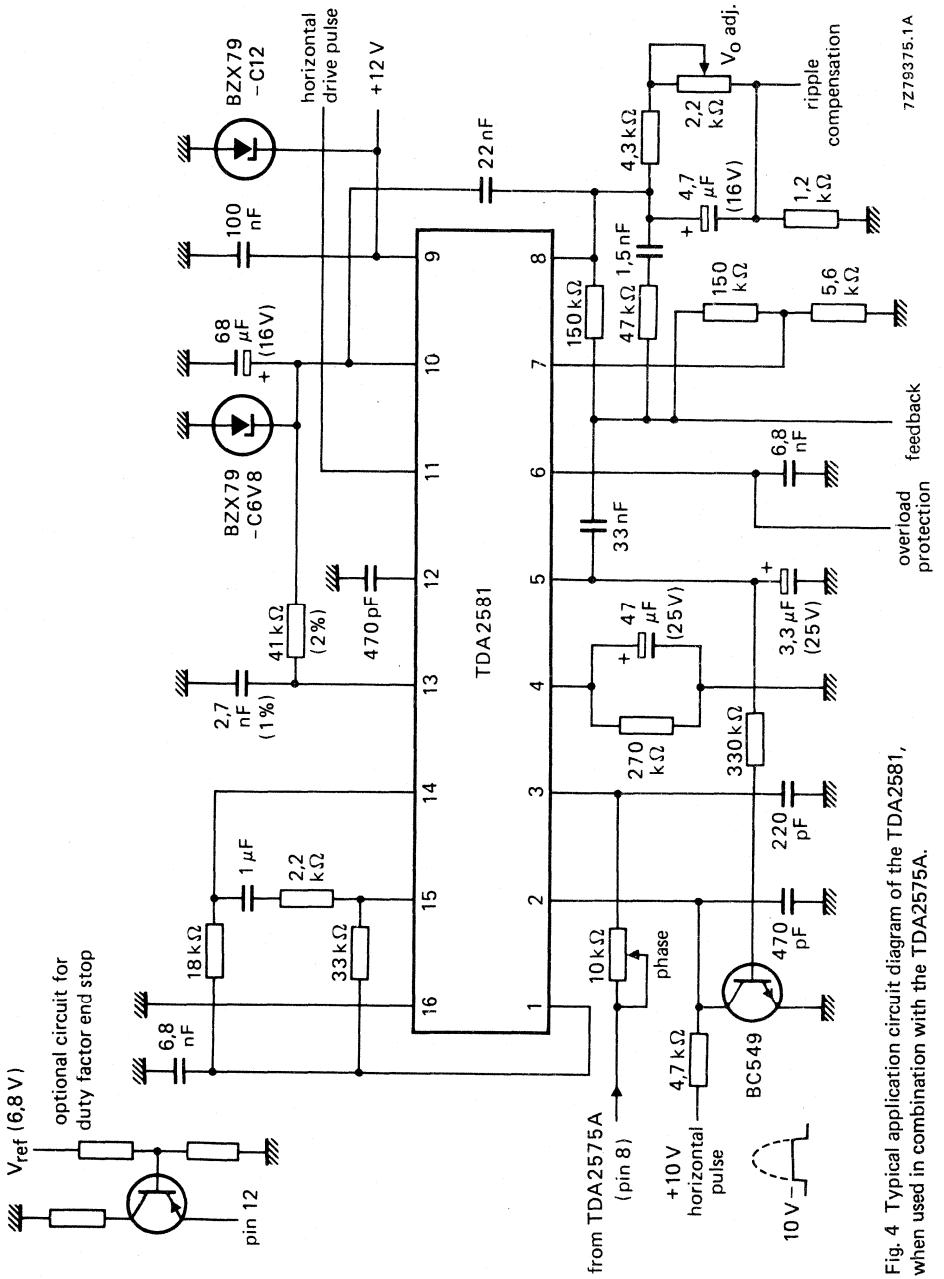


Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2575A.

HORIZONTAL OSCILLATOR COMBINATION WITH VERTICAL DIVIDER

The TDA2576 is a horizontal oscillator combination intended to be used in various types of transistorized line deflection circuits, e.g. switched-mode driven and power-pack system circuits.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Phase detector which compares the sync pulse with the oscillator voltage.
- Phase detector which compares the line flyback pulse with the oscillator voltage.
- Horizontal oscillator.
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals).
- Burst key pulse generator (sandcastle pulse).
- Vertical sync pulse separator.
- Very stable vertical synchronization due to the divider system.

QUICK REFERENCE DATA

Supply voltage	$V_{16\text{-}9}$	typ.	12	V
Supply current consumption	I_{16}	typ.	53	mA
Sync input voltage (peak-to-peak value)	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1	V
Slicing level		typ.	50	%
Control sensitivity sync to flyback		typ.	6	kHz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{10\text{-}9(p\text{-}p)}$	typ.	11	V
Vertical output pulse; pin 1 (peak-to-peak value)	$V_{1\text{-}9(p\text{-}p)}$	typ.	11	V
Vertical output pulse; pin 2 (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	typ.	10	V
Sandcastle output pulse (peak-to-peak value)	$V_{14\text{-}9(p\text{-}p)}$	typ.	11	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

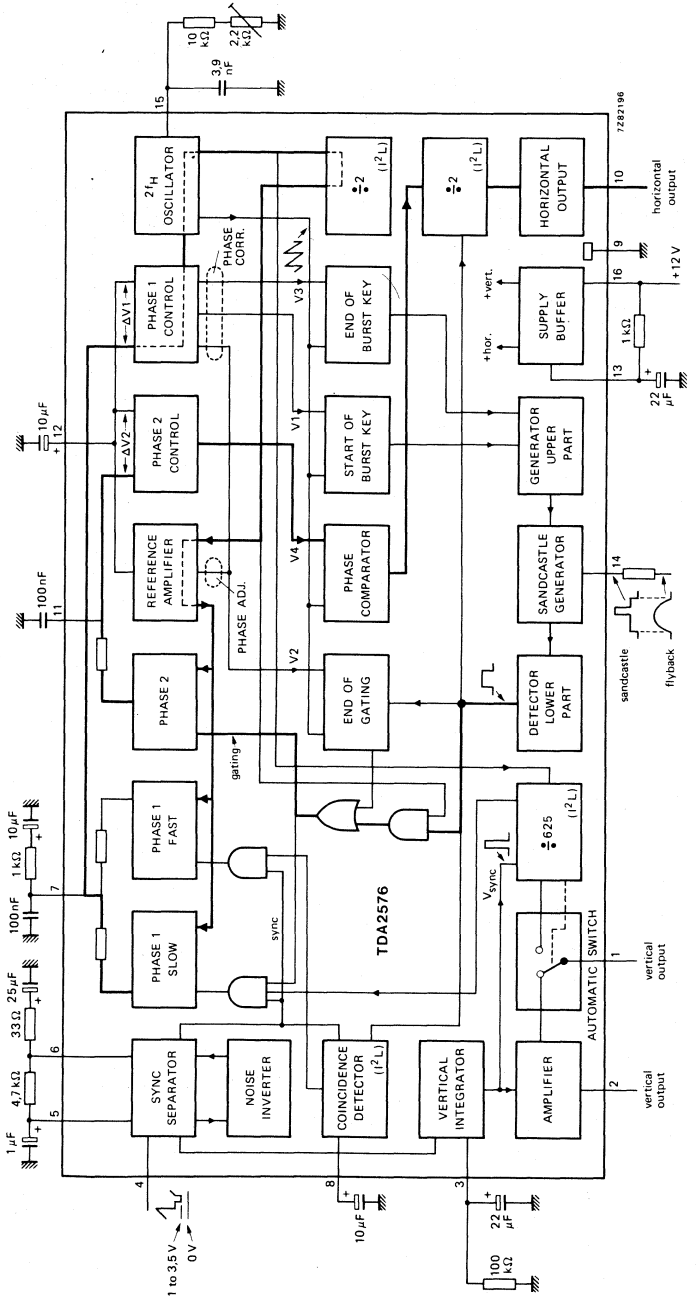


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{16\text{-}9}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 65 °C

CHARACTERISTICS

$V_{16\text{-}9}$ = 12 V; T_{amb} = 25 °C; measured in Fig. 2.

Supply voltage	$V_{16\text{-}9}$	typ.	12 V
			8 to 13,2 V
Supply current consumption	I_{16}	typ.	53 mA
		<	70 mA
Sync separator and noise gate			
Sync pulse amplitude (negative going) peak-to-peak value	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1 V*
Top-sync level	$V_{4\text{-}9}$		1,0 to 3,5 V
Slicing level noise gate	$V_{4\text{-}9}$	<	1 V
Delay between sync input and detector output (pin 7)		typ.	0,35 µs
First control loop (sync-to-oscillator)			
Holding range	Δf	typ.	± 1000 Hz
Catching range	Δf	typ.	± 900 Hz
Control sensitivity video			
with respect to oscillator		typ.	1,2 kHz/µs
with respect to sandcastle		typ.	5,0 kHz/µs
with respect to flyback pulse		typ.	6,0 kHz/µs
Second control loop (oscillator-to-flyback)			
Control sensitivity	$\Delta t_d/\Delta t_o$	typ.	20 **
Control range	t_d	<	18 µs

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (I_7).

CHARACTERISTICS (continued)

Horizontal oscillator			
Frequency; free running	f_o	typ.	31,250 kHz
Frequency at output pin 10	f_{10}	typ.	15,625 kHz
Spread of frequency without spread of external components	Δf_o	<	4 %
Temperature coefficient	T	typ.	$2{,}5 \times 10^{-4}$
Change of frequency when $V_{16\text{-}9}$ increases from 10 to 13,2 V	Δf_o	<	0,5 %
Minimum supply voltage (+ hor. see Fig. 1)		typ.	6 V
Frequency deviation at min. supply voltage		<	10 %
Horizontal output (pin 10)			
Maximum supply voltage		<	13,2 V
Minimum output voltage at a current of 20 mA	$V_{10\text{-}9}$	<	500 mV
Maximum output current	I_{10}	typ.	60 mA
Sandcastle pulse (pin 14)			
Output voltage during burst key pulse	$V_{14\text{-}9}$	<	10 V
Pulse duration	t_p	typ.	3,6 µs
Amplitude of lower part of output pulse	$V_{14\text{-}9}$	typ.	4,5 V
Pulse duration	flyback pulse		
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the flyback pulse		typ.	1,5 µs
Input current	I_{14}	<	20 mA
Phase adjustment (pin 12)			
Voltage at pin 12	$V_{12\text{-}9}$	typ.	2,8 V
Control sensitivity		typ.	0,6 V/µs
Control range		typ.	± 1 µs
Coincidence detector (pin 8)			
Voltage level of time constant switch	$V_{8\text{-}9}$	typ.	2,1 V
Voltage when the oscillator is in sync	$V_{8\text{-}9}$	typ.	1,2 V
Voltage when the oscillator is out-of-sync	$V_{8\text{-}9}$	typ.	2,5 V
Voltage during noise	$V_{8\text{-}9}$	typ.	1,7 V

Vertical outputs

Output voltage (peak-to-peak value)	$V_{1\text{-}9(p\text{-}p)}$	>	10 V
Output current	I_1	<	5 mA
Duration of output pulse during indirect synchronization; 21 lines	t_p	typ.	1,34 ms
Output voltage (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	>	9 V
Output current	I_2	<	2 mA

APPLICATION INFORMATION (see also Fig. 2)

The function is described against the corresponding pin number

1. Vertical output pulse

   This pulse is obtained from the divider circuit, the amplitude is in excess of 10 V peak-to-peak. This pulse has a duration of 1,34 ms (21 lines) when standard signals are received. The pulse is obtained from the vertical sync pulse integrator during non-standard signals and has a duration of about 150 μs. It has good stability and accuracy, so it is intended to be used for triggering the vertical oscillator and blanking the video signal (e.g. teletext signals).

2. Vertical output pulse

   This pulse is directly obtained from the vertical sync pulse separator. The amplitude is in excess of 9 V peak-to-peak. It can be used for search tuning purposes.

3. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 100 kΩ; C = 22 μF.

4. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,1 to 1 V peak-to-peak. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 100 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 1 V (typ. 0,7 V), thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

5. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 6. The capacitor connected to pin 5 must be about 1 μF.

6. Black level detector output

   The black level of the input signal is detected on this pin. A capacitor of 22 μF in series with a resistor of 33 Ω has to be connected to this pin. A 4,7 kΩ resistor must be connected between pins 5 and 6.

APPLICATION INFORMATION (continued)

7. Horizontal phase detector output and control oscillator input

   The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 7 and 12.
   The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out of sync. The result is a large catching range, and the phase detector is not gated in that condition. The output current is low when the oscillator is synchronized and the phase detector is gated. A good noise immunity is obtained in this case.

8. Coincidence detector output

   A 10 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
   The following output voltages can occur:
   - when in-sync 1,2 V
   - when out-of-sync 2,5 V
   - during noise at the input 1,7 V

   When the output voltage $< 2,1$ V, the phase detector output current is low and the phase detector is gated. A good noise immunity is obtained in this case. For a voltage $> 2,1$ V, the output current of the phase detector is high and the phase detector is not gated. This results in a large catching range and a high dynamical steepness of the PLL. This latter condition is required during VCR-playback. It can be obtained by connecting pin 8 to the positive supply line via a resistor of 10 kΩ.

9. Negative supply (ground)

10. Horizontal output

    This is an open collector output. The collector resistor must be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The output stage is designed such that the line output transistor cannot be switched-on during flyback. Switching-on occurs directly after the flyback pulse to avoid linearity errors. The duty factor of the output pulse depends on the delay in the output stage (correction via the second control loop).

11. Control voltage second loop

    This voltage controls the start of the output pulse at pin 10 (positive-going edge). The capacitor connected to this pin must have a value of about 100 nF.
    A resistor of 270 kΩ should be connected between pins 11 and 12 for safe operation.

12. Reference voltage control loops

    The reference voltage must be decoupled by means of a capacitor of about 10 μF.
    It is possible to obtain a phase shift between video and flyback pulse by changing this reference voltage externally. The possible phase shift is ± 1 μs.
    The required voltage change is ± 0,6 V.

13. Decoupling internal power supply

    The IC has two power supply terminals. The main terminal (pin 16) supplies the output stages, the sync separator and the divider circuit. The specially decoupled supply terminal (pin 13) supplies the horizontal oscillator. This is to avoid coupling of the video signal into the oscillator part. The capacitor connected to pin 13 should have a value of about 22 μF. The resistor connected between pins 13 and 16 should have a value of about 1 kΩ.

14. Flyback input/sandcastle output

This pin combines two functions e.g.:
- Input for the line flyback pulse, which is required for the second phase control loop.
- Generation of a sandcastle pulse. The flyback pulse has to be applied to pin 14 via a suitable series resistance. The amplitude of the flyback pulse must be about 100 V peak to peak. The pulse is clamped to a level of 4,5 V at the input of the IC. This level is increased to the supply voltage during the burst gate pulse.

15. RC-network horizontal oscillator

Stable components should be chosen for a good frequency stability. A part of the total resistance must be variable for adjusting the frequency. This part should be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be asjusted when pins 7 and 12 are short-circuited, or when pins 5 and 8 are connected to ground (see Fig. 2).

16. Positive supply

The supply voltage may vary between 8 V and 13,2 V. The current-draw is 53 mA (typical) and a range of 35 to 70 mA at 12 V.

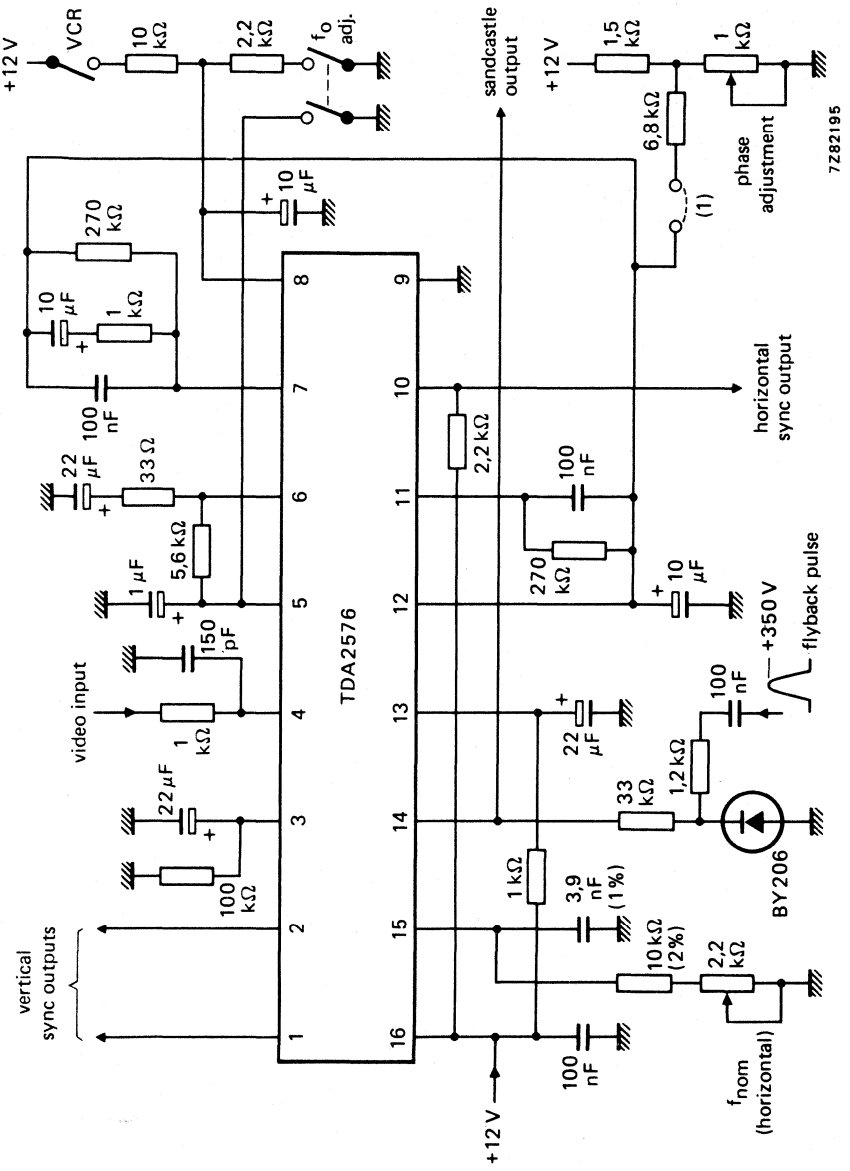


Fig. 2 Application circuit diagram.

(1) Optional circuit for phase adjustment.

HORIZONTAL OSCILLATOR COMBINATION WITH VERTICAL 625 DIVIDER SYSTEM

The TDA2576A is a horizontal oscillator combination intended to be used in various types of transistorized horizontal deflection circuits, e.g. switched-mode driven and power-pack system circuits.

The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Phase detector which compares the sync pulse with the oscillator voltage; this phase detector is gated.
- Phase detector which compares the line flyback pulse with the oscillator voltage.
- Horizontal oscillator (31,25 kHz).
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals).
- Burst key pulse generator (sandcastle pulse with three levels).
- Vertical sync pulse separator.
- Very stable vertical synchronization due to the 625 divider system, without delay after channel change.

QUICK REFERENCE DATA

Supply voltage	$V_{16\text{-}9}$	typ.	12	V
Supply current consumption	I_{16}	typ.	53	mA
Sync input voltage (peak-to-peak value)	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1	V
Slicing level		typ.	50	%
Control sensitivity sync to flyback		typ.	10	kHz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{10\text{-}9(p\text{-}p)}$	typ.	11	V
Vertical output pulse; pin 2 (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	typ.	11	V
Sandcastle output pulse (peak-to-peak value)	$V_{14\text{-}9(p\text{-}p)}$	typ.	11	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

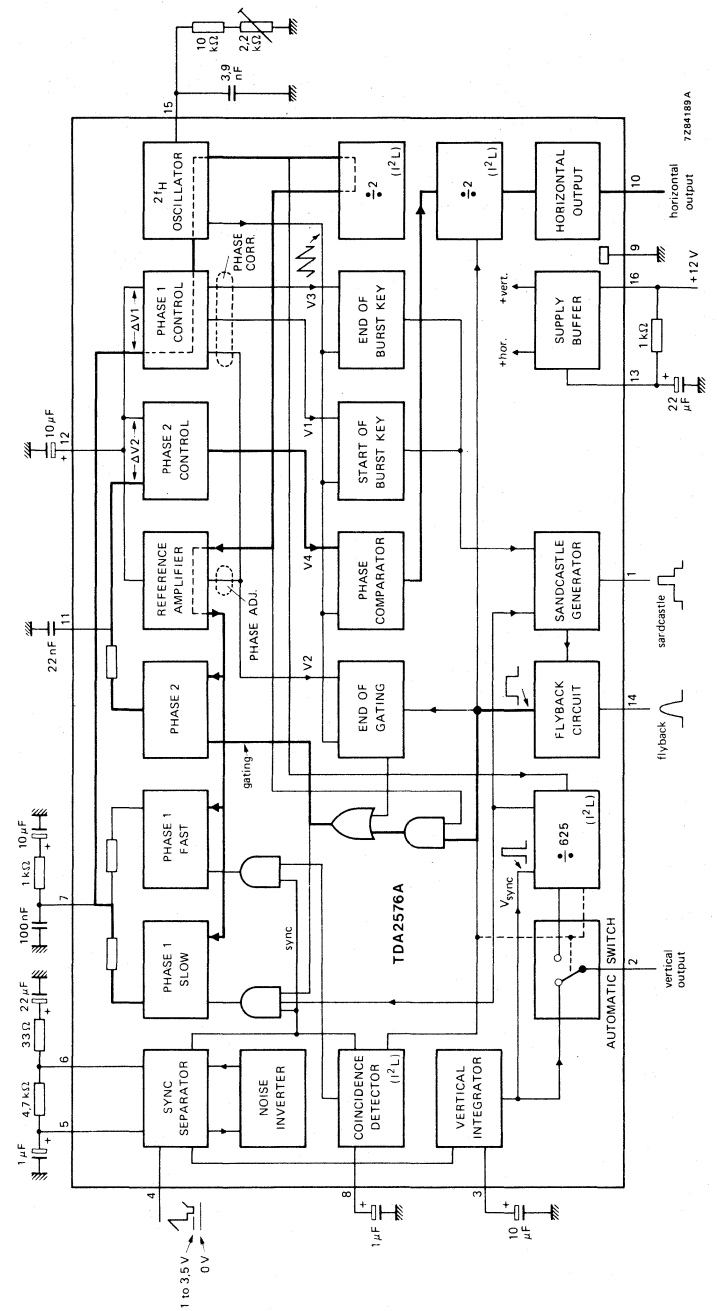


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{16-9}	max.	13,2 V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 65 °C

CHARACTERISTICS

V_{16-9} = 12 V; T_{amb} = 25 °C; measured in Fig. 2.

Supply voltage	V_{16-9}	typ.	12 V
			10 to 13,2 V
Supply current consumption	I_{16}	typ.	53 mA
		<	70 mA
Sync separator and noise gate			
Sync pulse amplitude (negative going) peak-to-peak value	$V_{4-9(p-p)}$		0,1 to 1 V*
Top-sync level	V_{4-9}		1,0 to 3,5 V
Slicing level noise gate	V_{4-9}	<	1 V
Delay between sync input and detector output (pin 7)		typ.	0,35 µs
First control loop (sync-to-oscillator)			
Holding range	Δf	typ.	± 1000 Hz
Catching range	Δf	typ.	± 900 Hz
Control sensitivity video			
with respect to oscillator		typ.	2,0 kHz/µs
with respect to sandcastle		typ.	10,0 kHz/µs
with respect to flyback pulse		typ.	10,0 kHz/µs
Phase modulation due to hum on the supply line (pin 16)		<	1,0 µs/V**
Second control loop (oscillator-to-flyback)			
Control sensitivity	$\Delta t_d/\Delta t_o$	typ.	250 ▲
Control range	t_d	<	26 µs

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** This voltage is a peak-to-peak value.

▲ t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (I_7).

CHARACTERISTICS (continued)

Horizontal oscillator			
Frequency; free running	f_o	typ.	31,250 kHz
Frequency at output pin 10	f_{10}	typ.	15,625 kHz
Spread of frequency without spread of external components	Δf_o	<	4 %
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$
Change of frequency when V_{16-9} increases from 10 to 13,2 V	Δf_o	<	0,5 %
Minimum supply voltage (+ hor. see Fig. 1)		typ.	7 V
Frequency deviation at min. supply voltage		<	10 %
Horizontal output (pin 10)			
Maximum supply voltage		<	13,2 V
Minimum output voltage at a current of 60 mA	V_{10-9}	<	700 mV
Maximum output current	I_{10}	<	60 mA
Duration of the output pulse	t_p		12 to 38 µs
Sandcastle pulse (pin 1)			
Output voltage during burst key pulse	V_{1-9}	>	10 V
Pulse duration	t_p	typ.	4,0 µs
Amplitude of second level of output pulse	V_{1-9}	typ.	4,5 V
Pulse duration	flyback pulse		
Amplitude of third level of output pulse	V_{1-9}	typ.	2,5 V
Pulse duration	t_p	typ.	1,34 µs*
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the burst key pulse	t_d	typ.	4,9 µs
Phase adjustment (pin 12)			
Voltage at pin 12	V_{12-9}	typ.	2,8 V
Control sensitivity		typ.	0,6 V/µs
Control range		typ.	± 1 µs
Coincidence detector (pin 8)			
Voltage level of time constant switch	V_{8-9}	typ.	2,1 V
Voltage when the oscillator is in sync	V_{8-9}	typ.	1,2 V
Voltage when the oscillator is out-of-sync	V_{8-9}	typ.	2,6 V
Voltage during noise	V_{8-9}	typ.	1,7 V

* During standard video signals.

Flyback input pulse (pin 14)			
Switching level	V_{14-9}	typ.	0,7 V
Input pulse	V_{14-9}	<	12 V
Input resistance		typ.	2,5 kΩ
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the flyback pulse	t_p	typ.	1,5 μs
Vertical outputs			
Output voltage (peak-to-peak value)	$V_{2-9(p-p)}$	>	10 V
Output current	I_2	<	5 mA
Output voltage low at I_2 = 5 mA	V_{2-9}	<	500 mV
Duration of output pulse during indirect synchronization	t_p	typ.	190 μs
Duration of output pulse during direct synchronization	t_p	typ.	160 μs
Ratio between basic horizontal oscillator frequency and vertical pulse			625 *

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 2; the pulse of the divider circuit is switched off.

APPLICATION INFORMATION (see also Fig. 2)

The function is described against the corresponding pin number

1. Sandcastle output pulse

   This output pulse has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level for the line blanking is typ. 4,5 V with a pulse duration equal to the line flyback pulse. The third level (typ. 2,5 V) is used for frame blanking and has a duration of typ. 1,34 ms (21 lines). This last pulse is only available with a standard video input signal. Under all other conditions, an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by means of an internal clamping circuit. The input current is typ. 2 mA.

2. Vertical output pulse

   This pulse is obtained from the divider circuit, the amplitude is in excess of 10 V peak-to-peak. This pulse has a duration of 190 μs when standard signals are received. The pulse is obtained from the vertical sync pulse integrator during non-standard signals and has a duration of about 160 μs. It has good stability and accuracy, so it is intended to be used for triggering the vertical oscillator.

3. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor with an internal resistor are required for the correct biasing of this circuit for various input conditions. A typical value for the capacitor is 10 μF.

4. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,1 to 1 V peak-to-peak. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 100 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 1 V (typ. 0,7 V), thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

5. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 6. The capacitor connected to pin 5 must be about 1 μF.

6. Black level detector output

   The black level of the input signal is detected on this pin. A capacitor of 22 μF in series with a resistor of 33 Ω has to be connected to this pin. A 4,7 kΩ resistor must be connected between pins 5 and 6.

7. Horizontal phase detector output and control oscillator input

   The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 7 and 12.
   The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out of sync. The result is a large catching range, and the phase detector is not gated in that condition. The output current is low when the oscillator is synchronized and the phase detector is gated. A good noise immunity is obtained in this case.

8 Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
The following output voltages can occur:
– when in-sync 1,2 V
– when out-of-sync 2,6 V
– during noise at the input 1,7 V

When the output voltage $<$ 2,1 V, the phase detector output current is low and the phase detector is gated. A good noise immunity is obtained in this case. For a voltage $>$ 2,1 V, the output current of the phase detector is high and the phase detector is not gated. This results in a large catching range and a high dynamical steepness of the PLL. This latter condition is required during VCR-playback. It can be obtained by connecting pin 8 to the positive supply line via a resistor of 10 kΩ. The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

9. Negative supply (ground)

10. Horizontal output

This is an open collector output. The collector resistor must be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The output stage is designed such that the line output transistor cannot be switched-on during flyback. Switching-on occurs directly after the flyback pulse to avoid linearity errors. The duty factor of the output pulse depends on the delay in the output stage (correction via the second control loop).

11. Control voltage second loop

This voltage controls the start of the output pulse at pin 10 (positive-going edge). The capacitor connected to this pin must have a value of about 22 nF.

12. Reference voltage control loops

The reference voltage must be decoupled by means of a capacitor of about 10 μF.
It is possible to obtain a phase shift between video and flyback pulse by changing this reference voltage externally. The possible phase shift is $\pm$ 1 μs.
The required voltage change is $\pm$ 0,6 V.

13. Decoupling internal power supply

The IC has two power supply terminals. The main terminal (pin 16) supplies the output stages, the sync separator and the divider circuit. The specially decoupled supply terminal (pin 13) supplies the horizontal oscillator. This is to avoid coupling of the video signal into the oscillator part. The capacitor connected to pin 13 should have a value of about 22 μF. The resistor connected between pins 13 and 16 should have a value of about 1 kΩ.

14. Flyback input pulse

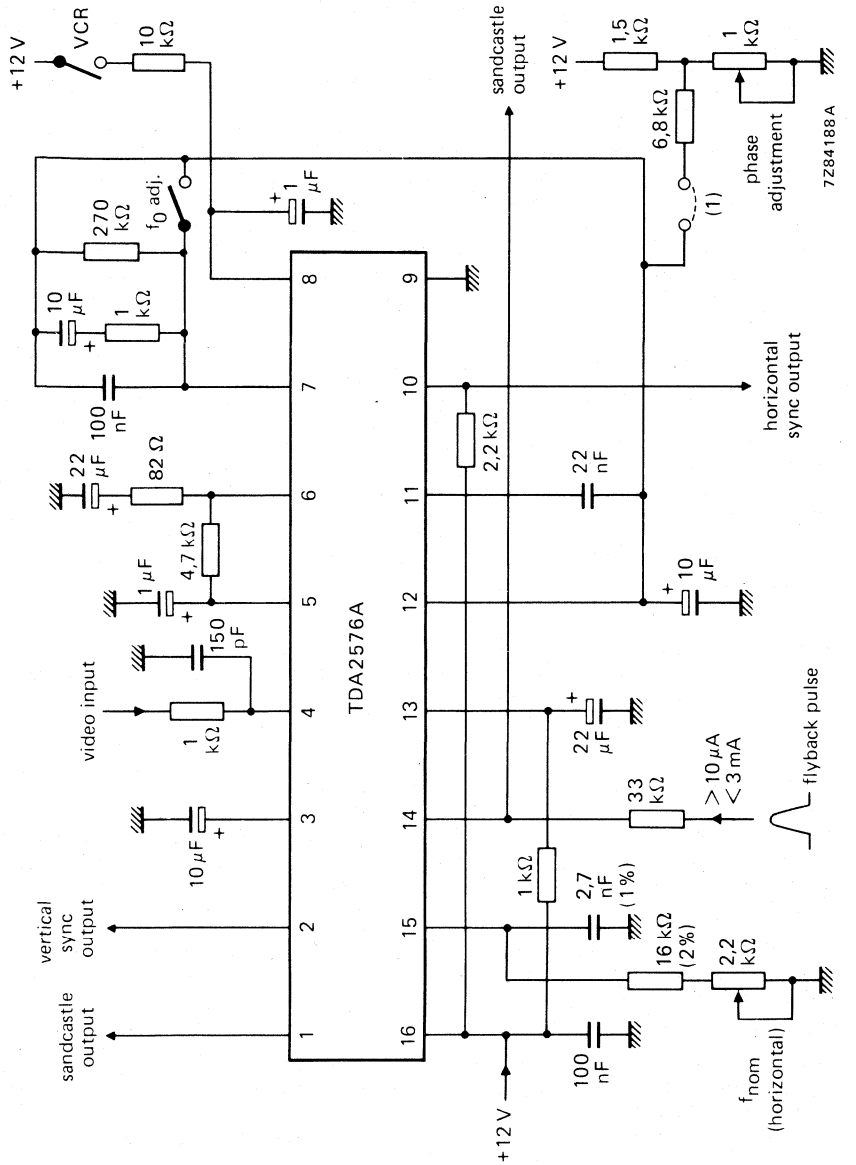
The flyback input pulse is required for the second phase control loop and for generating the line blanking pulse in the sandcastle output. The input current should be at least 10 μA and not exceed 3 mA.

15. RC-network horizontal oscillator

Stable components should be chosen for a good frequency stability. A part of the total resistance must be variable for adjusting the frequency. This part should be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be adjusted when pins 7 and 12 are short-circuited (see Fig. 2).

16. Positive supply: The supply voltage may vary between 10 V and 13,2 V. The current-draw is 53 mA (typical) and a range of 35 to 70 mA at 12 V.

DEVELOPMENT SAMPLE DATA



(1) Optional circuit for phase adjustment.

Fig. 2 Application circuit diagram.

CONTROL CIRCUIT FOR SMPS

The TDA2581 is a monolithic integrated circuit for controlling switched-mode power supplies (SMPS) which are provided with the drive for the horizontal deflection stage.

The circuit features the following:
- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the positive-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.

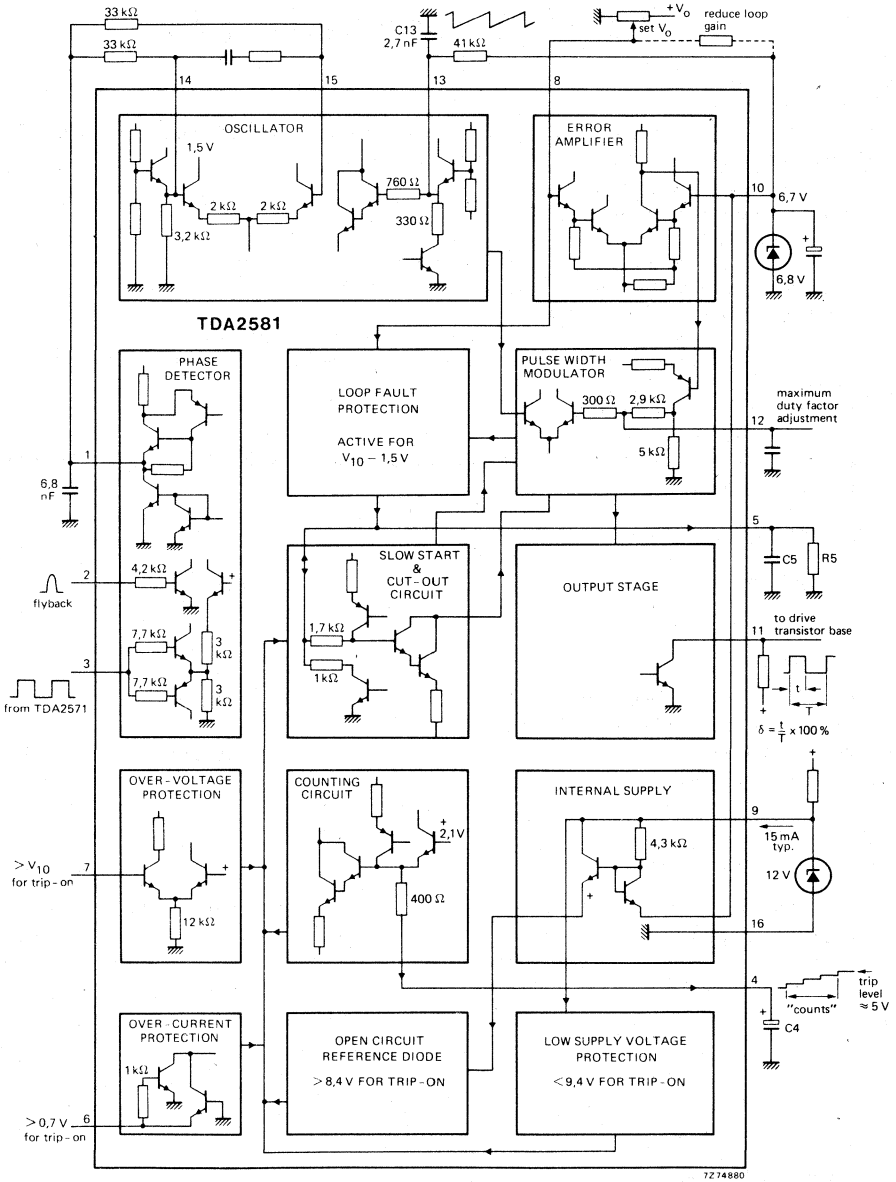
QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12	V
Supply current	I_9	typ.	15	mA
Input signals				
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	11	V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$	typ.	5	V
External reference voltage	$V_{10\text{-}16}$	typ.	6,7	V
Output signals				
Duty factor of output pulse	δ	$>$	0	%
		$<$	98 ± 0,6	%
Output voltage at $I_O < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8	V
Output current (peak value)	I_{11M}	$<$	40	mA

PACKAGE OUTLINES

TDA2581: 16-lead DIL; plastic (SOT-38).
TDA2581Q: 16-lead QIL; plastic (SOT-58).

BLOCK DIAGRAM



Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{9\text{-}16}$	max.	14 V
Voltage at pin 11	$V_{11\text{-}16}$		0 to 14 V
Output current	I_{11}	max.	40 mA
Total power dissipation	P_{tot}	max.	340 mW
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +80 °C

CHARACTERISTICS

$V_{9\text{-}16}$ = 12 V; $V_{10\text{-}16}$ = 6,7 V; T_{amb} = 25 °C; measured in the circuit on page 2

Supply voltage range	$V_{9\text{-}16}$	typ.	12 V 10 to 14 V
Protection voltage too low supply voltage	$V_{9\text{-}16}$	typ.	9,4 V 8,6 to 9,9 V
Supply current at δ = 50%	I_9	typ.	15 mA
Supply current during protection	I_9	typ.	15 mA
Minimum required supply current	I_9	<	18,5 mA*
Power consumption	P	typ.	180 mW
Required input signals			
Reference voltage	$V_{10\text{-}16}$	typ.	6,7 V 5,6 to 7,5 V**
High reference voltage protection: threshold voltage	$V_{10\text{-}16}$	typ.	8,4 V 7,9 to 8,9 V
Feedback input impedance at pin 8	$\lvert Z_{8\text{-}16}\rvert$	typ.	200 kΩ
Horizontal drive pulse (square-wave or differentiated; negative transient is reference) peak-to-peak value	$V_{3\text{-}16(p\text{-}p)}$	typ.	11 V 5 to 12 V
Flyback pulse or differential deflection current	$V_{2\text{-}16}$		1 to 5 V
Over-current protection: threshold voltage	$-V_{6\text{-}16}$	typ.	640 mV 690 to 695 mV▲
	$+V_{6\text{-}16}$	typ.	680 mV 640 to 735 mV▲
Over-voltage protection: threshold voltage	$V_{7\text{-}16}$	typ. $V_{10\text{-}16}$	$V_{10\text{-}16}$ −60 mV −130 to $V_{10\text{-}16}$ −0 mV

* This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9\text{-}16}$ = 10 V; $V_{10\text{-}16}$ = 6,8 V; δ = 50%.

** Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.

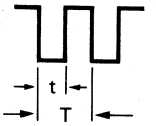
▲ This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Remote control voltage; switch off	$V_{4\text{-}16}$	>	5,8 V*
switch on	$V_{4\text{-}16}$	<	4,5 V*
Delivered output signals			
Horizontal drive pulse (loaded with a resistor of 560 Ω to +12 V) peak-to-peak value	$V_{11\text{-}16(p\text{-}p)}$	>	11,6 V
Output current; peak value	I_{11M}	<	40 mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ. <	200 mV 400 mV
at I_{11} = 40 mA	V_{CEsat}	<	525 mV
Duty factor of output pulse**	δ	> < 98 ± 0,6	0 % %
Charge current for capacitor on pin 4	I_4	typ.	120 μA
Charge current for capacitor on pin 5	I_5	typ.	130 μA
Supply current for reference	I_{10}	typ. 0,6 to 1,45	1 mA mA
Oscillator			
Temperature coefficient		typ. <	−300 ppm/°C −400 ppm/°C
Relative frequency deviation for $V_{10\text{-}16}$ changing from 6 to 7 V		typ. ⩽	−1,5 % −2 %
Oscillator frequency spread (with fixed external components)		⩽	±3 %
Frequency control sensitivity at pin 15		typ.	4,5 kHz/V▲
Phase control loop			
Loop gain of APC-system (automatic phase control)		typ.	5 kHz/μs
Catching range	Δf	typ.	±1,5 kHz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1 μs
Tolerance of phase relation	Δt	⩽	±0,4 μs

* See pin 4 on pages 7 and 8.

** The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

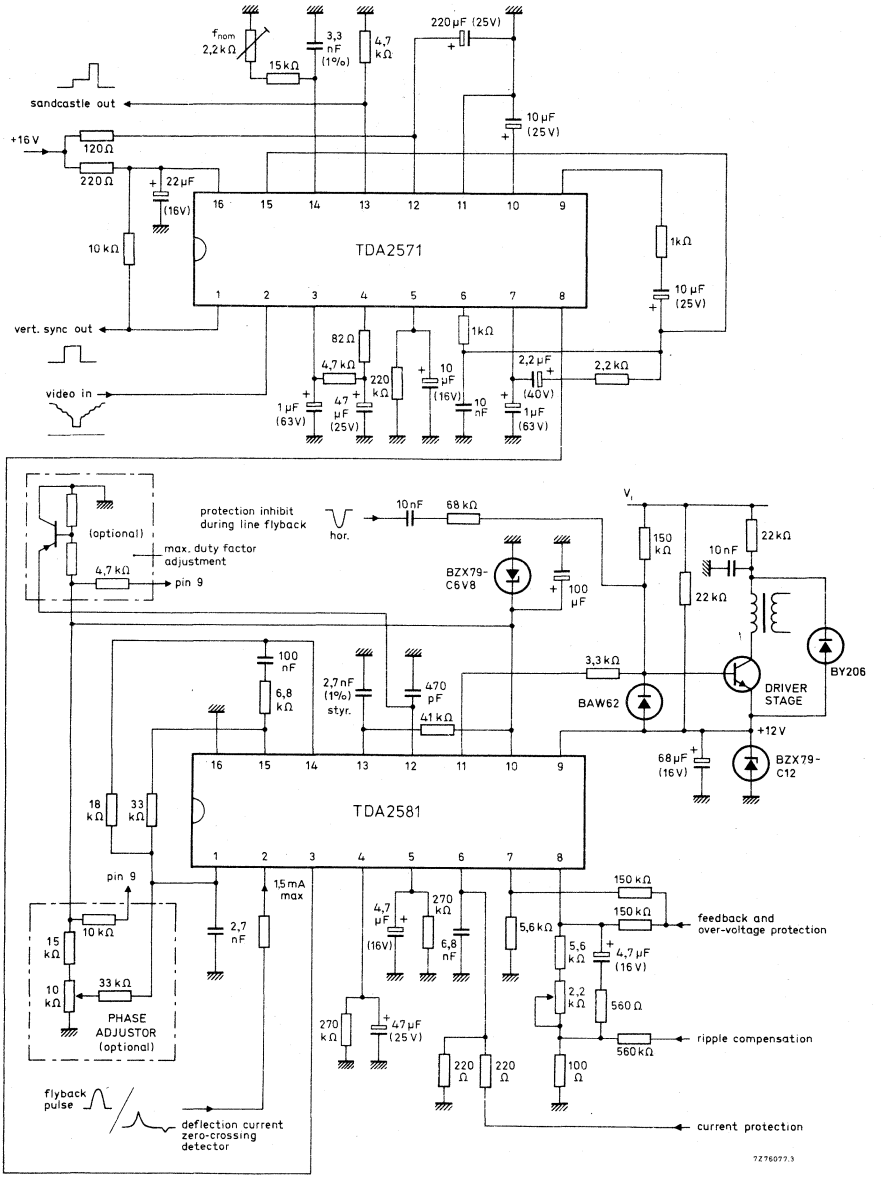
The maximum duty factor value can be set to a desired value (see application information pin 12 on page 9).

▲ For component values see circuit diagram on page 2.

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

APPLICATION INFORMATION



The TDA2571 and TDA2581 controlling an SMPS driver stage.

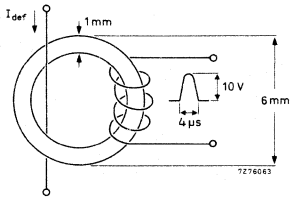
The function is quoted against the corresponding pin number

1. Phase detector output

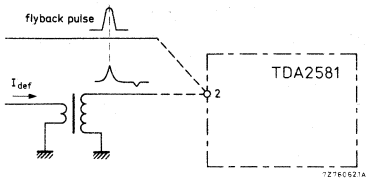
The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the reference signal on pin 3 is delivered by the TDA2571.
With a resistor of 18 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs.

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).



(a)



(b)

The toroidal transformer in (a) is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in (b).

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 10 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}8$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in the graph on page 10.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level, the protection circuit will operate. When this function is not used, pin 7 should be connected to pin 16.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the graphs on pages 10 and 11.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 7,5 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A low voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of a p-n-p transistor used as a voltage source.
The graph on page 10 plots the maximum duty factor as a function of the voltage applied to pin 12.
If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%.
This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

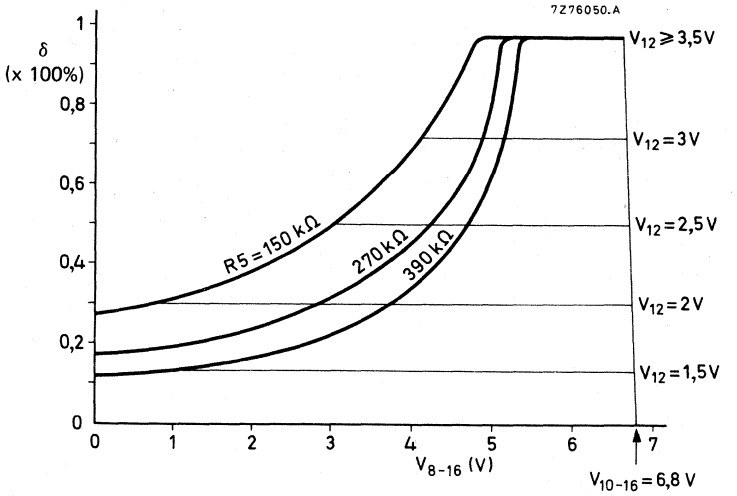
14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,5 V for reference voltage $V_{10\text{-}16}$ = 6,7 V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

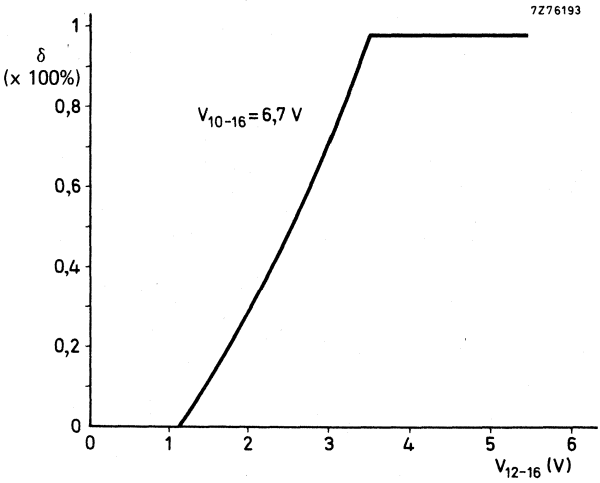
15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15.
Control sensitivity is typically 4,5 kHz/V.

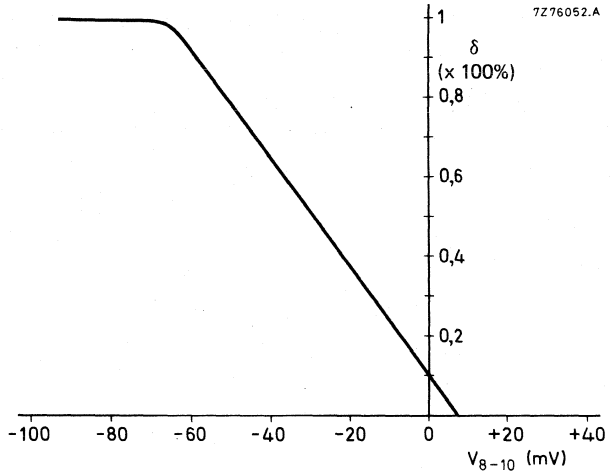
16. Negative supply (ground)



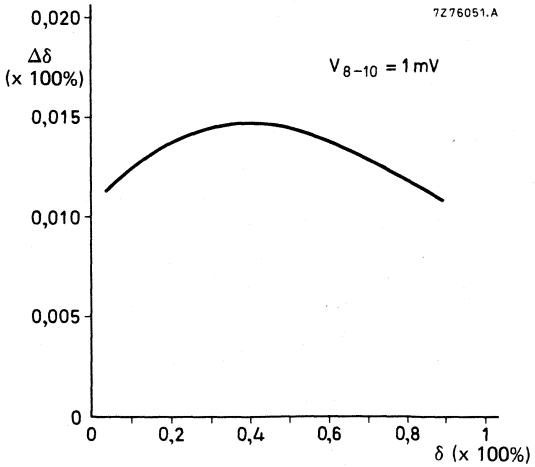
Duty factor of output pulses as a function of V_{8-16} with R5 as a parameter, and with V_{12} as a limiting value; V_{10-16} = 6,8 V.



Maximum duty factor limitation as a function of V_{12-16}.



Duty factor of output pulses as a function of error amplifier input (V_{8-10}).



Change in duty factor of output pulses for a 1 mV error amplifier input change (V_{8-10}) as a function of initial duty factor.

CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12 V
Supply current	I_9	typ.	14 mA
Input signals			
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 11 V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$		1 to 5 V
External reference voltage	$V_{10\text{-}16}$	typ.	6,1 V
Output signals			
Duty factor of output pulse	δ	$>$	0 %
		$<$	98 ± 0,8 %
Output voltage at $I_o < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8 V
Output current (peak value)	I_{11M}	$<$	40 mA

PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT-38).
TDA2582Q: 16-lead QIL; plastic (SOT-58).

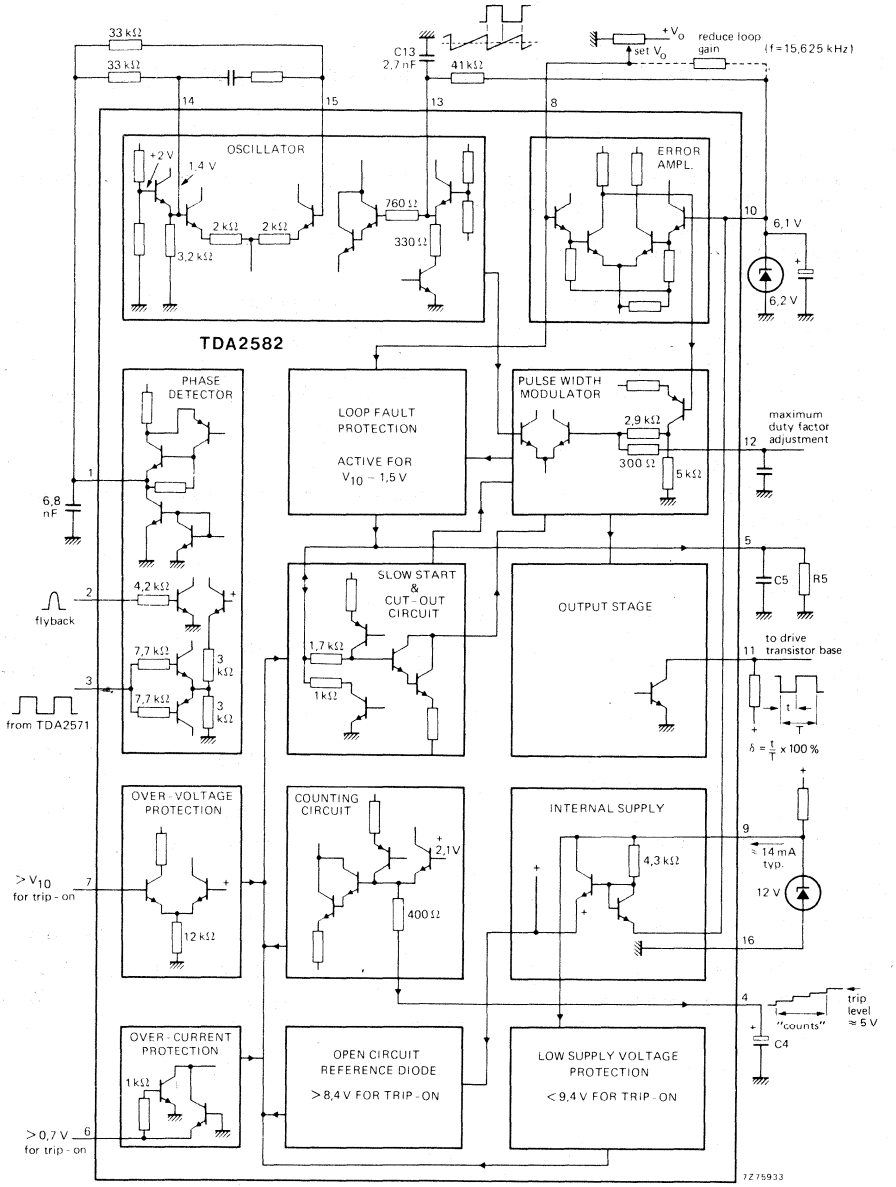


Fig. 1 Block diagram.

Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at pin 9	V_{9-16}	max.	14 V
Voltage at pin 11	V_{11-16}		0 to 14 V
Output current (peak value)	I_{11M}	max.	40 mA
Total power dissipation	P_{tot}	max.	280 mW
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 80 °C

CHARACTERISTICS

V_{9-16} = 12 V; V_{10-16} = 6,1 V; T_{amb} = 25 °C; measured in Fig. 4

Supply voltage range	V_{9-16}	typ.	12 V
			10 to 14 V
Protection voltage too low supply voltage	V_{9-16}	typ.	9,4 V
			8,6 to 9,9 V
Supply current at δ = 50%	I_9	typ.	14 mA
Supply current during protection	I_9	typ.	14 mA
Minimum required supply current (note 1)	I_9	<	17 mA
Power consumption	P	typ.	170 mW
Required input signals			
Reference voltage (note 2)	V_{10-16}	typ.	6,1 V
			5,6 to 6,6 V
Feedback input impedance	$\lvert Z_{8-16} \rvert$	typ.	200 kΩ
High reference voltage protection: threshold voltage	V_{10-16}	typ.	8,4 V
			7,9 to 8,9 V
Horizontal reference signal (square-wave or differentiated; negative transient is reference)			
Voltage driven (peak-to-peak value)	$V_{3-16(p-p)}$		5 to 12 V
Current driven (peak value)	I_{3M}		−1 to + 1,5 mA
Switching level current	$\pm I_3$	<	100 μA
Flyback pulse or differential deflection current	V_{2-16}		1 to 5 V
Flyback pulse current (peak value)	I_{2M}	<	1,5 mA
Over-current protection: (note 3) threshold voltage	$-V_{6-16}$	typ.	640 mV
			600 to 695 mV
	$+V_{6-16}$	typ.	680 mV
			640 to 735 mV

Notes

1. This value refers to the minimum required supply current that will start all devices under the following conditions: V_{9-16} = 10 V; V_{10-16}= 6,2 V; δ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Over-voltage protection: ($V_{ref} = V_{10\text{-}16}$) threshold voltage	$V_{7\text{-}16}$	typ. $V_{ref}-130$ to $V_{ref}-0$	$V_{ref}-60$ mV mV
Remote control voltage; switch-off (note 1)	$V_{4\text{-}16}$	>	5,6 V
Remote control voltage; switch-on	$V_{4\text{-}16}$	<	4,5 V
'Smooth' remote control; switch-off (note 2)	$V_{5\text{-}16}$	>	4,5 V
'Smooth' remote control; switch-on	$V_{5\text{-}16}$	<	3 V
Remote control switch-off current	I_4	<	1 mA
Delivered output signals			
Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value	$V_{11\text{-}16(p\text{-}p)}$	>	11,6 V
Output current; peak value	I_{11M}	<	40 mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ. <	200 mV 400 mV
at I_{11} = 40 mA	V_{CEsat}	<	525 mV
Duty factor of output pulse (note 3)	δ	> <	0 % 98 ± 0,8 %
Charge current for capacitor on pin 4	I_4	typ.	110 μA
Charge current for capacitor on pin 5	I_5	typ.	120 μA
Supply current for reference	I_{10}	typ.	1 mA 0,6 to 1,45 mA
Oscillator			
Temperature coefficient		typ. <	0,0003 $^{o}C^{-1}$ 0,0004 $^{o}C^{-1}$
Relative frequency deviation for $V_{10\text{-}16}$ changing from 5,6 to 6,6 V		typ. <	−1,4 % −2 %
Oscillator frequency spread (with fixed external components)		<	3 %
Frequency control sensitivity at pin 15 f_{nom} = 15,625 kHz		typ.	5 kHz/V

Notes

1. See function description pin 4 (pages 9 and 10).
2. See function description pin 5 (page 10).
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between $V_{8\text{-}16}$ and the duty factor is given in Fig. 7 and the relationship between $V_{12\text{-}16}$ and the duty factor is shown in Fig. 9.

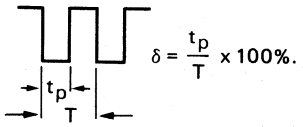


Fig. 2.

Phase control loop

Loop gain of APC-system (automatic phase control) *		typ.	5	kHz/μs
Catching range (f_{nom} = 15,625 kHz)	Δf	>	1300	Hz
		<	2100	Hz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	± 0,4	μs

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

* For component values see Fig. 1.

APPLICATION INFORMATION

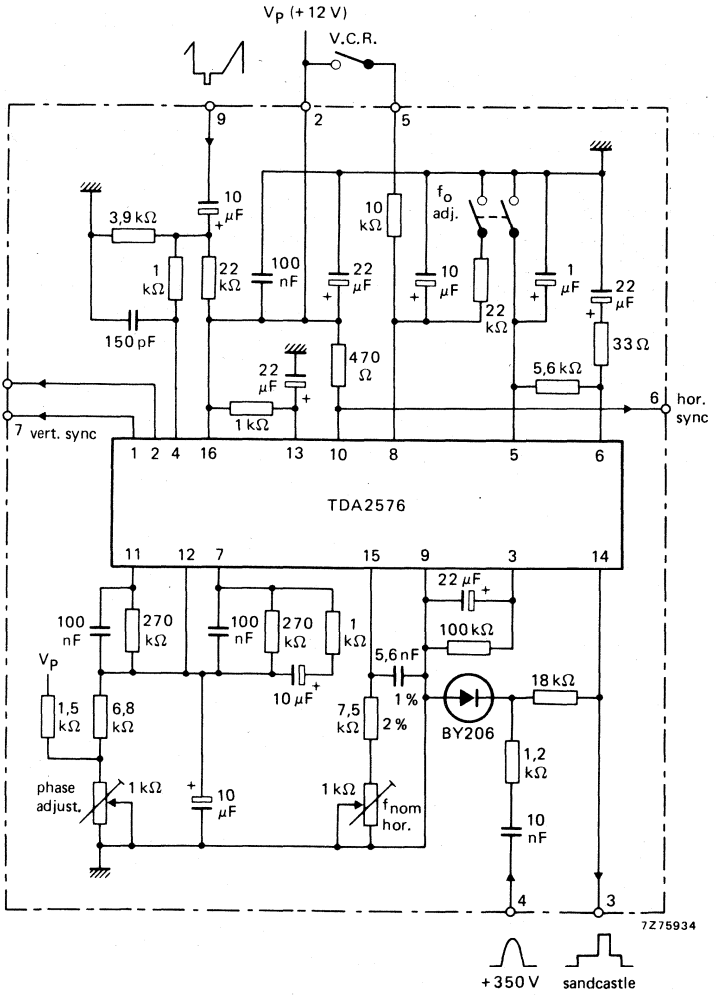


Fig. 3a.

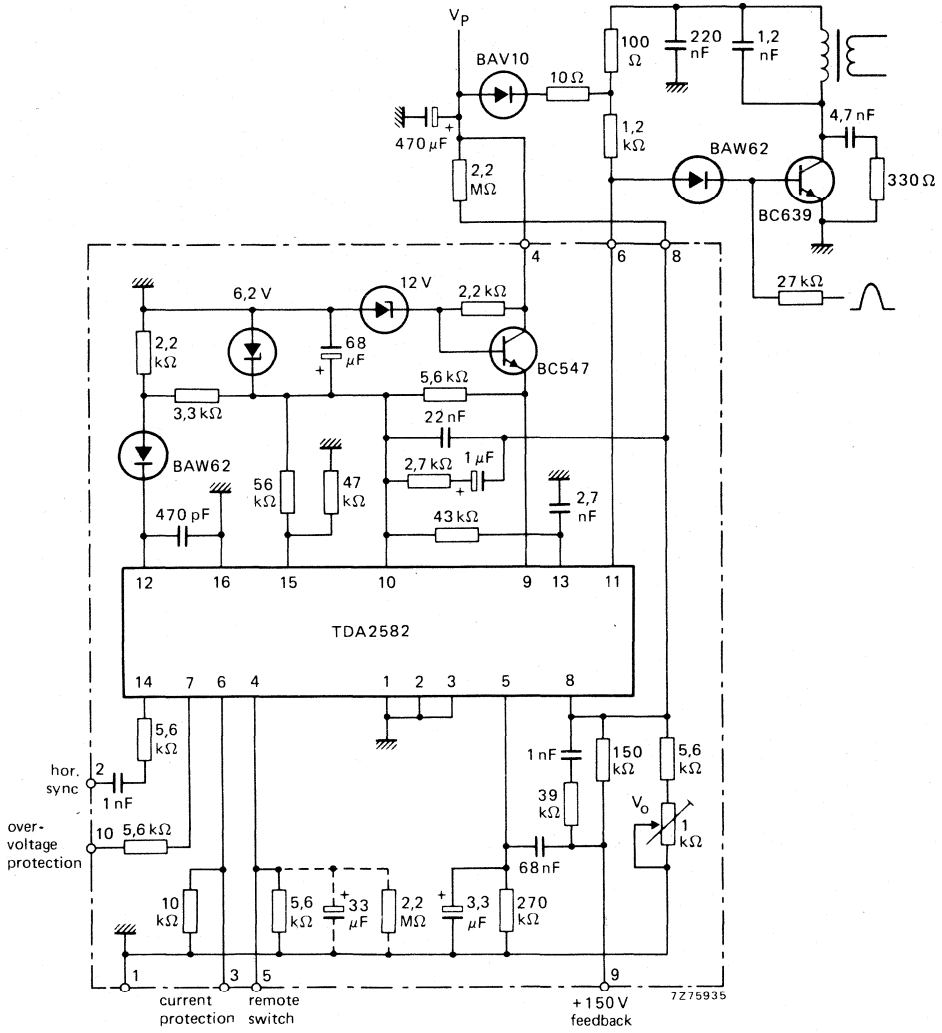


Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

APPLICATION INFORMATION

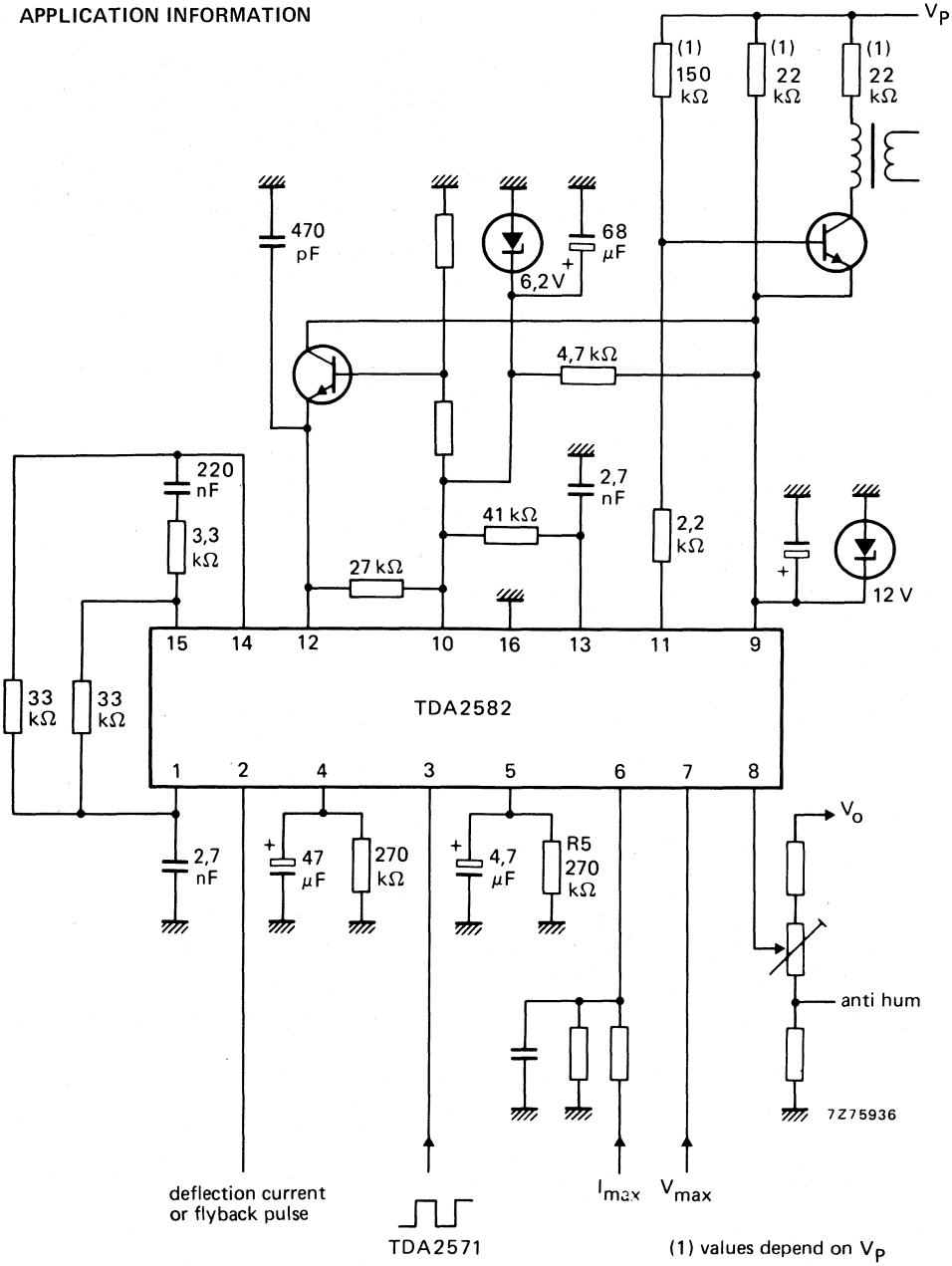


Fig. 4 Circuit diagram.

The function is described against the corresponding pin number

1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs (Fig. 4).

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).

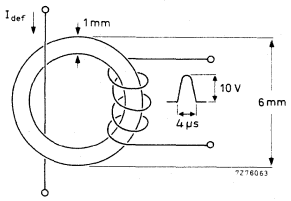


Fig. 5a.

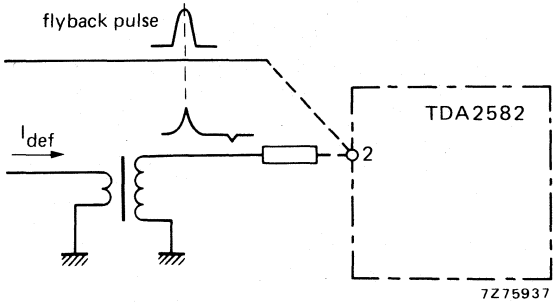


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in Fig. 7.

'Smooth' remote ON/OFF

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16} = 6{,}1$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

16. Negative supply (ground)

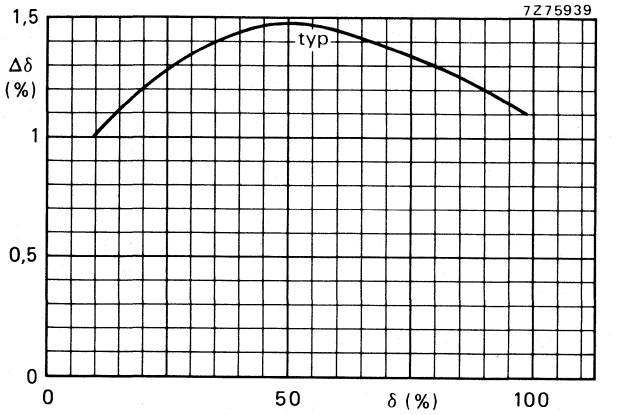


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)} = 1$ mV.

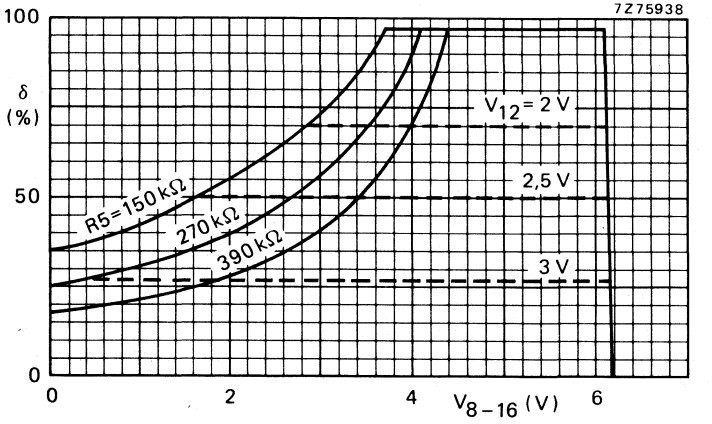


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16} = 6{,}1$ V.

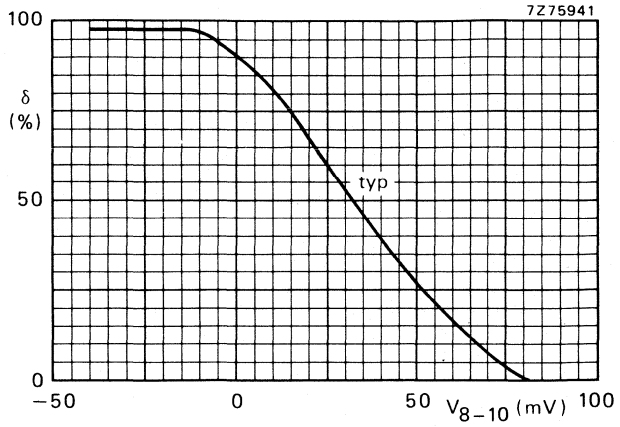


Fig. 8 Duty factor of output pulses as a function of error amplifier input ($V_{8\text{-}10}$); $V_{10\text{-}16}$ = 6,1 V.

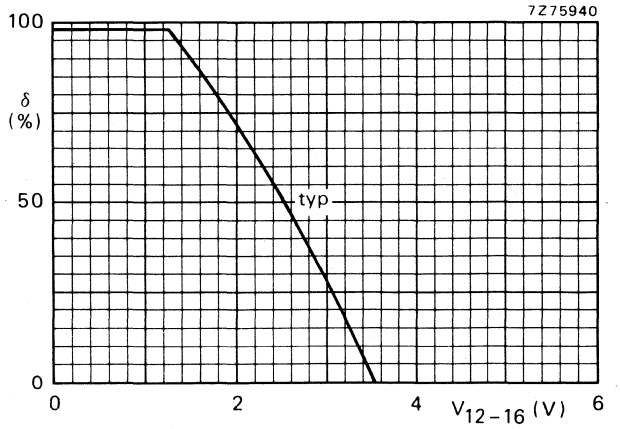


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; $V_{10\text{-}16}$ = 6,1 V.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5 V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

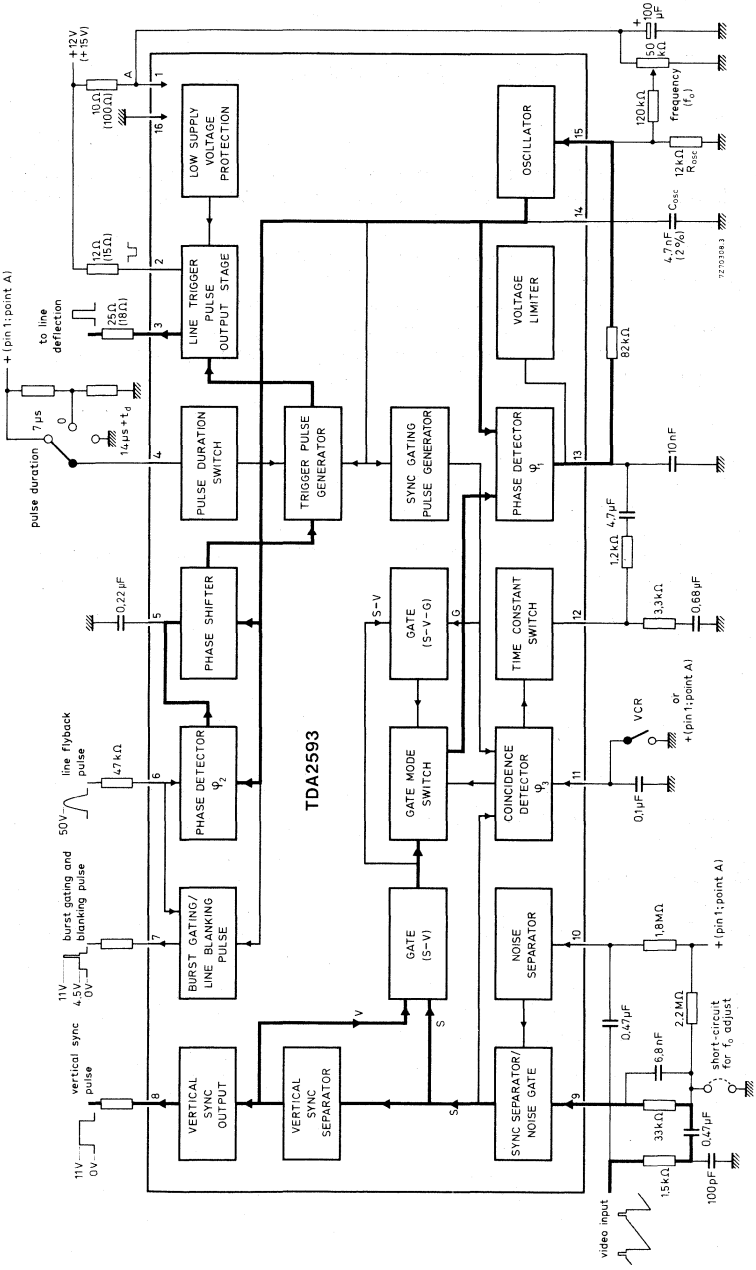


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	V_{1-16}	max.	13,2 V
at pin 2	V_{2-16}	max.	18 V
Voltages			
Pin 4	V_{4-16}	max.	13,2 V
Pin 9	$\pm V_{9-16}$	max.	6 V
Pin 10	$\pm V_{10-16}$	max.	6 V
Pin 11	V_{11-16}	max.	13,2 V
Currents			
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650 mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	10 mA
Pin 11	I_{11}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 70 °C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8 V
Input keying current	I_9		5 to 100 μA
Input leakage current at V_{9-16} = −5 V	I_9	<	1 μA
Input switching current	I_9	⩽	5 μA
Switch off current	I_9	>	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator			
Input switching voltage	V_{10-16}	typ.	1,4 V
Input keying current	I_{10}		5 to 100 μA
Input switching current	I_{10}	>	100 μA
		typ.	150 μA
Input leakage current at $V_{10-16} = -5$ V	I_{10}	<	1 μA
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4 V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7 V
Line flyback pulse			
Input current	I_6	typ.	1 mA
			0,02 to 2 mA
Input switching voltage	V_{6-16}	typ.	1,4 V
Input limiting voltage	V_{6-16}		−0,7 to + 1,4 V
Switching on VCR			
Input voltage	V_{11-16}		0 to 2,5 V
	V_{11-16}		9 to V_{1-16} V
Input current	$-I_{11}$	<	200 μA
	I_{11}	<	2 mA
Pulse duration switch			
For t = 7 μs (thyristor driving)			
Input voltage	V_{4-16}		9,4 to V_{1-16} V
Input current	I_4	>	200 μA
For t = 14 μs + t_d (transistor driving)			
Input voltage	V_{4-16}		0 to 3,5 V
Input current	$-I_4$	>	200 μA
For t = 0; $V_{3-16} = 0$ or input pin 4 open			
Input voltage	V_{4-16}		5,4 to 6,6 V
Input current	I_4	typ.	0 μA

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	$>$	10	V
		typ.	11	V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on}	μs
Burst gating pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	$>$	10	V
		typ.	11	V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}16} = 7$ V	t_p	typ.	4	μs
			3,7 to 4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16} = 7$ V	t	typ.	2,65	μs
			2,15 to 3,15	μs
Output trailing edge current	I_7	typ.	2	mA
Line flyback-blanking pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA
Line drive pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (thyristor driving)				
$V_{4\text{-}16} = 9{,}4$ to $V_{1\text{-}16}$ V	t_p	typ.	7	μs
			5,5 to 8,5	μs
Pulse duration (transistor driving)				
$V_{4\text{-}16} = 0$ to 4 V; $t_{fp} = 12$ μs	t_p		$14 + t_d$	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4	V
Overall phase relation				
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6	μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	$<$	0,7	μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration $t_{fp} = 12$ μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	$V_{14\text{-}16}$	typ.	4,4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0,05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	$V_{13\text{-}16}$		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	<	1	μA
Output resistance at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

Phase comparison φ_2 and phase shifter			
Control voltage range	$V_{5\text{-}16}$	5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ. 1	mA
Output resistance			
at $V_{5\text{-}16}$ = 5,4 to 7,6 V		high ohmic	*
at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V	R_5	typ. 8	kΩ
Input leakage current			
$V_{5\text{-}16}$ = 5,4 to 7,6 V	I_5	< 5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	< 15	μs
Static control error	$\Delta t/\Delta t_d$	< 0,2	%
Coincidence detector φ_3			
Output voltage	$V_{11\text{-}16}$	0,5 to 6	V
Output current (peak value)			
without coincidence	I_{11M}	typ. 0,1	mA
with coincidence	$-I_{11M}$	typ. 0,5	mA
Time constant switch			
Output voltage	$V_{12\text{-}16}$	typ. 6	V
Output current (limited)	$\pm I_{12}$	< 1	mA
Output resistance			
at $V_{11\text{-}16}$ = 2,5 to 7 V	R_{12}	typ. 0,1	kΩ
at $V_{11\text{-}16} < 1{,}5$ V or > 9 V	R_{12}	typ. 60	kΩ
Internal gating pulse			
Pulse duration	t_p	typ. 7,5	μs

* Current source.

SOUND OUTPUT CIRCUIT

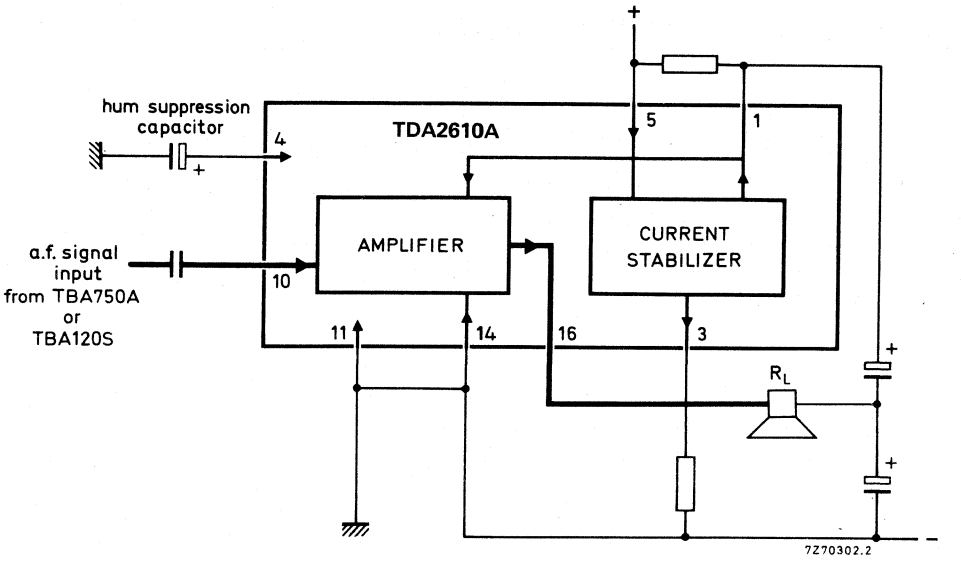
The TDA2610 and TDA2610A are sound output circuits for use in colour and black and white television receivers.
The output circuit in the TDA2610 is a class-B arrangement and can deliver an output power of 7 W. A current stabilizing circuit is incorporated in the TDA2610A to obtain a constant current drain and an output power of 4 W is available.
This constant current mode allows the TDA2610A to be supplied by the horizontal output transformer.
Furthermore the TDA2610 and TDA2610A feature :
- short circuit protected output
- thermal shut-down circuit
- low number of external components

QUICK REFERENCE DATA				
Supply voltage	V_{5-11}	typ.	25	V
Supply current	I_5	typ.	300	mA
Load resistance	R_{16-11}	typ.	15	Ω
Output power at f = 1 kHz; d_{tot} = 10%	P_o	typ.	4	W
Input voltage for $P_o = P_{o\,max}$	V_{10-11}	typ.	100	mW
Input impedance	$\lvert Z_{10-11} \rvert$	typ.	45	kΩ

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69B).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage at pin 5	V_{5-11}	max.	35	V
at pin 1	V_{1-11}	max.	35	V

Current

Output current (peak value)	I_{16M}	max.	2	A

Power dissipation

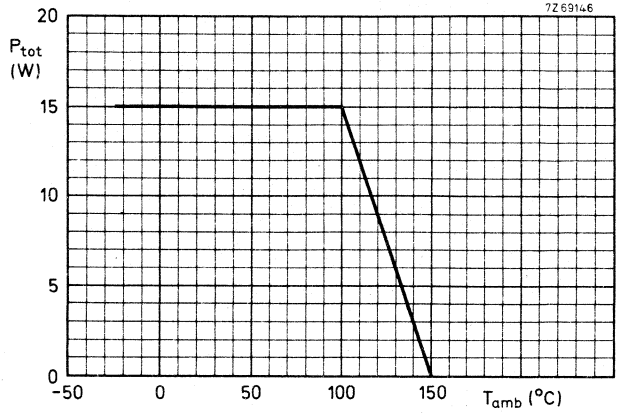
Total power dissipation — see derating curve on page 3

Temperatures

Storage temperature	T_{stg}	−55 to +150	°C
Operating ambient temperature	T_{amb}	−25 to +150	°C

RATINGS (continued)

Power derating curve



CHARACTERISTICS at T_{amb} = 25 °C; measured in the top circuit on page 4

Supply voltage	V_{5-11}	typ.	25	V
			15 to 35	V

Performance at V_{5-11} = 25 V; R_L = 15 Ω; f = 1 kHz

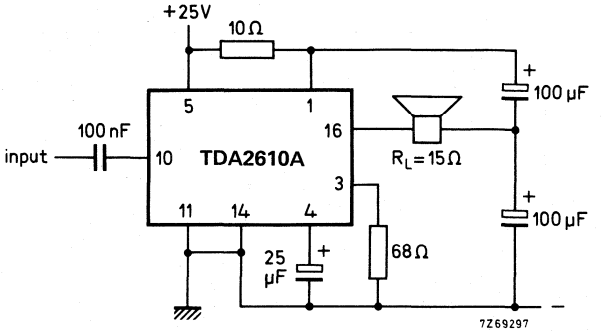
Stabilizing current	I_3	typ.	0,3	A
		<	0,5	A
Output power at d_{tot} = 10%	P_o	typ.	4	W
Output current (repetitive peak value)	I_{16RM}	typ.	0,8	A
Input voltage for $P_o = P_{o\,max}$	V_{10-11}	typ.	100	mV
Input impedance	$\lvert Z_{10-11} \rvert$	typ.	45	kΩ
Frequency response	f	>	15	kHz
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_{16-11}	<	0,5	mV

CHARACTERISTICS at T_{amb} = 25 °C; measured in the bottom circuit on page 4

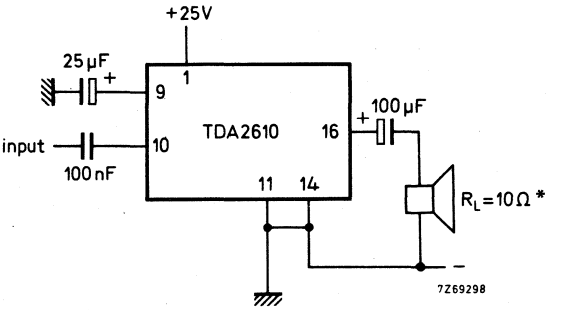
Performance at V_{1-11} = 25 V; R_L = 10 Ω; f = 1 kHz

Output power at d_{tot} = 10%	P_o	typ.	7	W
Output current (repetitive peak value)	I_{16RM}	typ.	1,2	A
Input voltage for P_o = 4 W	V_{10-11}	typ.	90	mV
Total quiescent current	I_{tot}	typ.	22	mA

APPLICATION INFORMATION



Sound output circuit with shunt stabilizer (P_o = 4 W)



Sound output circuit without shunt stabilizer (P_o = 7 W)

* Obtained via a transformer.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

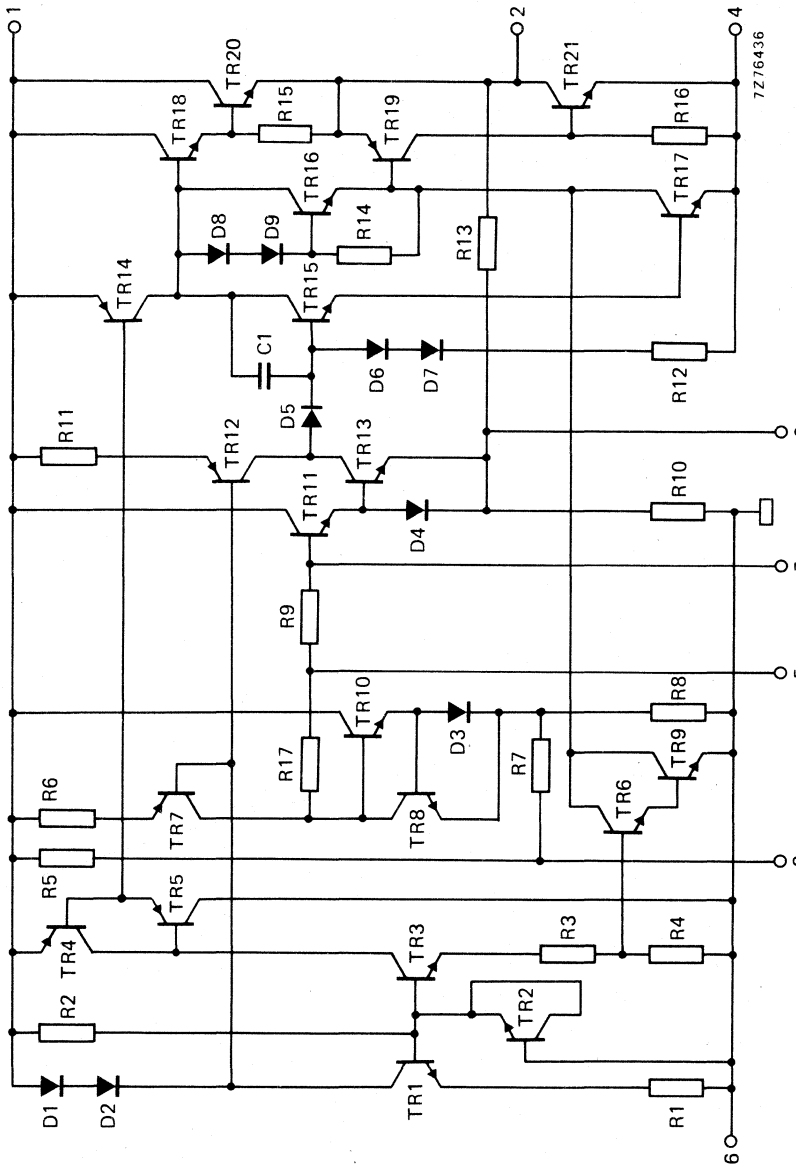


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C

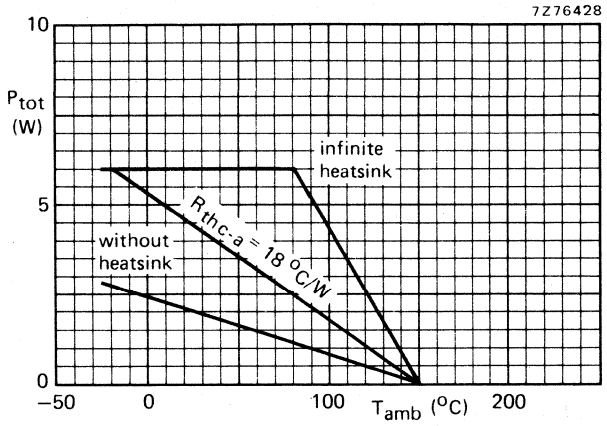


Fig. 2 Power derating curves.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
→ Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

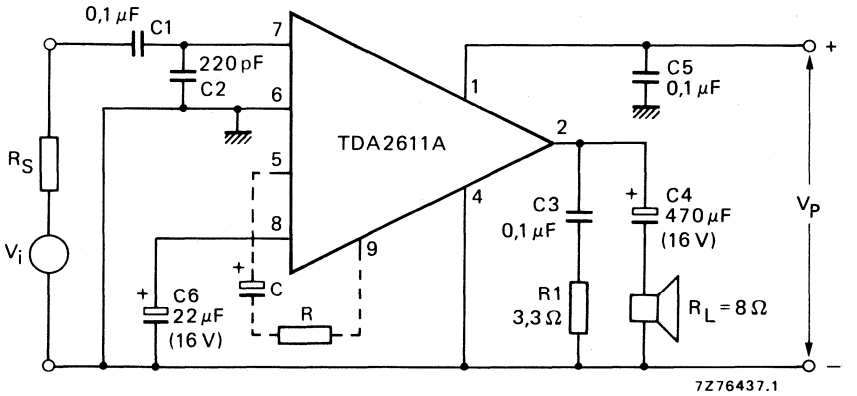


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

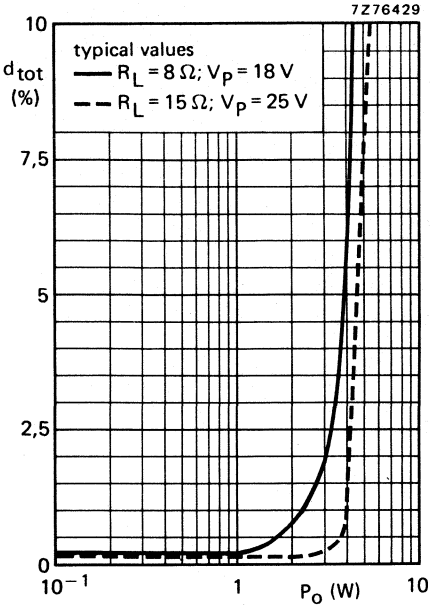


Fig. 4 Total harmonic distortion as a function of output power.

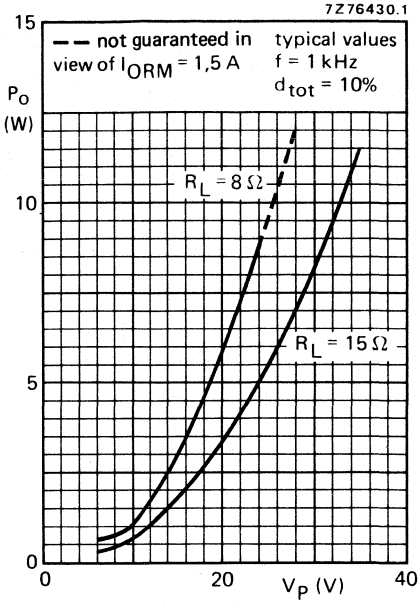


Fig. 5 Output power as a function of supply voltage.

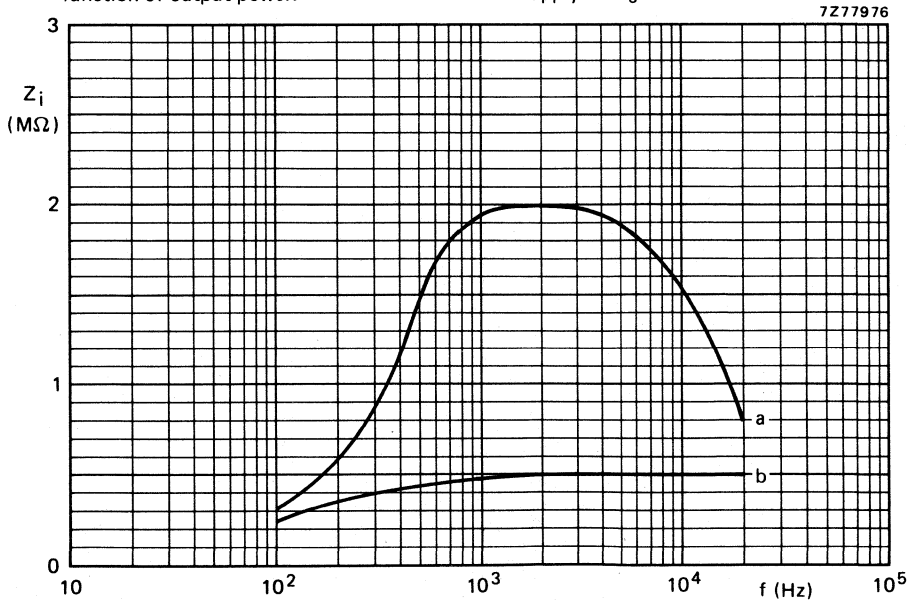


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

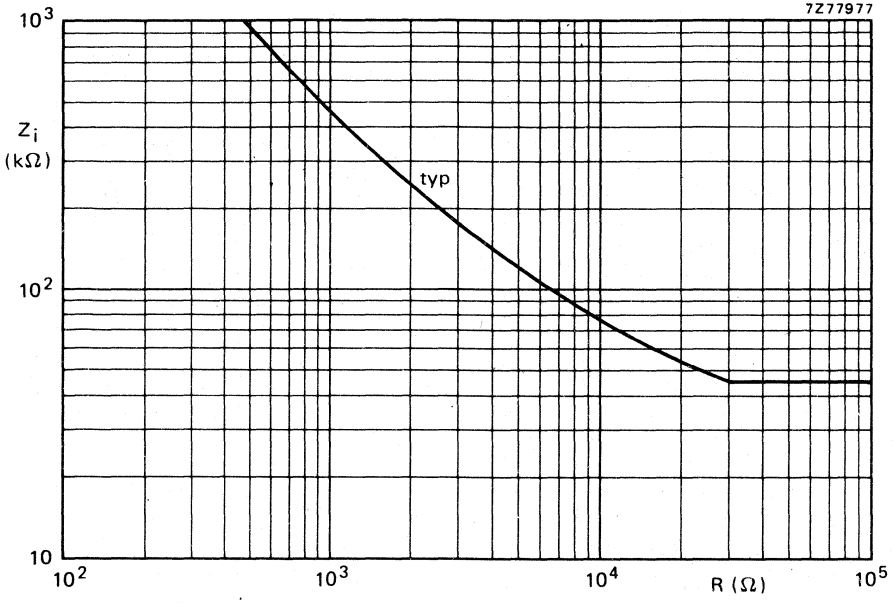


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

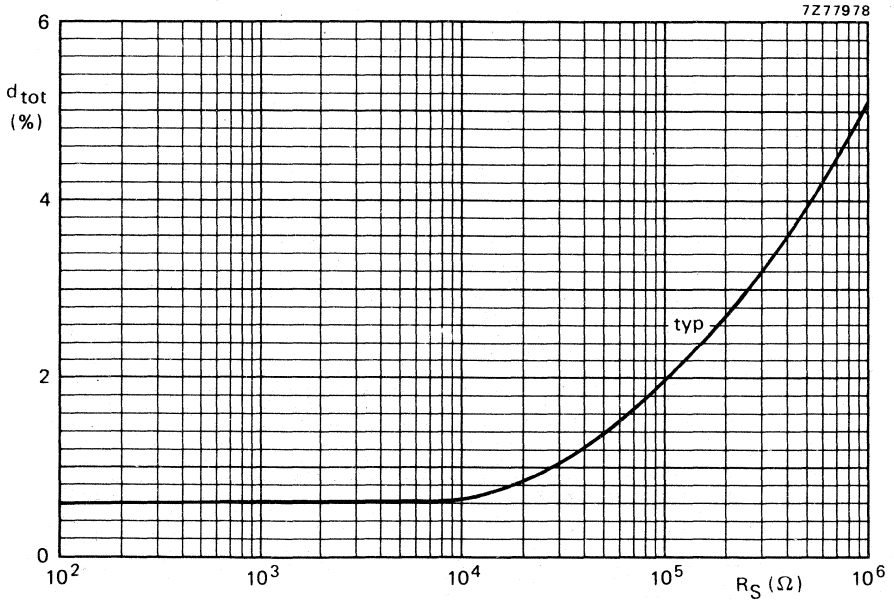


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

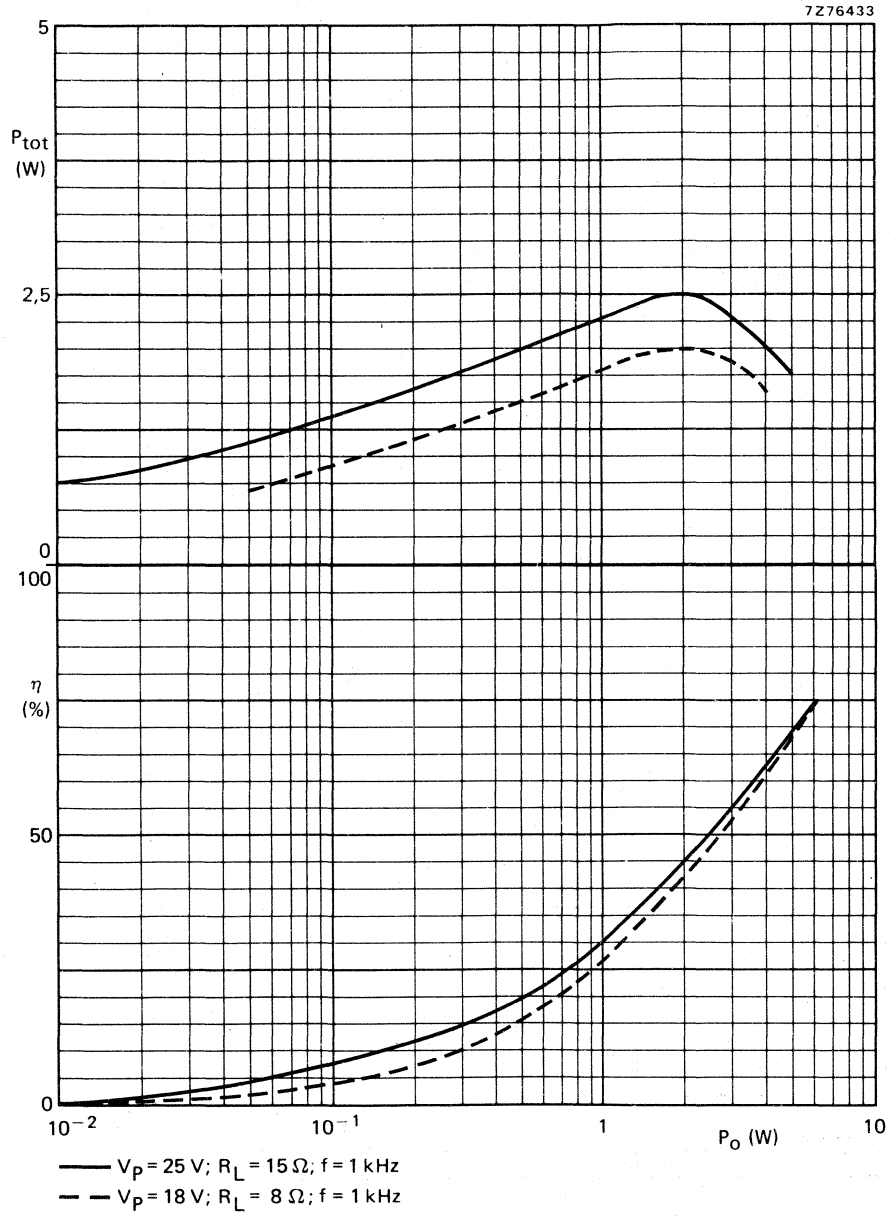


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

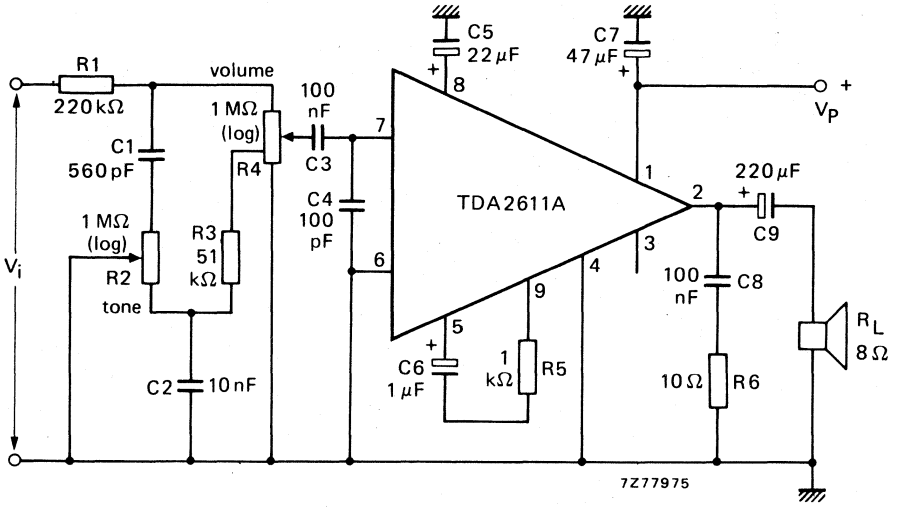


Fig. 10 Ceramic pickup amplifier circuit.

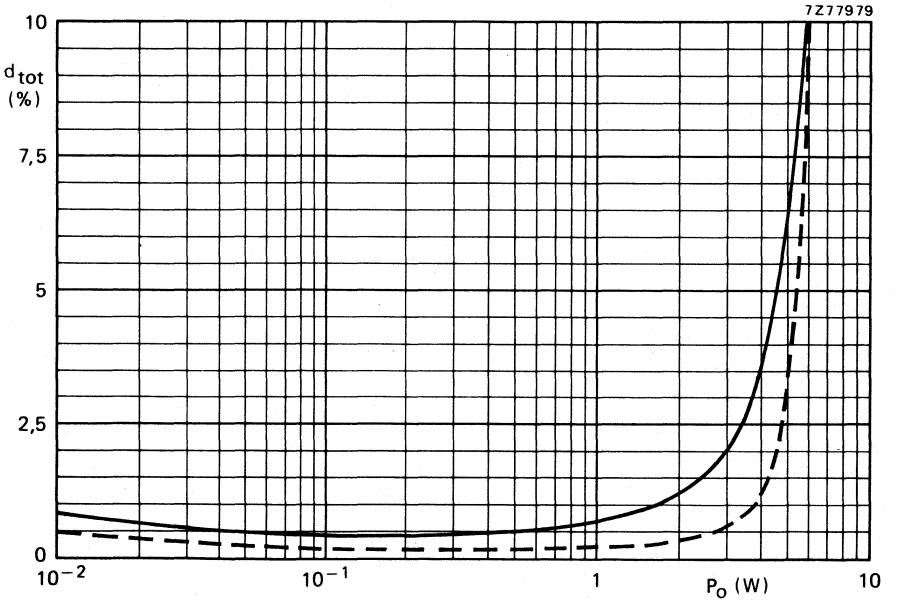


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

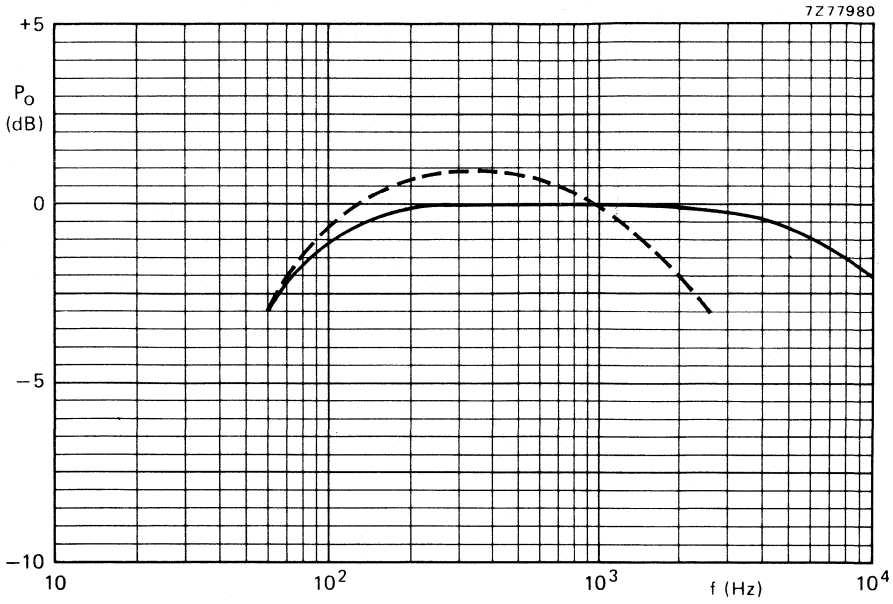


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_O relative to 0 dB = 3 W; typical values.

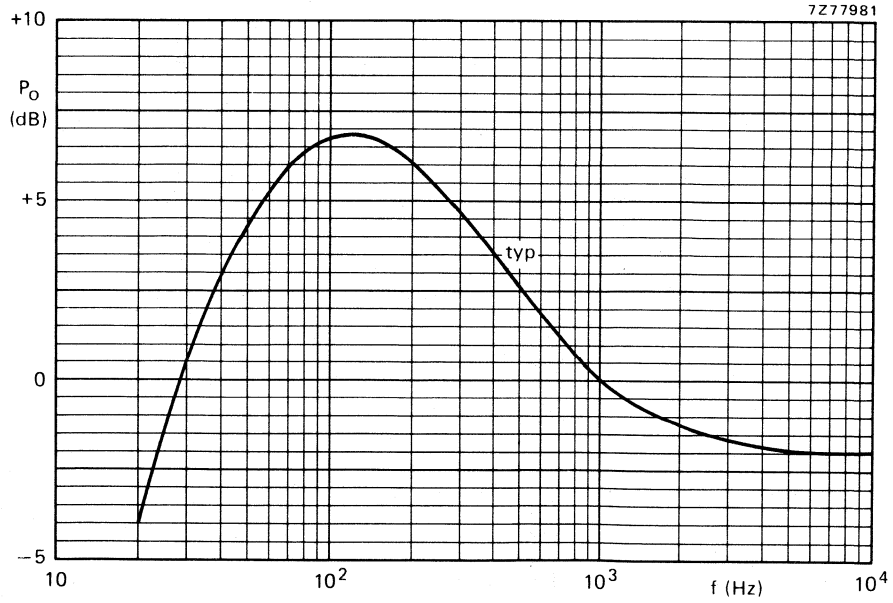


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

HI-FI POWER AMPLIFIER

The TDA2612 is a monolithic hi-fi power amplifier, intended for hi-fi television sets, radios, record players, tape recorders.
This IC can be used very well in conjunction with sound channel ICs, e.g. TBA570A, TBA120S and TDA2790.
The performance of the circuit fulfils DIN45500.

Features:
- Low harmonic distortion
- Low intermodulation distortion
- Low transient intermodulation
- Good hum suppression

QUICK REFERENCE DATA

Supply voltage range (pin 6)	V_S	10 to 35	V
Output power at d_{tot} = 0,7%; R_L = 4 Ω; V_{6-9} = 26 V	P_o	> 10	W
Total harmonic distortion at P_o = 6 W	d_{tot}	typ. 0,1	%
Power bandwidth (−3 dB); d_{tot} = 0,7%	B	40 Hz to 16	kHz
Input voltage for P_o = 10 W	V_i	typ. 180	mV
Signal-to-noise ratio (unweighted) related to P_o = 100 mW	S/N	typ. 72	dB

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69B).

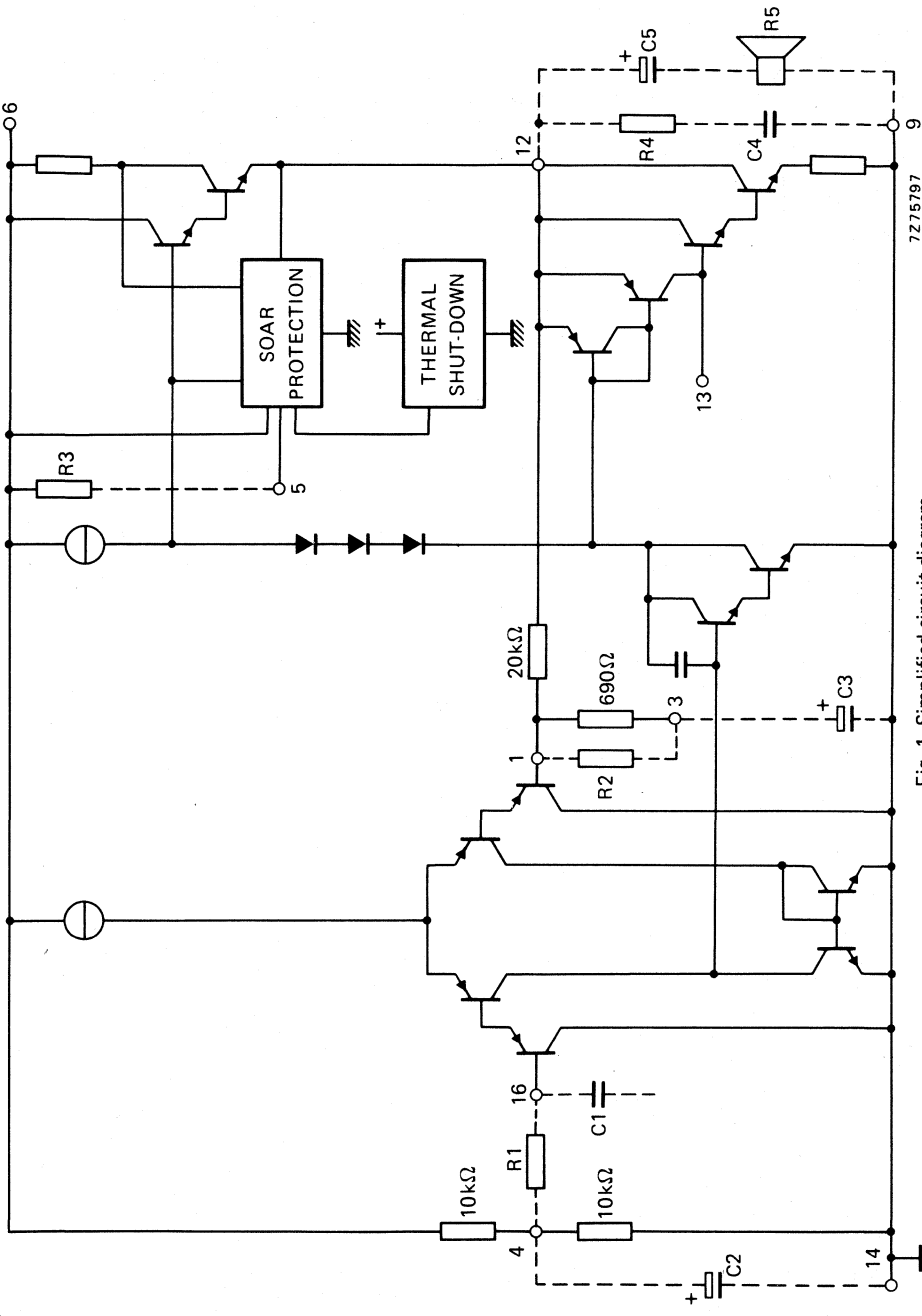


Fig. 1 Simplified circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{6-9}	max.	35	V
Non-repetitive peak output current	I_{12}	max.	5	A
Total power dissipation	see derating curves Fig. 2			
Shot-circuit time of load impedance during signal drive; V_S = 25 V	t_{sc}	max.	100	hours
Storage temperature	T_{stg}	max.	150	°C
Ambient temperature	T_{amb}	max.	150	°C

THERMAL RESISTANCE

The power derating curves (Fig. 2) are based on the following data

From junction to case	$R_{th\ j\text{-}c}$	=	3,3	°C/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	45	°C/W

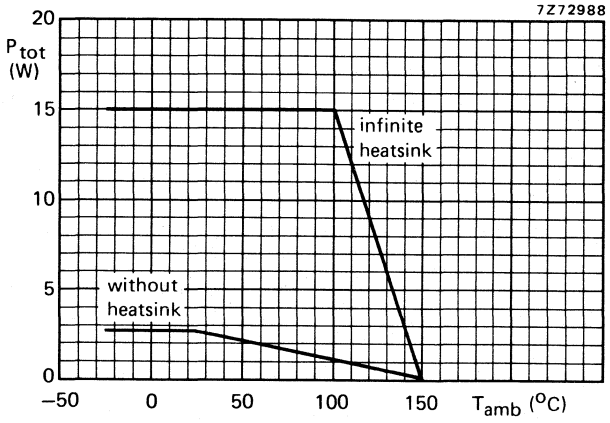


Fig. 2 Power derating curves.

CHARACTERISTICS

Supply voltage (pin 6)	V_S	typ.	26 V
			10 to 35 V
Characteristics at V_S = 26 V; T_{amb} = 25 °C; f = 1 kHz; see Fig. 3.			
Output current (peak value)	I_o	<	3,2 A
Total quiescent current	I_{tot}	typ.	70 mA
		<	105 mA
Output power at d_{tot} = 0,7% (note 1)	P_o	>	10 W
Total harmonic distortion at P_o = 6 W	d_{tot}	typ.	0,1 %
Power bandwidth (–3 dB); d_{tot} = 0,7%	B	40 Hz to	16 kHz
Input voltage for P_o = 10 W	V_i	typ.	180 mV
Input impedance		note 2	
Signal-to-noise ratio related to P_o = 100 mW (note 3)	S/N	>	60 dB
		typ.	72 dB
Damping factor (note 4)	R_L/Z_o	>	3
		typ.	32
Frequency response	f	>	16 kHz
Ripple rejection at f = 100 Hz; R_S = 5 kΩ (note 5)	RR	typ.	50 dB

Notes

1. Output power measured with an ideal coupling capacitor to the load impedance.
2. The input impedance determinated by the external resistor R1.
3. The unweighted noise is measured in a bandwidth of 40 Hz to 16 kHz at R_S = 5 kΩ.
4. Z_o is the output impedance measured between 40 Hz and 12,5 kHz.
5. The ripple rejection is defined as: 20 log $\frac{V_{SR}}{V_{OR}}$ in which V_{SR} = ripple voltage at supply line and V_{OR} = ripple voltage across loudspeaker load.

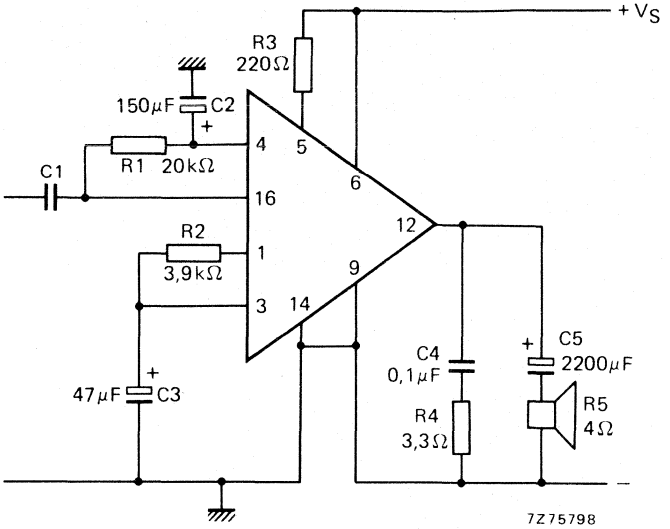


Fig. 3 Test circuit.

MOUNTING INSTRUCTIONS

When using an external heatsink, connected to the heat spreader of the IC, the thermal power in the circuit can be reduced to a negligible value.
The optimum heatsink dimensions (blackened aluminium) for a given operating ambient temperature, can be found from the derating curves in Fig. 2.
The fact that the thermal resistance of the encapsulation is very good, results in a relatively small heatsink for thermal power reduction.

Two mounting methods are shown in Figs 4 and 5.
By using these methods, no extra copper area is required on the printed-circuit board, so a saving in printed-wiring area is obtained.
Mounting the external heatsink can be done by screwing or clipping.
Mechanical stresses do not damage the IC.
It is recommended that a heatsink-compound be used between IC heat spreader and heatsink.

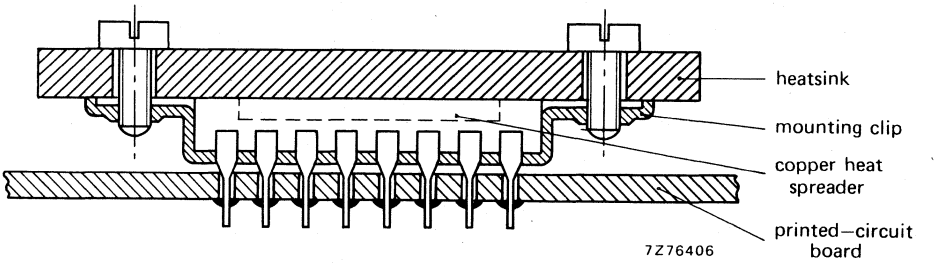


Fig. 4 Mounting method 1.

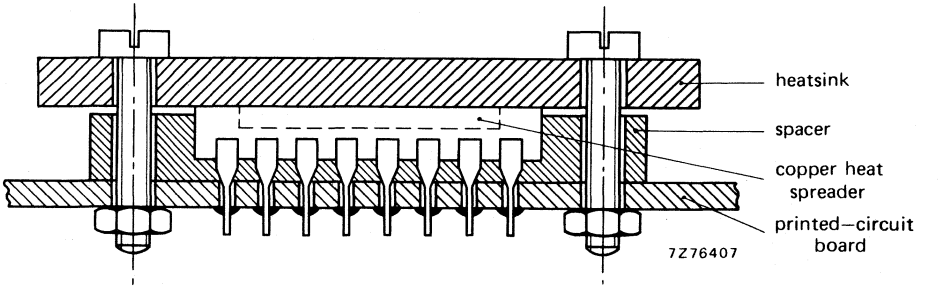


Fig. 5 Mounting method 2.

SWITCHED-MODE POWER SUPPLY DRIVE CIRCUIT

The TDA2640 is a monolithic integrated circuit for driving the switched-mode power supply of a colour or black and white television receiver.
Except for the drive and output voltage stabilizing circuitry the TDA2640 incorporates the following functions :

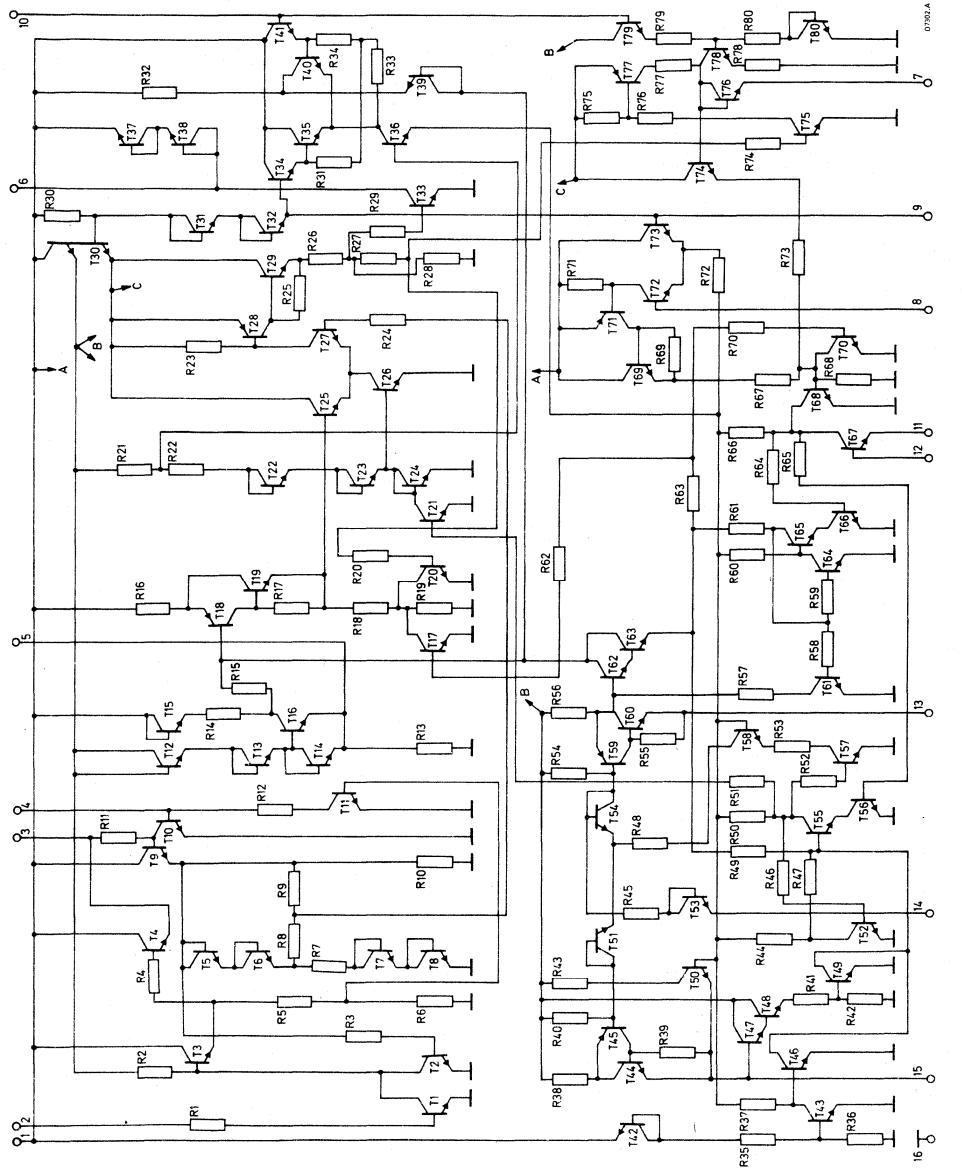
- fixed frequency determined by external components
- remote switch off and restart
- over-current protection
- over-voltage protection
- slow starting
- low supply voltage protection
- open-circuit feedback protection
- optional synchronization

QUICK REFERENCE DATA				
Supply voltage	V_{1-16}	typ.	12	V
Supply current	I_1	typ.	8,1	mA
Output voltage (peak-to-peak value)	$V_{6-16(p-p)}$	>	11,5	V
Output current (peak value)	I_{6M}	<	20	mA
Duty factor of output pulse	δ	typ.	20 to 85	%
Reference input voltage	V_{9-16}	typ.	6,2	V
Sync pulse (peak-to-peak value)	$V_{2-16(p-p)}$		1 to 10	V

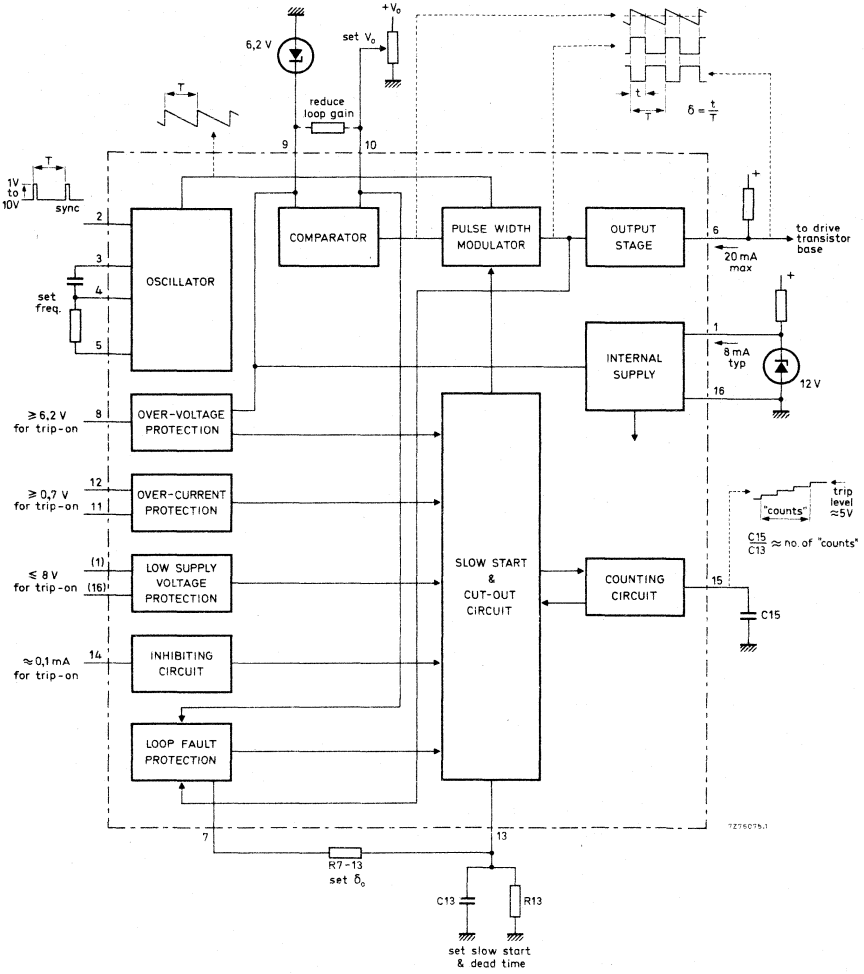
PACKAGE OUTLINES

TDA2640 : 16-lead DIL; plastic (SOT-38).
TDA2640Q : 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages			
Supply voltage	V_{1-16}	max.	13,8 V
Pin 2	V_{2-16}		−5 to +10 V
Pin 8	V_{8-16}		0 to +10 V
Pin 9	V_{9-16}		0 to +10 V
Pin 10	V_{10-16}		0 to V_{9-16} +1 V
Pin 9 with respect to pin 10	V_{9-10}		−1 to +7 V
Pin 11 (pin 12 not connected)	V_{11-16}		−1 to 0 V
Current			
Output current (peak value)	I_{6M}	max.	20 mA
Power dissipation			
Total power dissipation	P_{tot}	max.	145 mW
Temperatures			
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C

Supply current at δ = 50%	I_1	typ.	8,1 mA 5,1 to 10,4 mA
Reference voltage		typ.	6,2 V 5,6 to 6,5 V [1]
Sync pulse (peak-to-peak value)	$V_{2-16(p-p)}$		1 to 10 V
Remote switch: inhibit (switched off)	V_{14-16}		0 to 3 V
normal (switched on)	V_{14-16}		5 to 12 V [2]
Over-voltage protection: threshold voltage	V_{8-16}	typ.	6,2 V [3]
input current	I_8	typ.	2 μA
temperature coefficient		typ.	0,1 mV/°C
Over-current protection: threshold voltage	V_{12-11}		660 to 760 mV [4]
Low supply voltage protection: threshold voltage	V_{1-16}	typ.	8,6 V 8 to 9,5 V
Horizontal drive pulse (peak-to-peak value)	$V_{6-16(p-p)}$	>	11,5 V [5]
Duty factor of output pulse: maximum	δ_{max}	> typ.	85 % 90 % [6]
minimum	δ_{min}	typ. <	15 % 20 %

For notes see page 5.

CHARACTERISTICS (continued)

Saturation voltage of output transistor at I_6 = 20 mA	V_{CEsat}	typ. <	280 mV 400 mV
Feedback input impedance at pin 10	$\|Z_{10-16}\|$	typ.	100 kΩ
Temperature coefficient for constant duty factor at pin 10		typ.	0,3 mV/°C
Oscillator frequency spread (with fixed external components)		<	±3 %
Rise time of leading edge of output pulse		typ.	0,1 µs

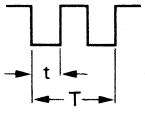
PINNING

1. Positive supply
2. Sync pulse input
3. Oscillator timing capacitor
4. Junction of oscillator timing C and R
5. Oscillator timing resistor
6. Output
7. Low feedback protection external resistor
8. Over-voltage protection input
9. Reference input
10. Feedback voltage input
11. Over-current protection input (emitter)
12. Over-current protection input (base)
13. Slow start C and R controlling network
14. Inhibitor
15. Re-start count capacitor
16. Negative supply (ground)

Notes (from page 4)

1. Voltage obtained via an external reference diode (6,2 V).
2. Or pin 14 not connected.
3. The over-voltage protection threshold is equal to the reference voltage V_{9-16} ±50 mV.
4. The temperature coefficient is typ. −1,7 mV/°C (pin 11 or pin 12 can be connected to pin 16).
5. The maximum voltage on pin 6 is limited to approximately the supply voltage (pin 1) by an internal diode.
6. Valid for normal operating conditions. The circuit starts with 0% duty factor, controlled by the switch-on circuit; the duty factor then rises to the normal operating value.

   The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

APPLICATION INFORMATION (see circuits on pages 3 and 8)

The function is quoted against the corresponding pin number

1. 12 V positive supply

The maximum voltage that may be applied is 13, 8 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 1 and 16 to ensure that the maximum voltage does not exceed 13, 8 V. When the voltage on this pin falls below a minimum of 8 V the protection circuit will switch off the power supply.

2. Sync pulse input

The switching repetition rate may be synchronized to a source of positive-going sync pulses between 1 and 10 V. The free-running frequency of the TDA2640 oscillator must be above the synchronized frequency.
The minimum duration of the sync pulses is the difference between the period of the oscillator pulses and the period of the sync pulses. Synchronization reduces the maximum obtainable duty factor. If synchronization is not required, connect pin 2 to pin 16.

3, 4 and 5. Oscillator timing network

The timing network consists of a capacitor connected between pins 3 and 4, and a resistor connected between pins 4 and 5. The value of these components determines the switching period of the SMPS drive pulses.

6. Output

An external resistor connected between this pin and the supply rail determines the base drive current for the drive transistor. The integrated output circuit consists of an n-p-n transistor with a catching diode connected between its collector and an internal 12 V supply. This provides a low impedance in the "ON" state, that is with the drive transistor turned off.

7. Low feedback protection

An external resistor connected between this pin and pin 13 determines the maximum obtainable duty factor for the output pulses if the feedback voltage (pin 10) remains below the specified limit during starting.

8. Over-voltage protection

A voltage that is proportional to the power supply output voltage can be connected to this pin to operate a protection circuit if a threshold level is exceeded. The threshold level is determined by the external voltage reference diode connected to pin 9 (6, 2 V nominal). If over-voltage protection is not required, pin 8 should be connected to pin 16.

9. Reference input

An external voltage reference diode (6, 2 V nominal) must be connected between this pin and pin 16. The stability of the reference source determines the overall stability of the power supply output voltage. The voltage reference diode current is derived from within the integrated circuit; it has a typical value of 0, 8 mA.

APPLICATION INFORMATION (continued)

10. Feedback voltage input

The control loop input is applied to pin 10. This pin is internally connected to one input of a differential error amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 9. Under normal operating conditions with the comparator at balance, the voltage on pin 10 will be about equal to the reference voltage on pin 9 (6,2 V), and the d.c. feedback factor of the external network should be designed for this value.

11 and 12. Over-current protection

A voltage proportional to the output current of the SMPS is applied to these pins. Pin 11 is connected to the emitter of an internal n-p-n detection transistor; pin 12 is connected to its base. Either of these pins may be grounded (pin 16) depending on the polarity of the input during increasing current. For example, if pin 11 is grounded the trip level on pin 12 is 660 mV to 760 mV; if pin 12 is grounded, the trip level on pin 11 is −660 mV to −760 mV.

13. Slow start

A resistor and capacitor in parallel must be connected between this pin and pin 16 (1 μF and 390 kΩ). This network controls the rate at which the duty factor of the SMPS drive pulses increases to its normal operating value after switch-on. This minimizes inrush current. The network also influences the repetition period of the slow start during a fault.

14. Inhibitor

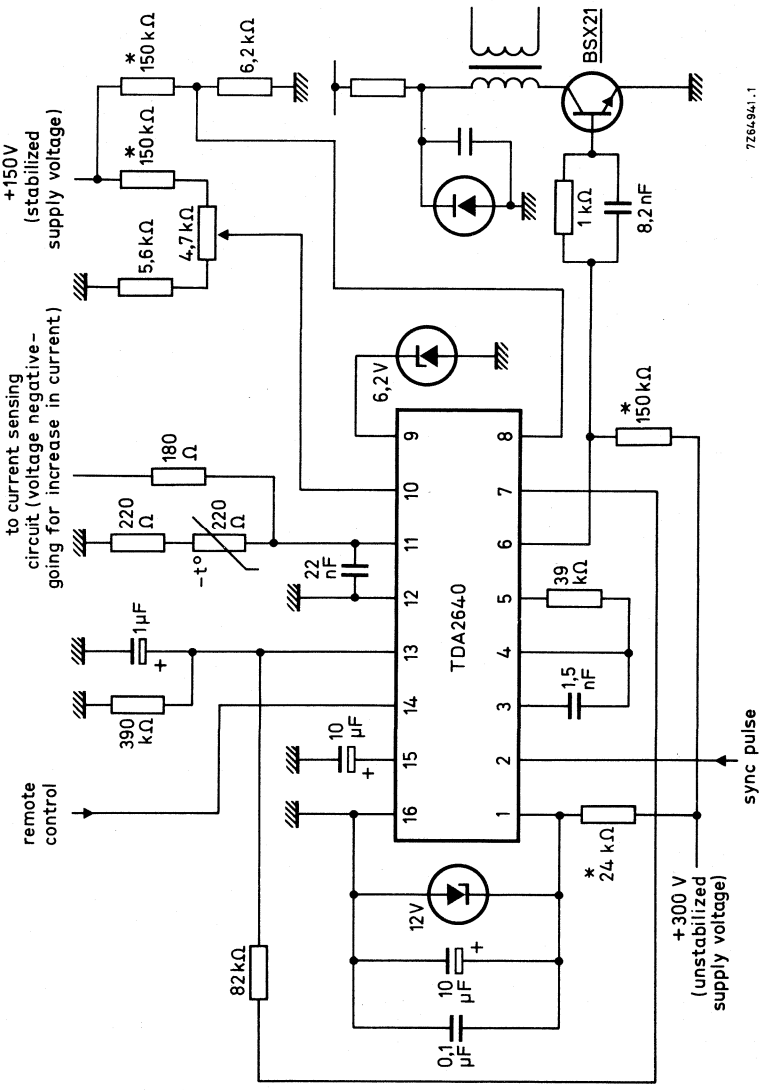
The power supply is switched off if the voltage on this pin is between 0 V and 3 V ($-I_{14} > 0,1$ mA). The power supply is switched on if this pin is not connected, or is connected to a voltage of between 5 V and the 12 V supply. The slow start and protection circuits remain operative under both conditions.

15. Re-start count capacitor

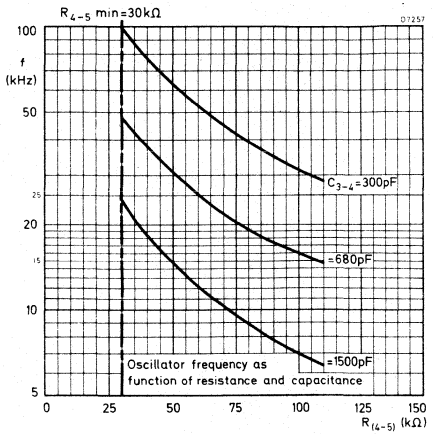
An external capacitor (C15 = 10 μF) should be connected between pins 15 and 16. This capacitor controls the characteristics of the protection circuits as follows. When the protection circuit operates due to a fault, the duty factor of the drive pulses is reduced to zero. After an interval determined by the time-constant of the circuit connected to pin 13, the duty factor of the pulses slowly increases toward its normal operating value. If the fault persists, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated. The number of times that the cycle is repeated before the power supply drive pulses are permanently discontinued is determined by the value of the capacitor connected to pin 15. The number of counts is roughly C15/C13.

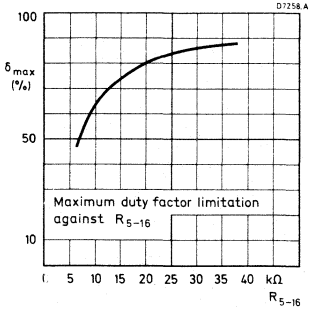
16. Negative supply (ground)

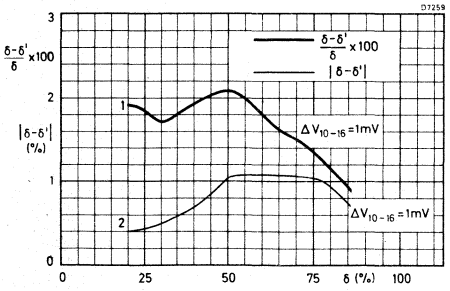
APPLICATION INFORMATION (continued)



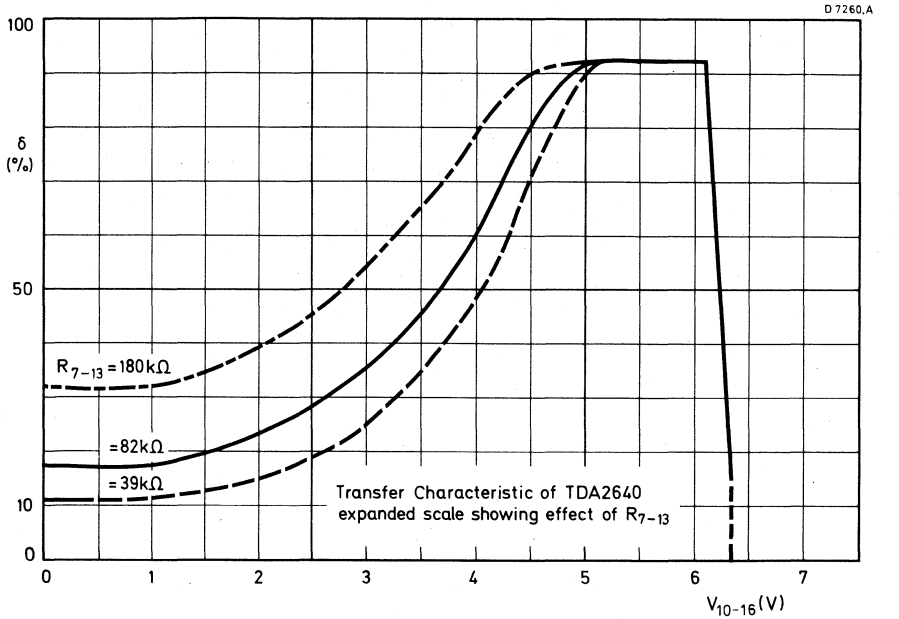
Note: To operate with other supply and output voltages, alternative values of resistors marked thus * must be chosen.

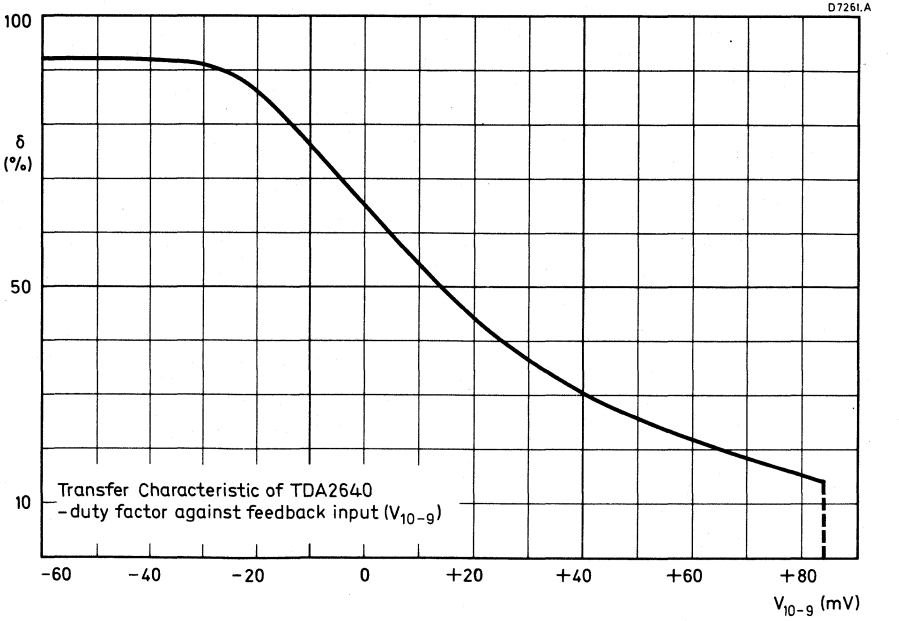






1. Change of transfer characteristic against duty factor for $\Delta V_{10-16} = 1$ mV.
2. Percentage change of transfer characteristics against duty factor for $\Delta V_{10-16} = 1$ mV.


D 7260,A
100
δ
(%)
50
10
0
R_{7-13} = 180kΩ
=82kΩ
=39kΩ
Transfer Characteristic of TDA2640
expanded scale showing effect of R_{7-13}
0
1
2
3
4
5
6
7
V_{10-16}(V)


D7261,A
100
δ
(%)
50
10
Transfer Characteristic of TDA2640
-duty factor against feedback input (V_{10-9})
-60
-40
-20
0
+20
+40
+60
+80
V_{10-9} (mV)

VERTICAL DEFLECTION CIRCUIT

The TDA2652 is a monolithic integrated circuit for colour television receivers with 110° deflection. With an external circuit it can be used in 20AX and 30AX systems. The circuit incorporates the following functions:

- Synchronization circuit
- Vertical oscillator
- Blanking pulse generator
- Sawtooth generator with buffer stage
- Preamplifier
- Driver and output stage
- Short-circuit and thermal protection
- Guard circuit
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Output current (peak-to-peak value)	$I_{G(p-p)}$	max.	4	A
Total power dissipation	P_{tot}	max.	10	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to copper heat spreader (tab)	$R_{th\ j\text{-}tab}$	=	3	K/W

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69C).

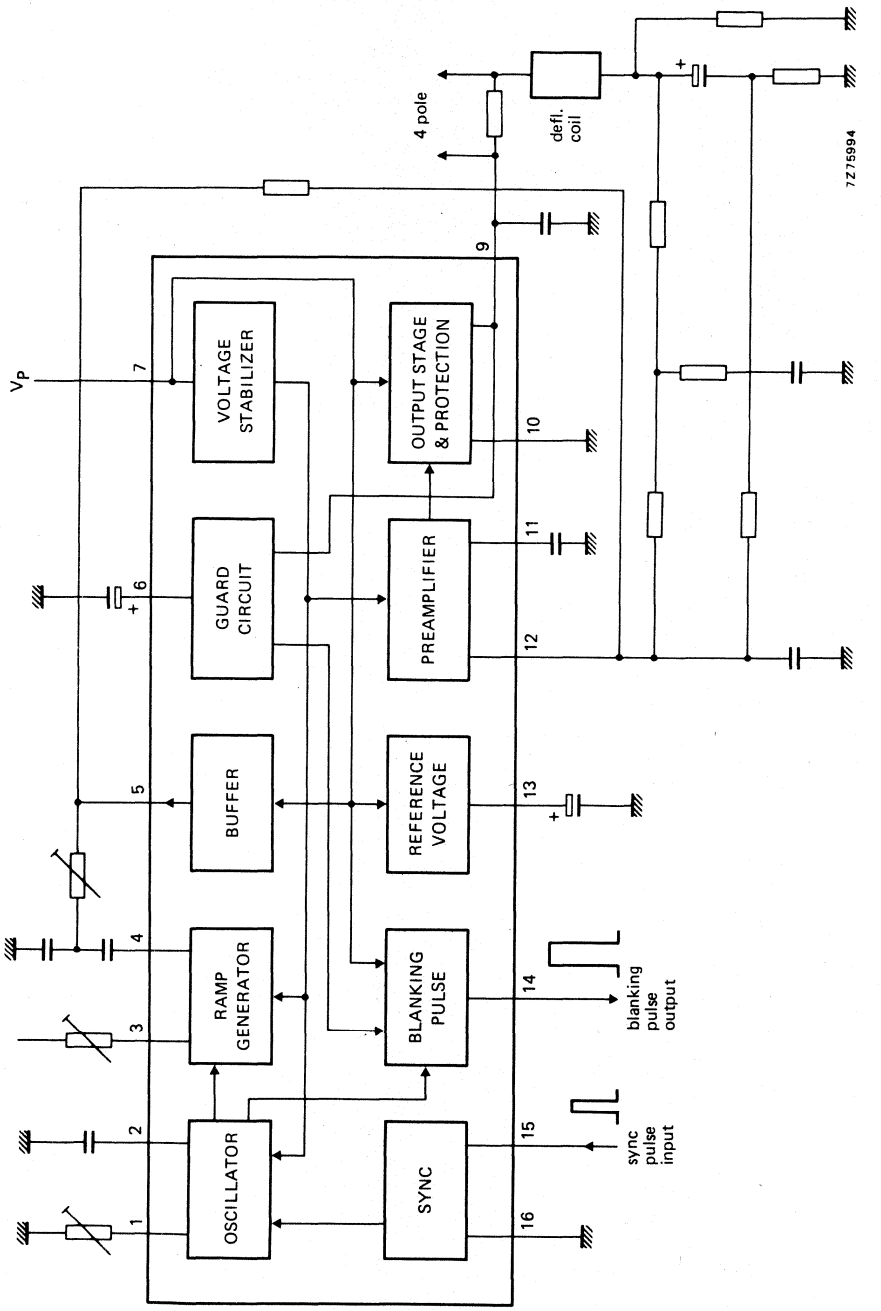


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Pin 2	V_{2-16}	max.	8 V
Pin 4	V_{4-16}	max.	50 V
Pin 7 (supply voltage)	V_{7-16} (V_P)	max.	50 V
Pin 9	V_{9-16}	max.	50 V
Pin 11	V_{11-16}	max.	50 V
Pin 12	V_{12-16}	max.	12 V
Pin 13	V_{13-16}	max.	50 V
Pin 15	V_{15-16}	max.	12 V

Currents

Pin 1	$-I_1$	max.	1 mA
Pin 3	I_3	max.	1 mA
Pin 5	I_5	max.	5 mA
Pin 6	I_6	max.	1 mA
Pin 7, 9, 10	Internally limited by short-circuit protection		
Pin 14	$\pm I_{14}$	max.	15 mA

Total power dissipation internally limited by the thermal protection circuit.

Storage temperature	T_{stg}	−25 to + 150	°C
Operating junction temperature	T_j	max. 150	°C

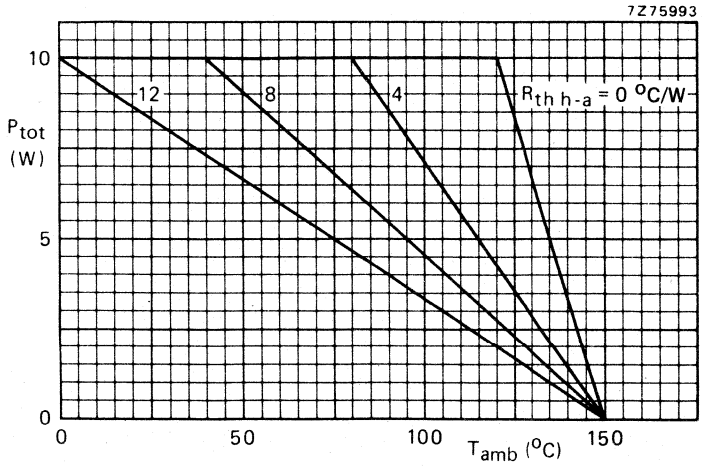


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes the $R_{th\ tab-h}$ which is expected when heatsink compound is used. $R_{th\ j-tab}$ = 3 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Supply voltage	$V_P = V_{7-16}$		15 to 35 V
Input voltage V_P = 30,5 V	V_{12-16}	typ. 	2,07 V 2,01 to 2,13 V
Input current V_P = 30,5 V	I_{12}	typ.	1 μA
Blanking pulse duration synchronized at 50 Hz	t_p	typ. 	1,4 ms 1,33 to 1,47 ms
Blanking pulse current	$\pm I_{14}$	typ.	12 mA
Blanking pulse generator output voltage $\pm I_{14}$ = 10 mA	V_{7-14} V_{14-16}	typ. typ.	1 V 1 V
Oscillator voltage (d.c.)	V_{1-16}	typ.	9 V
Sawtooth generator output voltage	V_{5-16}		1 to V_P–0,5 V
Sync pulse amplitude	V_{15-16}		1 to 12 V
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T$	typ.	0,0001 $°C^{-1}$
Oscillator voltage dependency V_P = 15 to 35 V	$(\Delta f/f)/\Delta V_P$	typ.	0,0004 V^{-1}
Junction temperature switching point thermal protection	T_j	typ. 	150 °C 142 to 158 °C
Synchronization range		typ.	15 %
Output voltage $-I_9$ = 2 A I_9 = 2 A	V_{9-16} V_{9-16}		V_P–2,3 to V_P–2,6 V 2,3 to 2,6 V
Output current	I_9	⩽	2 A

PINNING

1. Oscillator adjustment
2. Oscillator capacitor
3. Amplitude adjustment
4. Sawtooth capacitors
5. Output ramp oscillator
6. Guard circuit
7. Positive supply
8. n.c.
9. Output
10. Ground
11. Preamplifier
12. Preamplifier input
13. Reference voltage stage
14. Blanking output
15. Synchronization input
16. Ground.

APPLICATION INFORMATION

The function is described against the corresponding pin number

1.2. Oscillator
The frequency of the oscillator is determined by a potentiometer at pin 1 and a capacitor at pin 2.

3.4. Sawtooth generator
The timing of the ramp generator is determined by a potentiometer at pin 3 and a capacitor at pin 4. This capacitor has been split to realize linearity control.

5. Output ramp oscillator
This pin delivers a ramp signal which is used for linearity control, and drive of the preamplifier. The ramp signal is applied via a shaping network to pin 4 (linearity) and via a resistor to pin 12 (preamplifier).

6. Guard circuit input
When a capacitor is connected between this pin and ground a continuous blanking signal is available at pin 14 in case of missing vertical deflection current.
When no continuous blanking is required this capacitor is replaced by a resistor between pin 6 and pin 7.

7. Positive supply
No voltage stabilizer is necessary resulting in optimum tracking with line deflection. The internal stabilizer delivers the voltage for the oscillator, ramp generator and preamplifier.

8. Not connected.

9. Output of class B power stage
The deflection coil is connected to this pin, via a four-pole network, a coupling capacitor and a feedback resistor, to ground.

10. Ground for output stage.

11. Preamplifier
The cut-off frequency of the internal differential amplifier (preamplifier) is adjusted with the capacitor between pin 11 and ground.

12. Preamplifier input
The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the ramp voltage at pin 5 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

13. Reference voltage stage
The bias stage of the preamplifier is decoupled at this pin.

14. Blanking output
The maximum pulse amplitude with no load is V_P. When I_{14} is 10 mA the amplitude of the pulse is 1 V.

15. Synchronization input
The oscillator has to be synchronized by a positive-going pulse of between 1 and 12 V.

16. Ground of small signal part.

APPLICATION INFORMATION (continued)

			20AX (Fig. 3)	30AX (Fig. 4)
Supply voltage	V_S	typ.	33 V	35 V
Output voltage (d.c.)	$V_{9\text{-}16}$	typ.	17 V	16 V
Output voltage (peak value)	$V_{9\text{-}16}$	typ.	36 V	43 V
Supply current	I_7	typ.	500 mA	290 mA
Deflection current (peak-to-peak value)	$I_{(p\text{-}p)}$	typ.	3,6 A	2,1 A
Output current (peak-to-peak value)	$\pm I_{9(p\text{-}p)}$	typ.	1,9 A	1,1 A
Flyback time	t_{fl}	typ.	0,85 ms	1,2 ms
Total power dissipation in I.C.	P_{tot}	typ.	8,5 W *	4 W **
Blanking time	t_b	typ.	1,4 ms	1,4 ms
Non-linearity		$<$	3 %	3 %

* For 20AX systems the heatsink has to be constructed for $P_{tot} < 10$ W, $R_{th\ h\text{-}a} = 4$ °C/W at $T_{amb} = 60$ °C.

** For 30AX systems the heatsink has to be constructed for $P_{tot} < 5$ W, $R_{th\ h\text{-}a} = 8{,}5$ °C/W at $T_{amb} = 60$ °C.

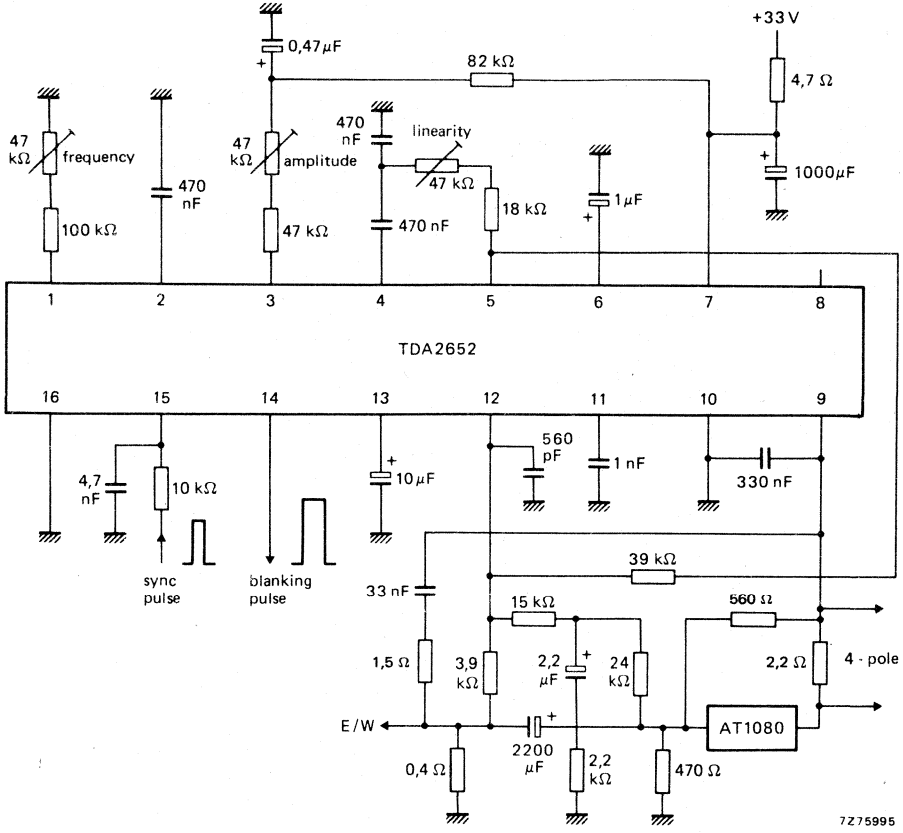


Fig. 3 Complete vertical deflection circuit for 20AX.

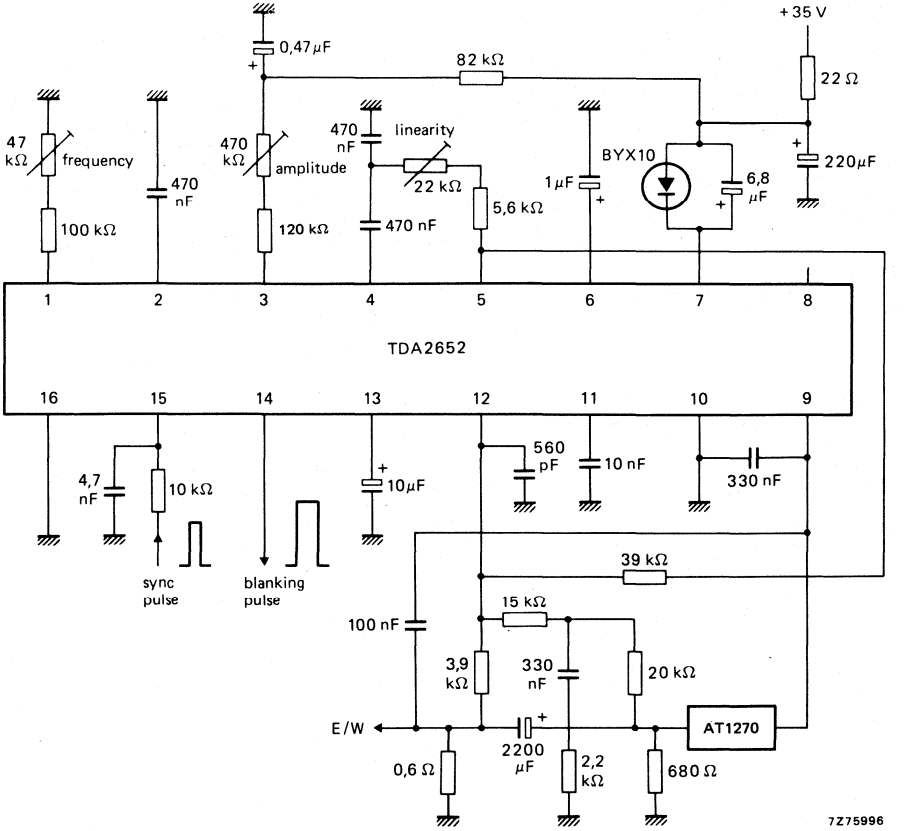


Fig. 4 Complete vertical deflection circuit for 30AX.

VERTICAL DEFLECTION CIRCUIT

The TDA2653 is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Frequency detector and storage
- Sawtooth generator
- Amplitude switch for 50 Hz/60 Hz
- Buffer stage
- Reference voltage unit
- Preamplifier
- Output stage
- Flyback generator
- Voltage stabilizer
- Guard circuit
- Output stage protections

QUICK REFERENCE DATA

Supply voltage range (pin 6)	$V_{6\text{-}16} = V_P$		9 to 50 V
Output current (peak-to-peak value)	$I_{9(p\text{-}p)}$	typ.	2,4 A
Operating junction temperature	T_j	max.	150 °C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\ j\text{-}mb}$	typ.	5 K/W

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69C).

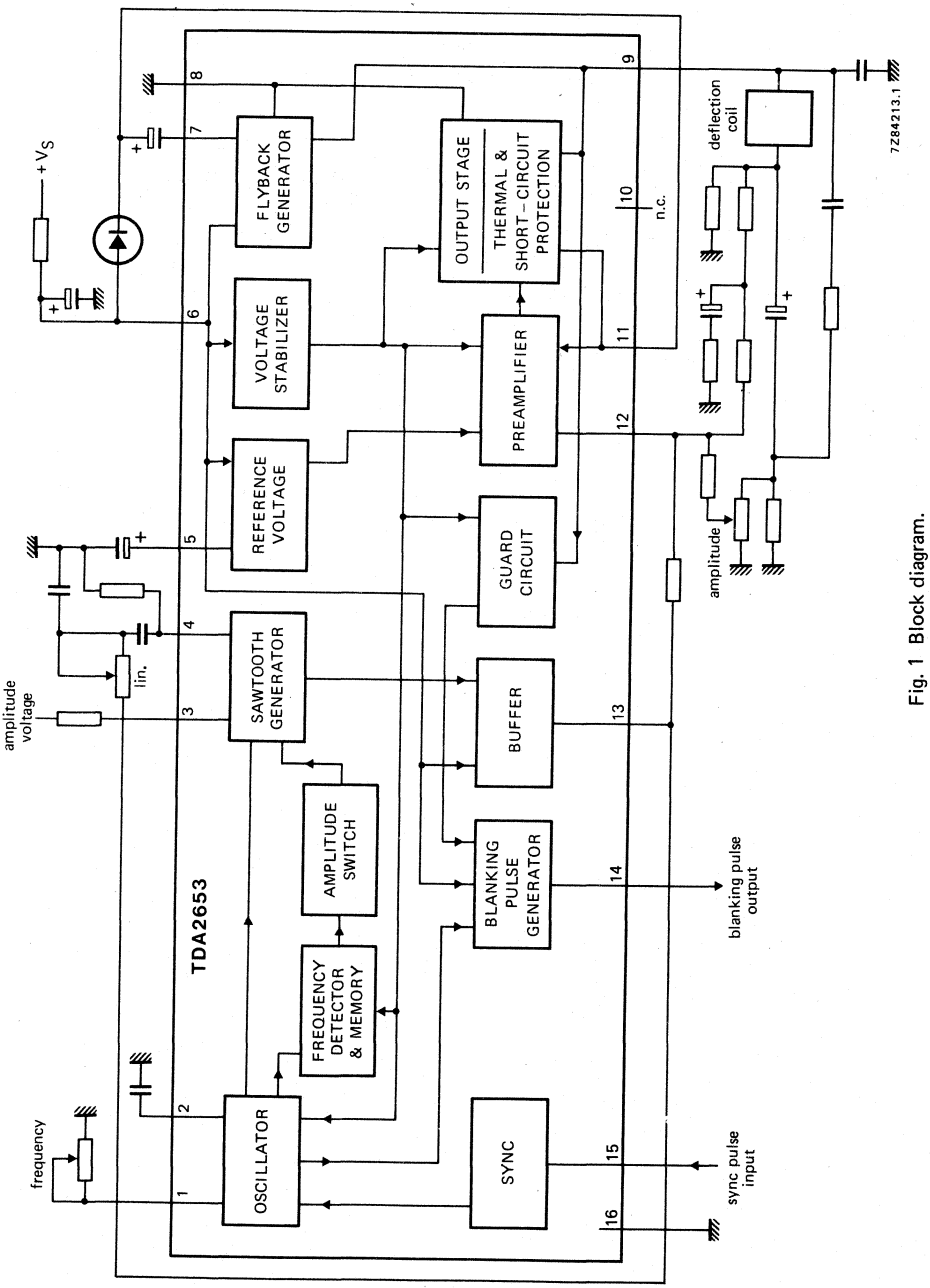


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages			
Pin 2; oscillator voltage	$V_{2\text{-}16}$	max.	7 V
Pin 4; sawtooth voltage	$V_{4\text{-}16}$	max.	40 V
Pin 5; decoupling reference voltage	$V_{5\text{-}16}$	max.	40 V
Pin 6; supply voltage	$V_{6\text{-}16} = V_P$	max.	40 V
Pin 7; output voltage flyback generator	$V_{7\text{-}16}$	max.	40 V
Pin 9; output voltage	$V_{9\text{-}16}$	max.	50 V
Pin 11; supply voltage output stage	$V_{11\text{-}16}$	max.	50 V
Pin 12; input voltage preamplifier	$V_{12\text{-}16}$	max.	12 V
Pin 15; sync voltage	$V_{15\text{-}16}$	max.	30 V
Currents			
Pin 1; oscillator	$-I_1$	max.	1 mA
Pin 3; sawtooth generator	I_3	max.	1 mA
Pin 7; flyback generator	I_7		−1,5 to + 1,2 A
Pins 8, 9, 10; internally limited by the short-circuit protection circuit			
Pin 14; blanking pulse	$\pm I_{14}$	max.	15 mA
Total power dissipation; internally limited by the thermal protection circuit (see also Fig. 2)			
Storage temperature	T_{stg}		−25 to + 150 °C
Operating junction temperature	T_j	max.	150 °C

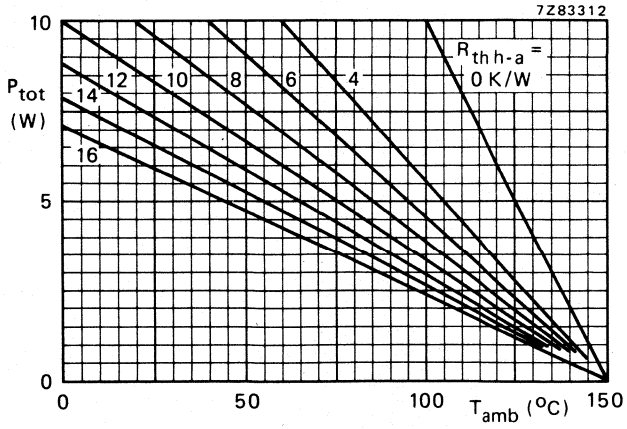


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heatsink compound is used. $R_{th\ j\text{-}mb}$ = 5 K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Supply voltage	$V_{6-16} = V_P$		9 to 50	V*
Supply voltage output stage	V_{11-16}		9 to 50	V
Maximum flyback generator output voltage	V_{7-16}	typ.	V_P–2,2	V
Preamplifier input voltage	V_{12-16}	typ.	2	V
Preamplifier input current	$-I_{12}$	typ.	1	μA
Sync input voltage	V_{15-16}		1 to 12	V
Sawtooth generator output current at I_3 = 50 μA				
synchronized at 50 Hz	I_4	typ.	50	μA
synchronized at 60 Hz	I_4	typ.	60	μA
Sawtooth generator output voltage	V_{13-16}		1,2 to V_P–0,5	V
Oscillator voltage (d.c.)	V_{1-16}		6 to 9	V
Output voltage at $I_{9(p-p)}$ = 2,2 A				
minimum	V_{9-16}	typ.	1,3	V
maximum	V_{9-16}	typ.	V_{11-16}–1,9	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	<	2,4	A
Current at pin 7	$\pm I_7$	<	1,2	A
Voltage at pin 7 during flyback	V_{7-16}	typ.	V_P–2,2	V
Blanking pulse generator output voltage $\pm I_{14}$ = 10 mA	V_{14-16}	typ.	6	V
	V_{6-14}	typ.	6	V
Blanking pulse output current	$\pm I_{14}$	<	12	mA
Blanking pulse duration at 50 Hz	t_b		1,4 ± 0,07	ms
Tracking range oscillator		typ.	28	%
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T$	typ.	0,0001	K^{-1}
Oscillator voltage dependency V_P = 10 to 30 V	$(\Delta f/f)/\Delta V_P$	typ.	0,0004	V^{-1}
Junction temperature switching point thermal protection	T_j	typ.	150 ± 8	°C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\ j\text{-}mb}$	typ.	5	K/W

* When the flyback generator is used, the maximum supply voltage must be chosen such that during flyback the voltage at pin 11 (supply voltage output stage) does not exceed 50 V.

PINNING

1. Oscillator adjustment
2. Oscillator capacitor
3. Amplitude adjustment
4. Sawtooth capacitor
5. Reference voltage decoupling
6. Positive supply
7. Flyback generator output
8. Negative supply (ground) of output stage
9. Output
10. n.c. (not connected)
11. Positive supply of output stage
12. Preamplifier input
13. Output of sawtooth buffer stage
14. Blanking output
15. Synchronization input
16. Negative supply (ground) of small signal part

APPLICATION INFORMATION

The function is described against the corresponding pin number

1. 2. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 2.

3. 4. Sawtooth generator

The timing of the sawtooth generator is determined by a potentiometer at pin 3 and a capacitor at pin 4. This capacitor has been split to realize linearity control.

5. Reference voltage decoupling

An electrolytic capacitor connected from this pin to ground, suppresses the ripple voltage on the supply voltage, from which, via an internal resistor divider the reference voltage is derived.

6. Positive supply

The supply voltage at this pin is used to supply the flyback generator, the voltage stabilizer, reference voltage unit, buffer stage and blanking pulse generator.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 11 to complete the flyback generator.

8. Negative supply (ground) of output stage

9. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

10. Not connected

11. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 11 and 7, and a diode between pins 6 and 11 have to be connected for proper operation of the flyback generator.

12. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 13 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

13. Output of sawtooth buffer stage

The sawtooth signal is fed via a buffer stage to pin 13. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 4 (linearity) and via a resistor to pin 12 (preamplifier).

APPLICATION INFORMATION (continued)

14. Blanking output

    The maximum pulse amplitude with no load is V_P. When I_{14} is 10 mA the amplitude of the pulse is 6 V.

15. Synchronization input

    The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector, with storage and amplitude switch, takes care of automatic recognition and processing of 50 Hz or 60 Hz signals.

16. Negative supply (ground) of small signal part.

The following application data are measured in a typical 30AX system (Fig. 3).

Supply voltage	$V_P = V_{6-16}$	typ.	26	V
Output voltage (d.c. value)	V_{9-16}	typ.	14	V
Output voltage (peak value)	V_{9-16}	typ.	42	V
Supply current	$I_3 + I_6$	typ.	310	mA
Output current (peak-to-peak value)	$I_{9(p-p)}$	typ.	2,1	A*
Flyback time	t_{fl}	typ.	0,85	ms
Blanking time	t_b	typ.	1,46	ms
Total power dissipation in IC	P_{tot}	typ.	4	W
Total power consumption	P	typ.	8,1	W
Non-linearity		<	2	%
Thermal resistance of heatsink	$R_{th\ h-a}$	typ.	10	K/W

* Including 6% overscan.

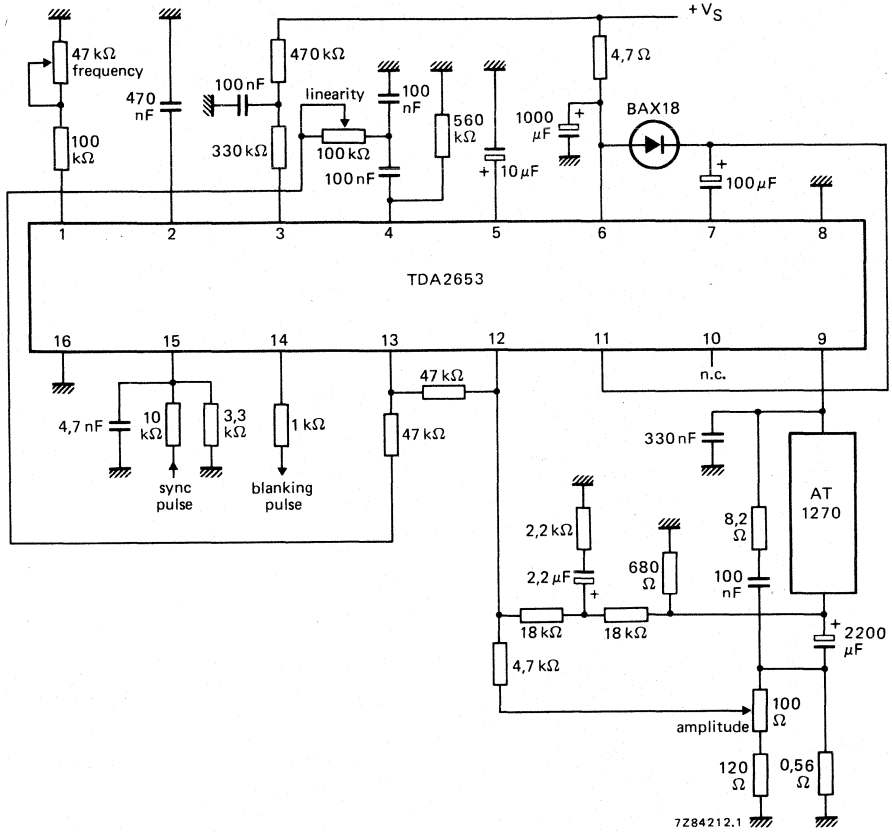


Fig. 3 Complete vertical deflection circuit for 30AX.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{G(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

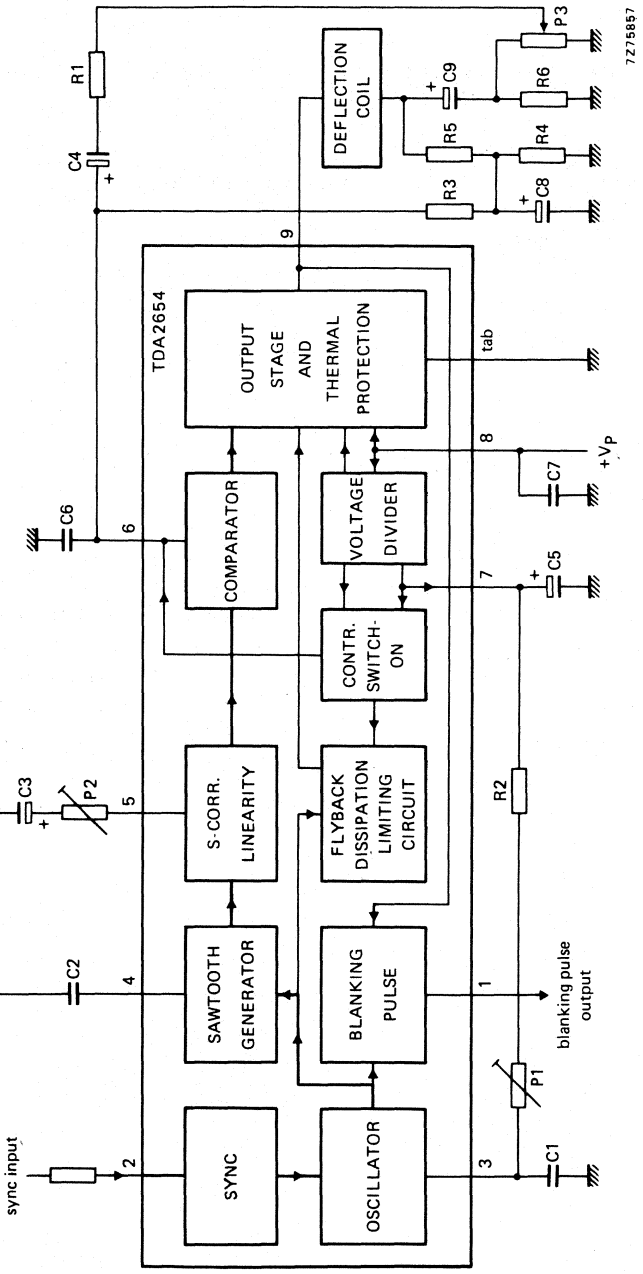


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages			
Pin 2	V_2	max.	5 V
Pin 3	V_3	max.	17 V
Pin 4	V_4	max.	17 V
Pin 5	V_5	max.	6 V
Pin 6	V_6	max.	13 V
Pin 7	V_7	max.	18 V
Pin 8	V_8 (V_P)	max.	35 V
Currents			
Pin 1	$+I_1$	max.	1 mA
	$-I_1$	max.	5 mA
Pin 2	I_2	max.	2,5 mA
Pin 3	I_3	max.	30 mA
Pin 4	I_4	max.	30 mA
Pin 5	$\pm I_5$	max.	1 mA
Pin 6	$\pm I_6$	max.	3 mA
Pin 9 (repetitive)	$\pm I_9$	max.	1 A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5 A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5 W
Storage temperature	T_{stg}	−25 to + 150	°C
Operating junction temperature	T_j	max.	150 °C

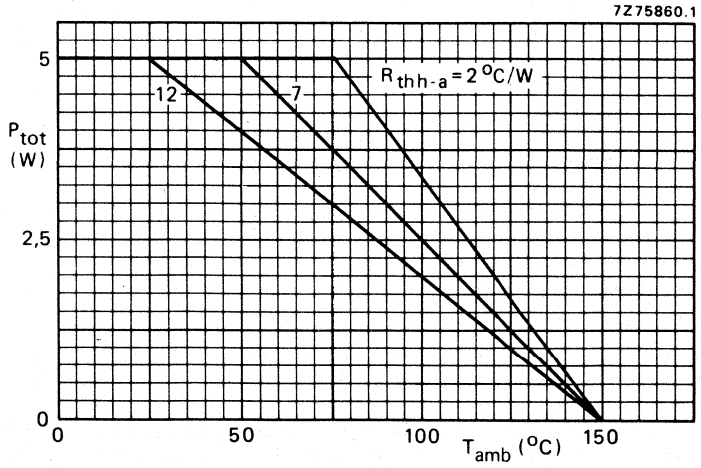


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\,tab-h}$ = 1 °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\,j-tab}$ = 12 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9\,(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9\,(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	−0,01	−0,01	Hz/°C
Oscillator voltage shift		typ.	−0,13	−0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

The value depends on the deflection coil.

9. Output

The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

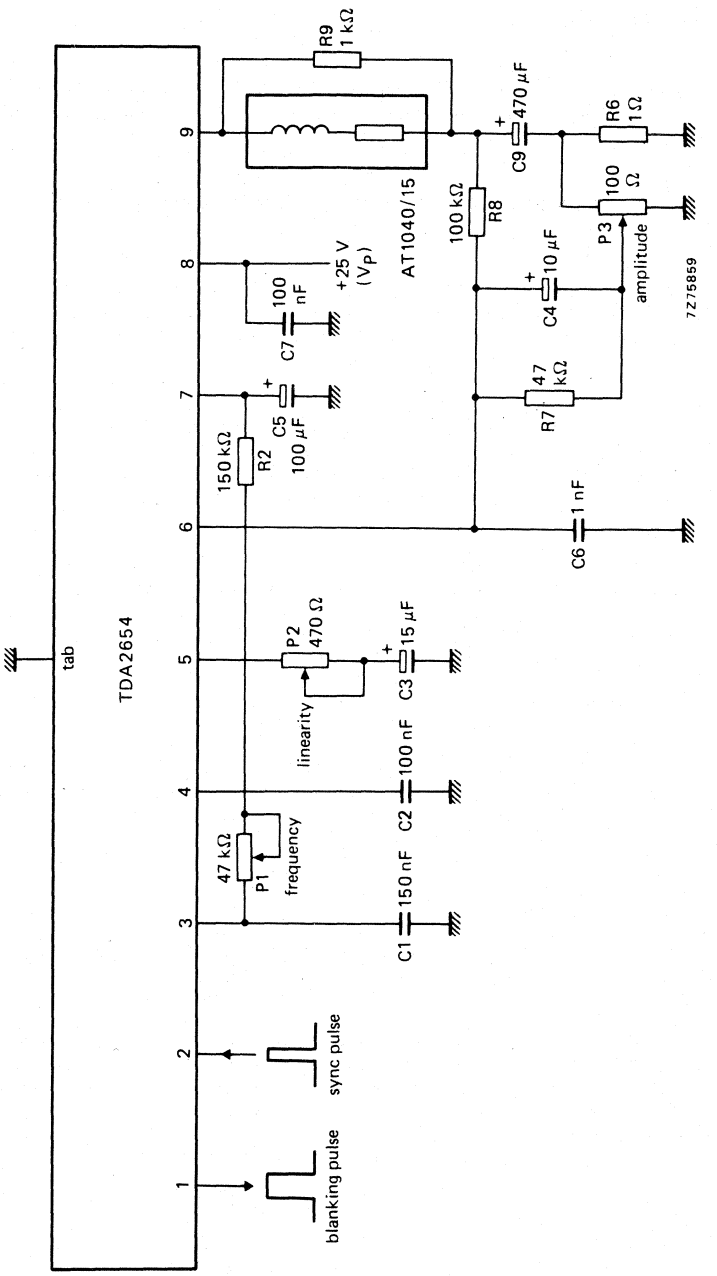
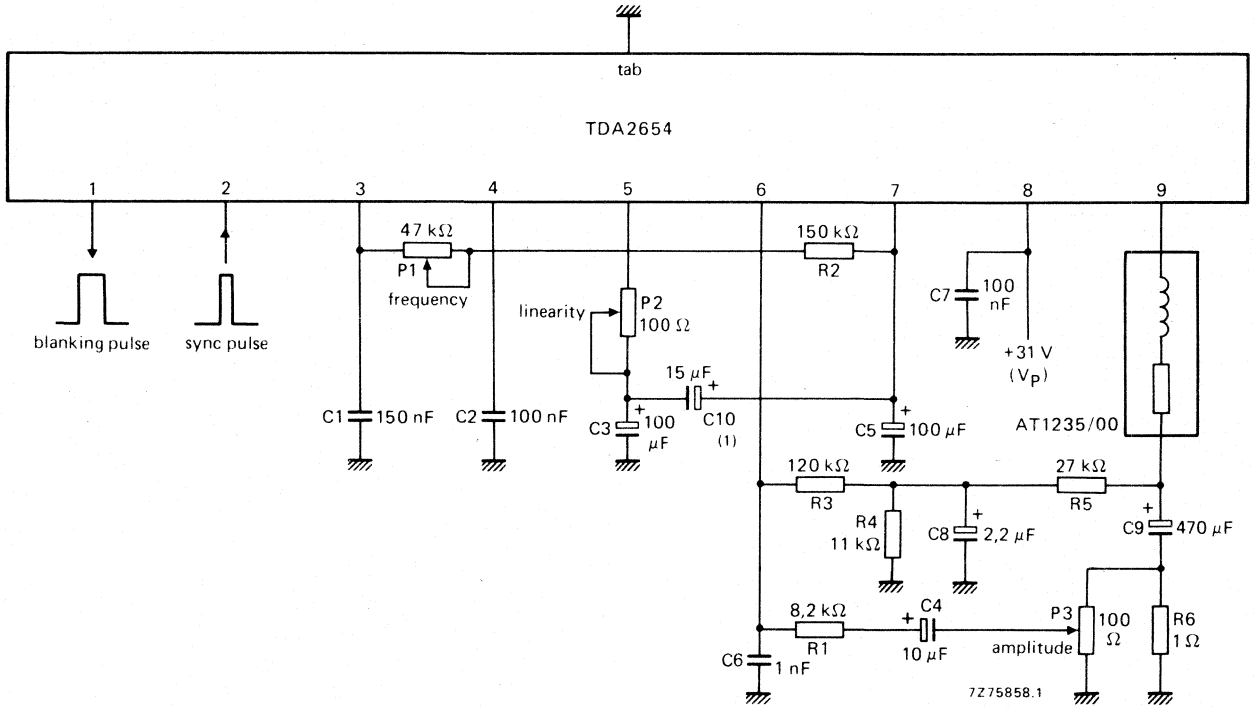


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)



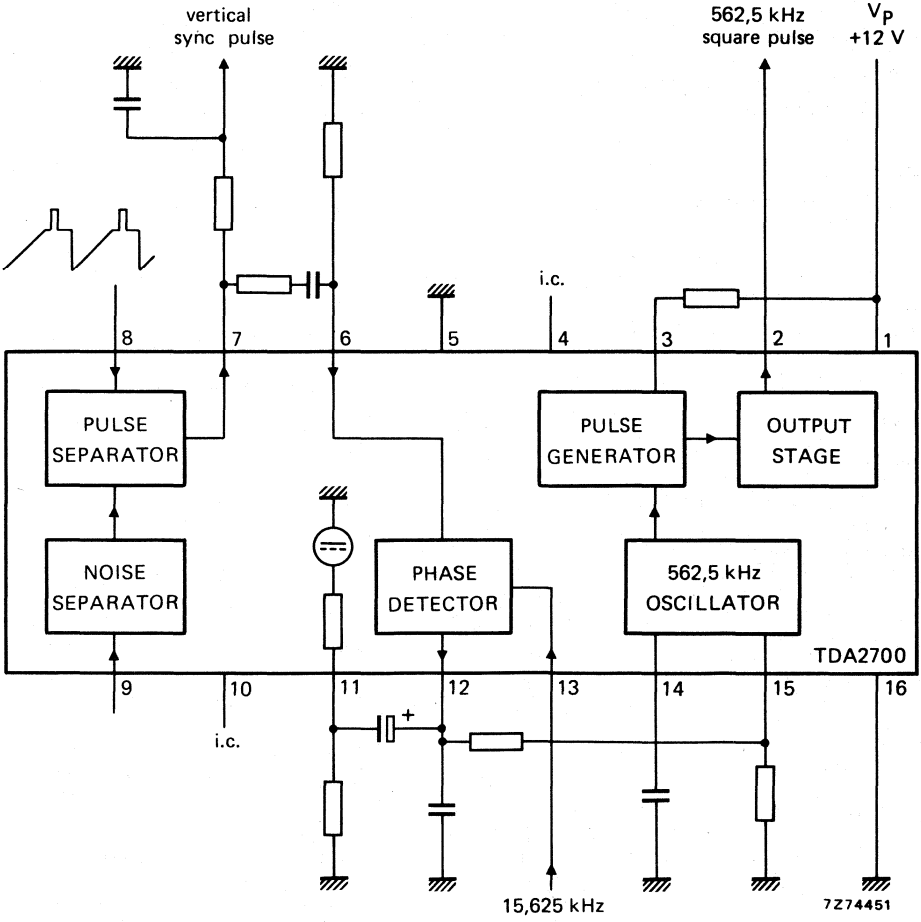
(1) Only required when rapid variations in the supply voltage are expected.

Fig. 4 Colour 90° vertical deflection system.

OSCILLATOR FOR VIDEO RECORDERS

The TDA2700 is a monolithic integrated circuit for video recorders incorporating the following functions :

- 562, 5 kHz oscillator
- pulse separator
- noise separator
- phase detector
- pulse generator
- low-ohmic output stage



PACKAGE OUTLINE 16-lead DIL; plastic (SOT-38).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Supply voltage	V_{1-16}	max.	13,2	V
Pin 3	V_{3-16}	0 to	V_{1-16}	V
Pin 8	$-V_{8-16}$	max.	12	V
Currents				
Pin 2 (average value)	$-I_{2(AV)}$	max.	20	mA
(peak value)	$-I_{2M}$	max.	200	mA
Pin 6 (peak value)	$\pm I_{6M}$	max.	10	mA
Pin 7 (peak value)	$-I_{7M}$	max.	10	mA
Pin 8 (peak value)	I_{8M}	max.	10	mA
Pin 9 (peak value)	$\pm I_{9M}$	max.	10	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	600	mW
Temperatures				
Storage temperature	T_{stg}	−25 to	+125	°C
Operating ambient temperature	T_{amb}	−20 to	+60	°C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C; measured in circuit on page 4

Inputs

Supply				
Supply current at $I_2 = 0$	I_1	typ.	36	mA
Sync pulse separator				
Negative video input signal (peak-to-peak value)	$V_{8-16(p-p)}$	typ.	3	V
			1 to 7	V
Input current (peak value)	I_{8M}	≥	10	μA
Input leakage current at $V_{8-16} = -3$ V	$-I_8$	≤	1	μA
Noise separator				
Input voltage	V_{9-16}	typ.	0,7	V
Input current range	I_9	0,03 to	10	μA
Input resistance	R_{9-16}	typ.	200	Ω

CHARACTERISTICS (continued)

Outputs

Sync pulse separator

Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	10	V	
Output resistance : at leading edge of sync pulse	R_{7-16}	typ.	50	Ω	1)
at trailing edge of sync pulse	R_{7-16}	typ.	2,2	kΩ	
Additional external load resistance	$R_{7-16(ext)}$	≥	2	kΩ	

Output stage

Output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V	
Output resistance	R_{2-16}	low-ohmic			
Duty factor of output pulse	δ	typ.	50	%	

Phase detector

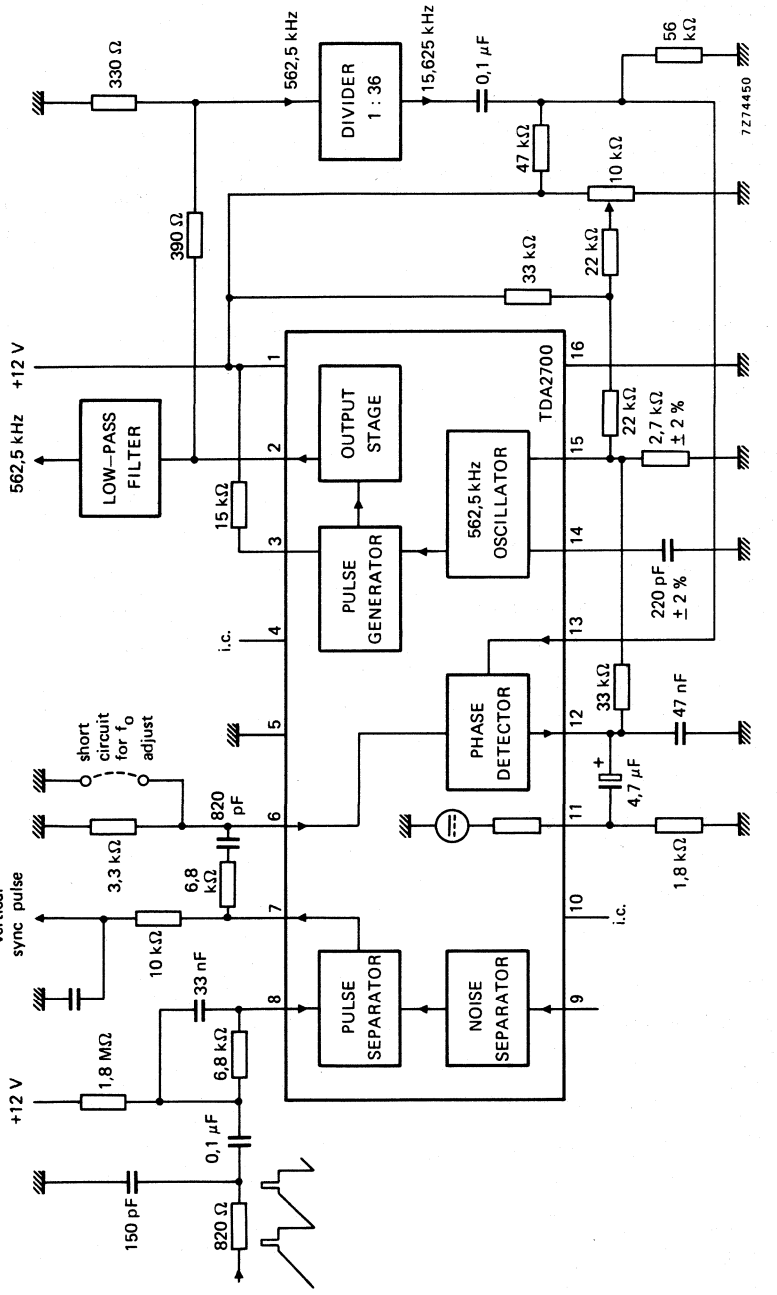
Input voltage	V_{6-16}	typ.	1,5	V	
Input current range	I_6		0,03 to 3	mA	
Control voltage range	V_{12-16}		1,3 to 5,5	V	
Output resistance in the control voltage range	R_{12-16}	high-ohmic			2)
Control current	$\pm I_{12}$	typ.	7,5	mA	
Input voltage range for I_{12} positive	V_{13-16}		7,2 to 9	V	
for I_{12} negative	V_{13-16}		0 to 5,5	V	
Input current at $V_{13-16} \geq 7,2$ V	I_{13}	<	6	μA	
at $V_{13-16} \leq 5,5$ V	I_{13}	<	1	μA	
Catching and holding range (based on 15,625 kHz)	Δf	typ.	±1	kHz	3)
D.C. level at pin 11	V_{11-16}	typ.	3,1	V	
Internal resistance at pin 11	R_{11-16}	typ.	2	kΩ	

Oscillator

Output voltage (peak-to-peak value)	$V_{14-16(p-p)}$	typ.	3	V	
Charge and discharge current	$I_{14} = \pm I_{15}$	typ.	0,94	mA	
Voltage at pin 15	V_{15-16}	typ.	3,1	V	
Frequency ; free running	f_o	typ.	562,5	kHz	
Frequency adjustment range	$\Delta f_o/f_o$	typ.	10	%	

1) Emitter follower.
2) Current source.
3) Adjustable with $R_{12-15(ext)}$.

APPLICATION INFORMATION

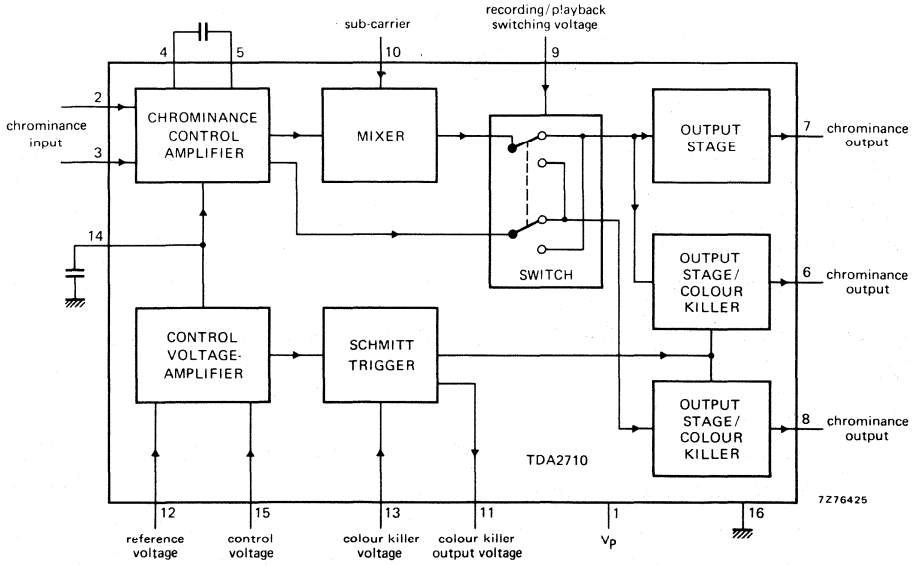


CHROMINANCE SIGNAL/MIXER FOR VIDEO RECORDERS

The TDA2710 is a monolithic integrated circuit for video recorders incorporating the following functions:

- controlled chrominance amplifier
- control voltage amplifier
- mixer for the chrominance signal
- electronic recording/playback switch
- Schmitt trigger for killing the chrominance signal
- colour killer output stage

BLOCK DIAGRAM



PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Supply voltage (pin 1)	V_P (V_{1-16})	0 to 13,2		V
At pin 4	V_{4-16}	0 to V_P		V
At pin 5	V_{5-16}	0 to V_P		V
At pin 12	V_{12-16}	0 to V_P		V
At pin 13	V_{13-16}	0 to V_P		V
At pin 15	V_{15-16}	0 to V_P		V
At pin 9	$\pm V_{9-16}$	max.	4	V
Currents				
At pin 6	$-I_6$	max.	5	mA
At pin 7	$-I_7$	max.	5	mA
At pin 8	$-I_8$	max.	5	mA
At pin 11	I_{11}	max.	5	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	700	mW
Temperatures				
Storage temperature	T_{stg}	−25 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +60		°C

CHARACTERISTICS at V_P = 12 V; T_{amb} = 25 °C; measured in circuit on page 4

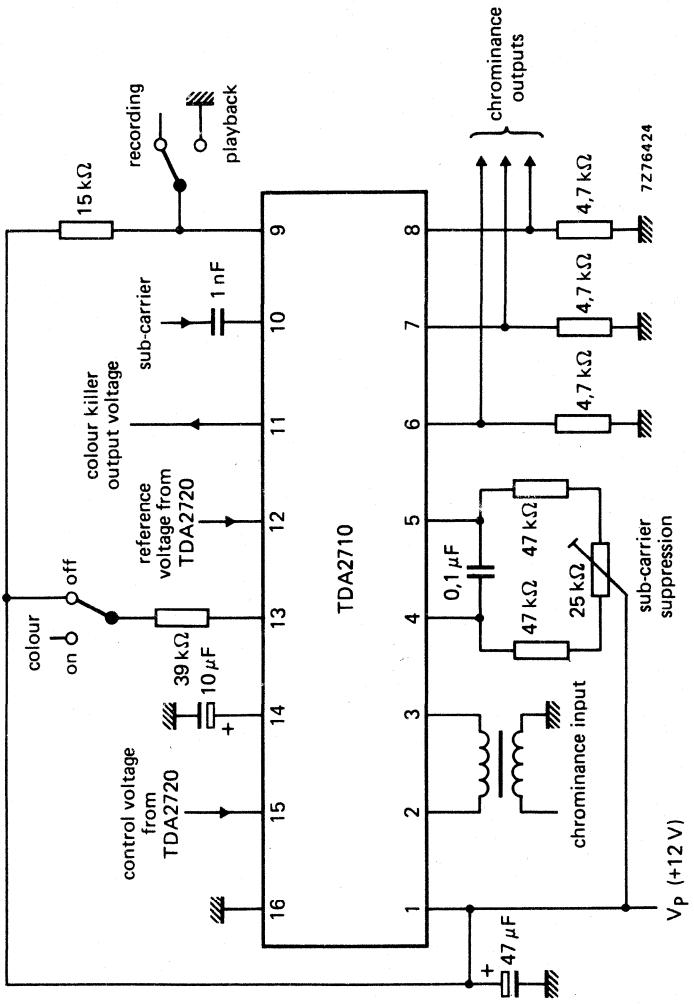
Inputs

Chrominance input (pins 2 and 3)				
Input resistance	$R_{2;3-16}$	typ.	3,3	kΩ
D.C. input voltage (without signal)	$V_{2;3-16}$	typ.	5,9	V
Input voltage range at a peak-to-peak burst of 0,5 V	$V_{2;3-16}$	2,5 to 75		mV
Sub-carrier (pin 10)				
Input resistance	R_{10-16}	typ.	2	kΩ
D.C. input voltage (without signal)	V_{10-16}	typ.	4,4	V
Input voltage range (peak-to-peak value)	$V_{10-16(p-p)}$	60 to 500		mV

CHARACTERISTICS (continued)

Reference voltage (pin 12)				
External reference voltage	V_{12-16}	typ.	7	V
Control voltage (pin 15)				
Voltage at control voltage input				
for colour on	V_{15-16}	≤	5,7	V
for colour off	V_{15-16}	≥	6,1	V
Colour killer input (pin 13)				
Input voltage for colour off	V_{13-16}	≥	6	V
Recording/playback switch (pin 9)				
Input resistance	R_{9-16}	typ.	1	kΩ
Input voltage : for recording	V_{9-16}	≤	0,3	V
for playback	V_{9-16}	≥	0,85	V
Outputs				
Colour killer output (pin 11)				
Output resistance for colour on	R_{11-1}	typ.	10	kΩ
Output voltage for colour off	V_{11-16}	≤	0,5	V
Recording				
Output voltages (peak-to-peak values) at a peak-to-peak burst of 0,5 V	$V_{6;7-16(p-p)}$	typ.	0,5	V
Output voltage at pin 8 (peak-to-peak value) at $V_{6-16(p-p)}$ = 0,5 V	$V_{8-16(p-p)}$	0,35 to	0,5	V
Playback				
Sub-carrier suppression at pins 6 and 7 at $V_{10-16(p-p)}$ = 300 mV; $V_{6-16(p-p)}$ = $V_{7-16(p-p)}$ = 1 V; sub-carrier suppression at pins 4 and 5		≥	60	dB

APPLICATION INFORMATION

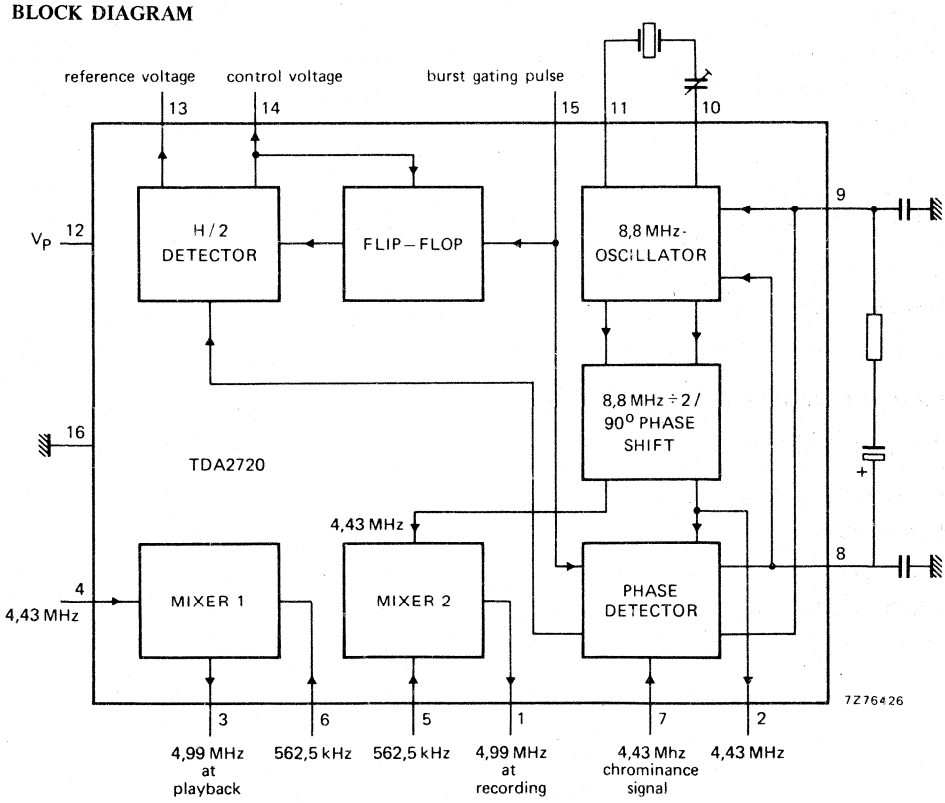


COLOUR SUB-CARRIER OSCILLATOR FOR VIDEO RECORDERS

The TDA2720 is a monolithic integrated circuit for video recorders incorporating the following functions:

- 8,8 MHz colour sub-carrier oscillator with divider stage
- keyed phase comparison for optimum noise behaviour
- a stage to obtain automatic chrominance control
- a stage to obtain a colour killer signal and an identification signal
- 2 mixer stages to obtain the 4,99 MHz sub-carrier frequency

BLOCK DIAGRAM



PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Supply voltage (pin 12)	V_P (V_{12-16})	max.	13,2	V
At pin 1	V_{1-16}		0 to V_P	V
At pin 2	V_{2-16}	min.	0	V
At pin 3	V_{3-16}		0 to V_P	V
At pins 5, 6, 7 and 11	$V_{5;6;7;11-16}$	min.	0	V
At pin 13	V_{13-16}		0 to V_P	V
At pin 14	V_{14-16}		0 to V_P	V
At pin 15	V_{15-16}		0 to V_P	V
Currents				
At pins 2, 5 and 6	$I_{2;5;6}$	max.	5	mA
At pins 7, 11 and 13	$I_{7;11;13}$	max.	5	mA
At pin 10	$-I_{10}$	max.	2	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	750	mW
Temperatures				
Storage temperature	T_{stg}		−25 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

CHARACTERISTICS at V_P = 12 V; T_{amb} = 25 °C

Supply current (pin 12)	I_{12}	typ.	40	mA
8,8 MHz oscillator				
Input resistance	R_{11-16}	typ.	270	Ω
Output resistance	R_{10-16}	typ.	200	Ω
Overall holding range	Δ_f	typ.	±500	Hz
Oscillator output voltage	V_{10-16}	typ.	10	V

CHARACTERISTICS (continued)

Reference voltage part

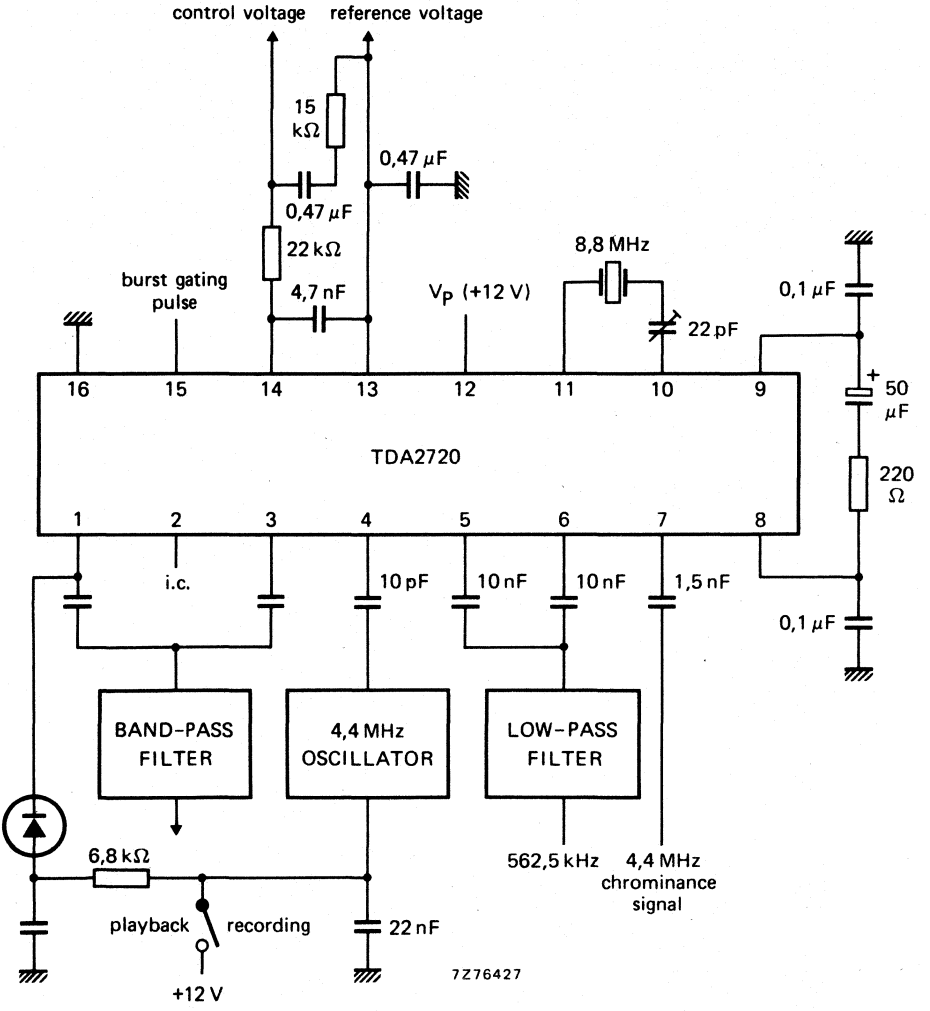
Burst signal (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	0,5	V
Linear output voltage range (peak-to-peak value)	$V_{7-16(p-p)}$	≤	1,5	V
D.C. voltage at pin 14 with a peak-to-peak burst of 0,5 V	V_{14-16}	typ.	5,5	V
without burst	V_{14-16}	typ.	7,0	V
Reference voltage	V_{13-16}	typ.	7,0	V
Burst keying pulse	V_{15-16}	≥	2,0	V
Voltage at pin 2; 4,4 MHz (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	0,5	V

Mixer

Carrier suppression at 1 V peak-to-peak; 4,99 MHz [1]				
Recording mixer		≥	20	dB
Playback mixer		≥	20	dB
Gain for both mixers	G	typ.	7	
Gain variation	ΔG	≤	3	dB
Gain difference of mixers	ΔG	≤	3	dB
Linear output voltage range (peak-to-peak value) pin 5	$V_{5-16(p-p)}$	≤	0,6	V
pin 6	$V_{6-16(p-p)}$	≤	0,6	V
Voltage at pin 4; 4,4 MHz (peak-to-peak value)	$V_{4-16(p-p)}$	typ.	0,4	V
D.C. voltage at pin 4	V_{4-16}	typ.	5,0	V
at pin 5	V_{5-16}	typ.	3,5	V
at pin 6	V_{6-16}	typ.	3,5	V

[1]) Pin 4 connected to pin 2 via a 1 nF capacitor.

APPLICATION INFORMATION

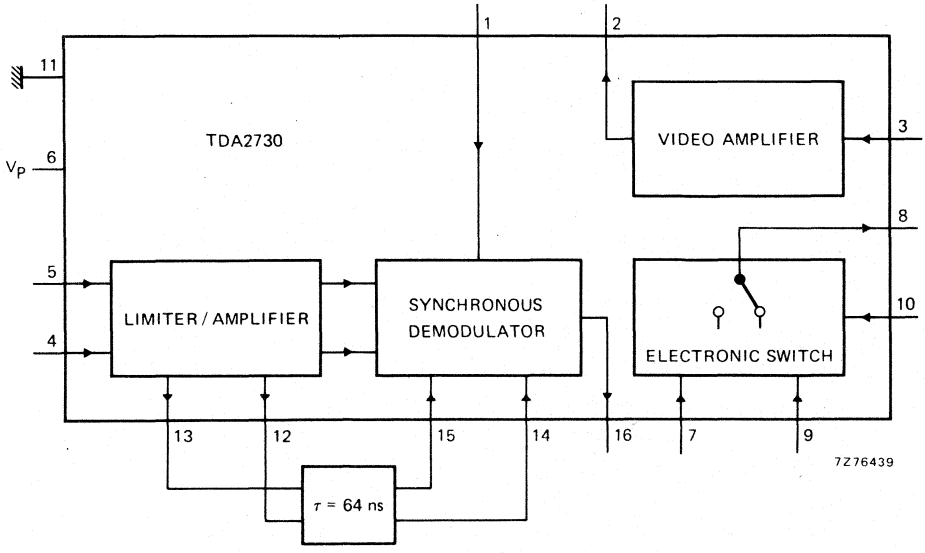


FM LIMITER/DEMODULATOR

The TDA2730 is a monolithic integrated circuit for use in audio-visual equipment, e.g.; video recorders and video disc players.
The circuit comprises an f.m. limiter/demodulator for the playback signal, a video amplifier and an electronic switch, which can be used for drop-out elimination.

QUICK REFERENCE DATA				
Supply voltage	V_{6-11}	typ.	12	V
Supply current	I_6	typ.	42	mA
Input signal range (peak-to-peak value)	$V_{4-5(p-p)}$		30 to 2000	mV
Video output signal (peak-to-peak value)	$V_{2-11(p-p)}$	typ.	4	V

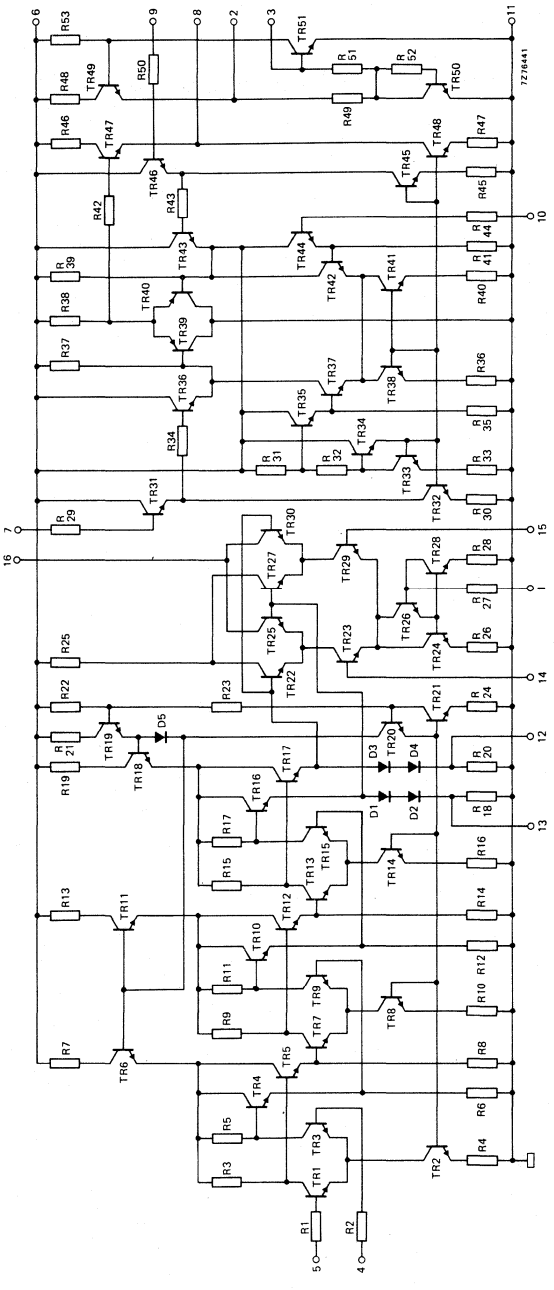
BLOCK DIAGRAM



PACKAGE OUTLINE

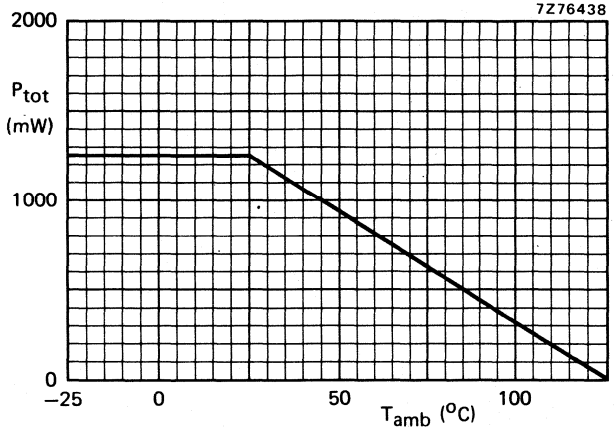
16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{6-11}	max.	13	V
Power dissipation				
Total power dissipation (see also derating curve below)	P_{tot}	max.	1,25	W
Temperatures				
Storage temperature	T_{stg}		−65 to +125	°C
Operating ambient temperature			see derating curve below	



CHARACTERISTICS measured in the circuit on page 7 (Fig. 1)

Supply voltage range	V_{6-11}	typ.	12	V
			11 to 13	V

The following characteristics are measured at V_{6-11} = 12 V; T_{amb} = 25 °C

Supply current	I_6	typ.	42	mA
			25 to 54	mA

Limiter

Start of limiting (−3 dB) f_o = 4 MHz; peak-to-peak value	$V_{4-5(p-p)}$	typ.	0,8	V
Input signal range for constant luminance output (peak-to-peak value)	$V_{4-5(p-p)}$	30 to 2000		mV
Output voltage (peak-to-peak value)	$V_{12-13(p-p)}$	typ.	750	mV
Available output voltage at an external load of 1 kΩ; peak-to-peak value	$V_{12-13(p-p)}$	>	5	V

Demodulator

Measured at I_1 = 4 mA; $|Z_{16-11}|$ = 1,5 kΩ; delay time τ = 64 ns; Δf = 1,4 MHz (f_L = 3,0 MHz, f_H = 4,4 MHz)

Current ratio	I_1/I_{16}	typ.	1	
Output voltage (peak-to-peak value)	V_{16-11}	typ.	540	mV

Drop-out switch

Input drive voltage range	$V_{7;9-11}$	6,5 to 12		V
Voltage drop between input and output for signal flow from pin 7 to pin 8	V_{7-8}	typ.	1,5	V
for signal flow from pin 9 to pin 8	V_{9-8}	typ.	1,5	V
Input offset voltage	$\lvert V_{7-8}-V_{9-8}\rvert$	<	20	mV
Switch actuating input voltage for signal flow from pin 7 to pin 8	V_{10-11}	0 to 2,7		V
for signal flow from pin 9 to pin 8	V_{10-11}	3,7 to 6,0		V
Output impedance at 1,5 mA by internal load	Z_{8-11}	emitter follower		

CHARACTERISTICS (continued)

Video amplifier

Input voltage level	V_{3-11}	typ.	730	mV
Output voltage level	V_{2-11}	typ.	5,5	V
Open loop gain	G	typ.	43	dB
Bandwidth (3 dB)	B	typ.	8,8	MHz
Output voltage (peak-to-peak value; see note)	$V_{2-11(p-p)}$	typ.	4	V

Note

The gain of the amplifier is determined by the feedback network comprising the impedances between pins 2 and 3, and pins 8 and 3. The values quoted apply to the circuit on page 7 (Fig. 1).

PINNING

1. Current setting demodulator
2. Video amplifier output
3. Video amplifier input
4. F.M. signal input
5. F.M. signal input
6. Positive supply
7. Switch input
8. Switch output
9. Switch input
10. Switch actuating input
11. Negative supply (ground)
12. Limiter output
13. Limiter output
14. Demodulator input
15. Demodulator input
16. Demodulator output

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Current setting of demodulator

   The current into this pin directly determines the amplitude and the d.c. level of the demodulator output. At I_1 = 4 mA, optimum temperature compensation is obtained.

2. Video amplifier output

   A signal up to 4 V peak-to-peak is available from this output (Fig. 1).
   This can be the video signal (Fig. 1) or the f.m. signal to the delay line (drop-out elimination; Fig. 2).

3. Video amplifier input

   The demodulator output signal is the input signal to this pin (Fig. 1) or the f.m. modulated signal (Fig. 2).

4. F.M. signal input (in conjunction with pin 5)

   A frequency modulated signal of 1 V peak-to-peak is applied between pins 4 and 5. D.C. feedback from the limiter output is applied to stabilize the operation.

5. F.M. signal input

   See pin 4.

APPLICATION INFORMATION (continued)

6. Positive supply

   Correct operation can be obtained in the range 11 to 13 V.

7. Switch input

   The signal applied to pin 7 or to pin 9 is transferred to pin 8, depending on the switch position. For an input level between 0 and 2,7 V at pin 10, the signal at pin 7 is transferred to pin 8, and when between 3,7 and 6 V the input signal at pin 9 is transferred to pin 8.
   The signal at pin 7 or pin 9 may vary from 6,5 to 12 V.
   The signal at pin 8 is 1,5 V below the value at pin 7 or 9.
   The difference in input level at pins 7 and 9, to obtain equal output at pin 8, will be less than 20 mV.

8. Switch output

   See pin 7.

9. Switch input

   See pin 7.

10. Switch actuating input

    See pin 7.

11. Negative supply (ground)

12. Limiter output

    A balanced signal is available between pins 12 and 13. The signal amplitude is limited to 750 mV at both outputs.

13. Limiter output

    See pin 12.

14. Demodulator input

    A phase shifted signal (with respect to the internally applied signal) is applied between pins 14 and 15.

15. Demodulator input

    See pin 14.

16. Demodulator output

    The output signal is proportional to :
    - current into pin 1
    - slope of the phase characteristic of the network between pins 12 and 13, and pins 14 and 15
    - impedance level at the output
    - the sweep (Δf) of the f.m. signal.

    A signal of typically 540 mV is available at this pin when using the component values in Fig. 1 and Δf = 1,4 MHz.

APPLICATION INFORMATION (continued)

Test circuit

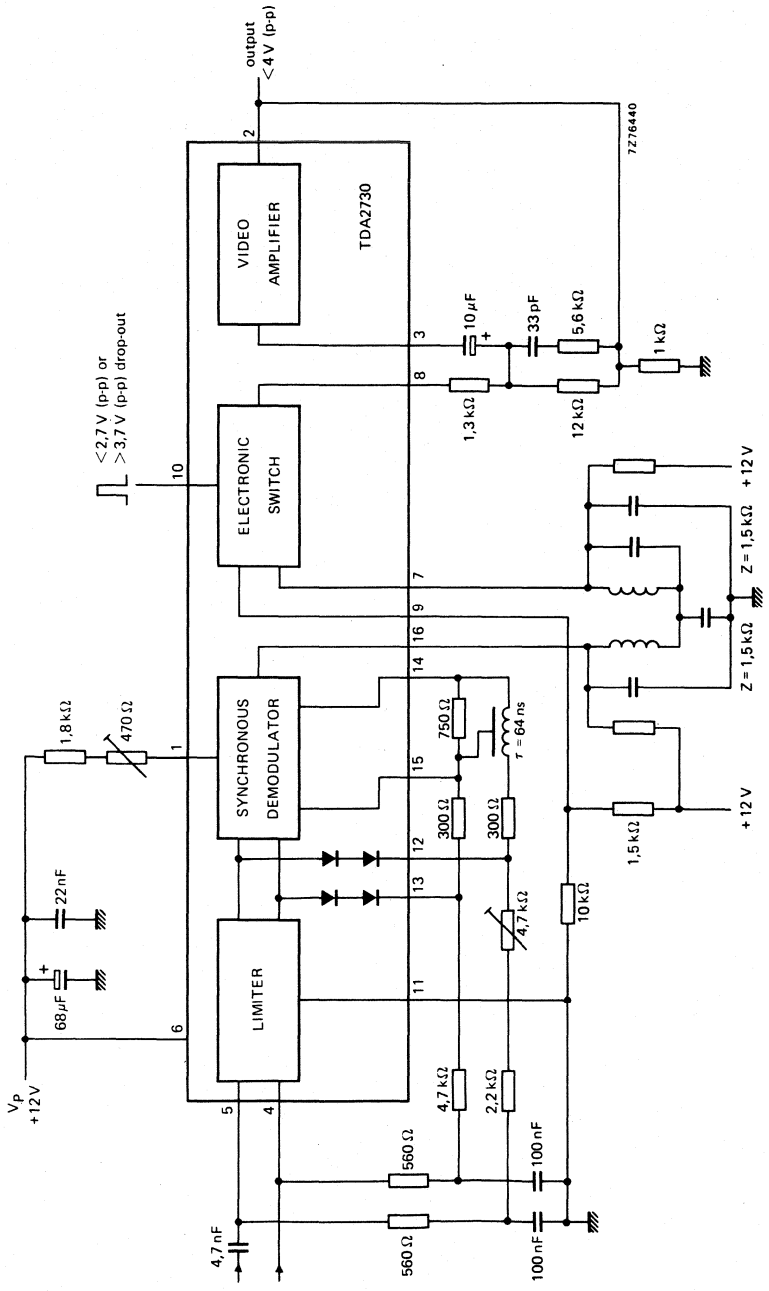


Fig. 1

APPLICATION INFORMATION (continued)

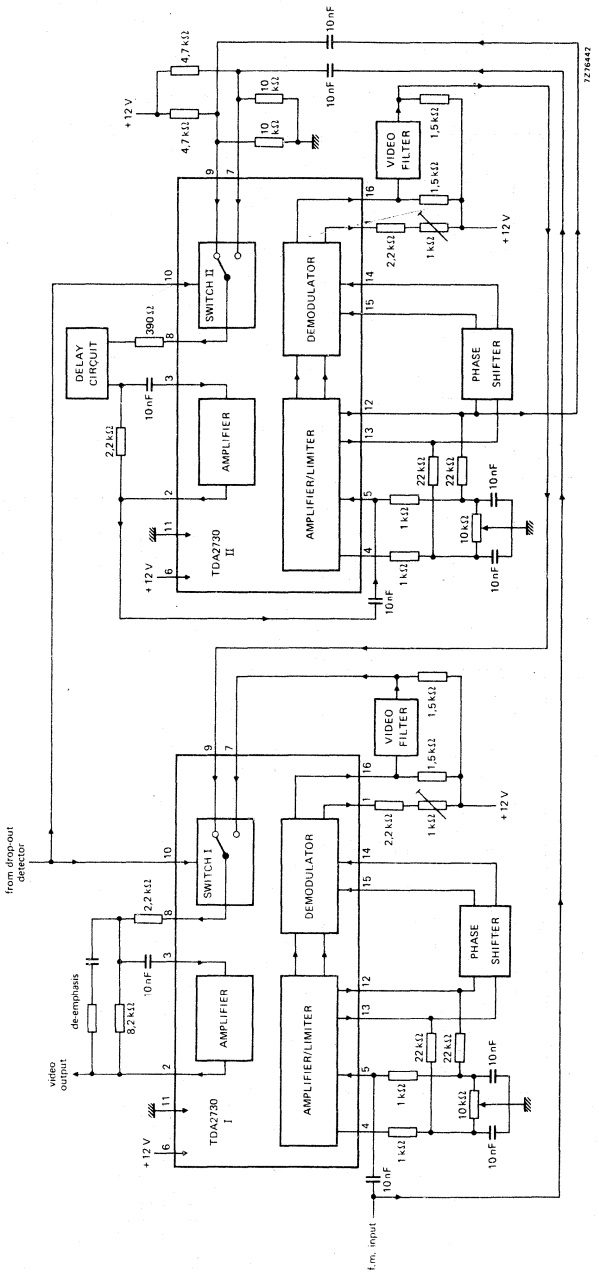


Fig. 2. Drop-out eliminator.

TELEVISION SOUND COMBINATION

The TDA2790 contains the following functions:

- Limiter/amplifier.
- F.M. detector.
- Physiological d.c. volume control.
- D.C. tone control.

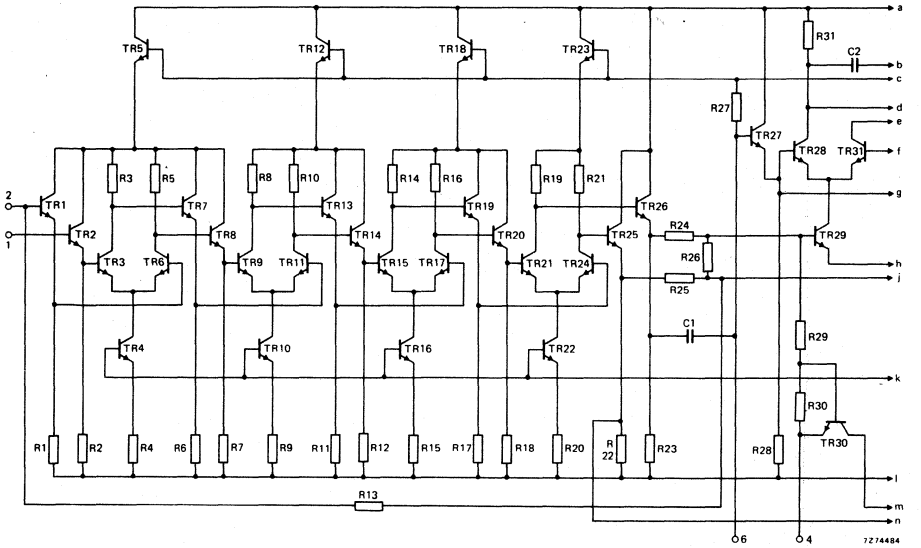
The limiter/amplifier is designed as a four-stage differential amplifier, to obtain good noise and interference suppression.
The detector is a balanced quadrature demodulator.
The demodulator output impedance is low during normal operation.
The limiter/amplifier and demodulator can be switched-off via pin 4; in that condition the output impedance becomes high (10 kΩ).
This switching action occurs without a d.c. shift, so that no transients will be noticed in the speaker.
Due to this switching action audio signals (e.g. from a VCR) can be inserted before the tone and volume control circuits.
The circuit is very flexible in its application because the characteristics of the various controls can be adapted by changing external component values.

QUICK REFERENCE DATA

Supply voltage	V_{13-3}	typ.	12	V
Total current drain, normal operation	I_{13}	typ.	50	mA
Total current drain, VCR operation	I_{13}	typ.	53	mA
Frequency	f_o		5,5	MHz
Input voltage at start of limiting	$V_{i(rms)}$	typ.	100	μV
A.M. rejection at V_i = 1 mV	α	typ.	45	dB
A.F. output voltage at $\Delta f = \pm 15$ kHz (at pin 7 after de-emphasis)	$V_{o(rms)}$	typ.	100	mV
D.C. bass control range		<	$^{+16}_{-19}$	dB
D.C. treble control range		<	$^{+12}_{-15}$	dB
D.C. volume control range		>	−75	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).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TR12
TR18
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R31
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R16
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R21
TR1
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TR29
C1
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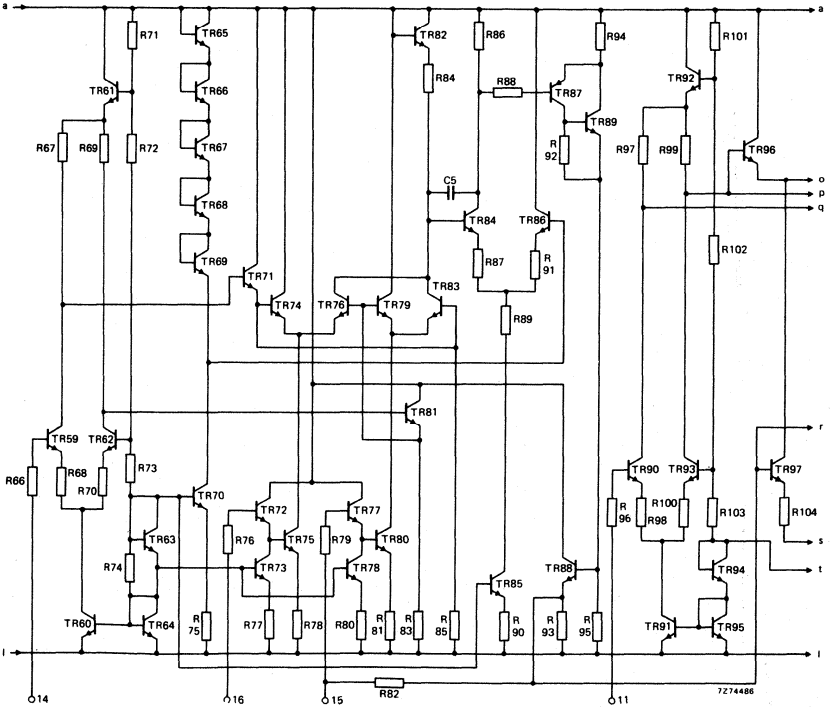
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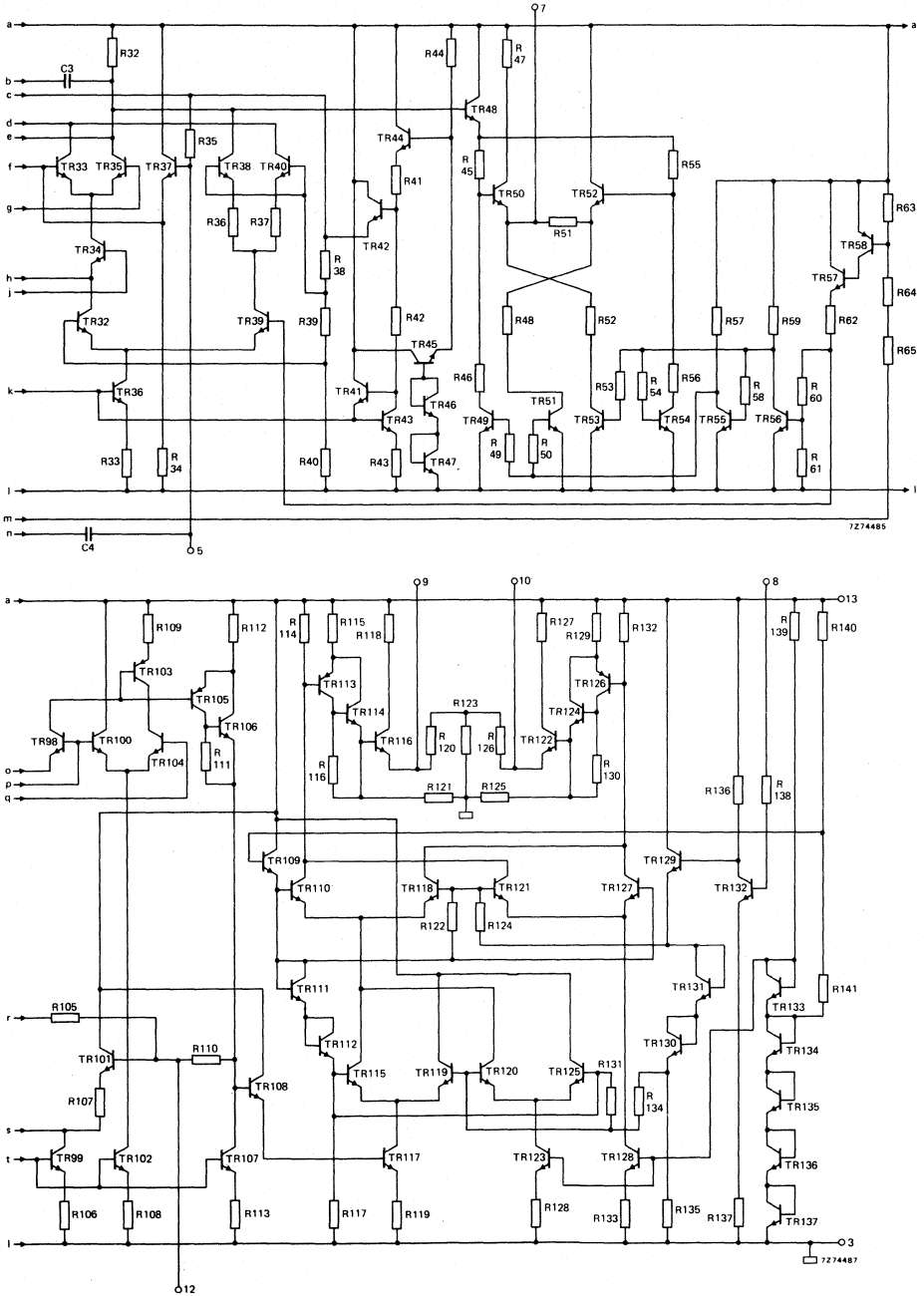
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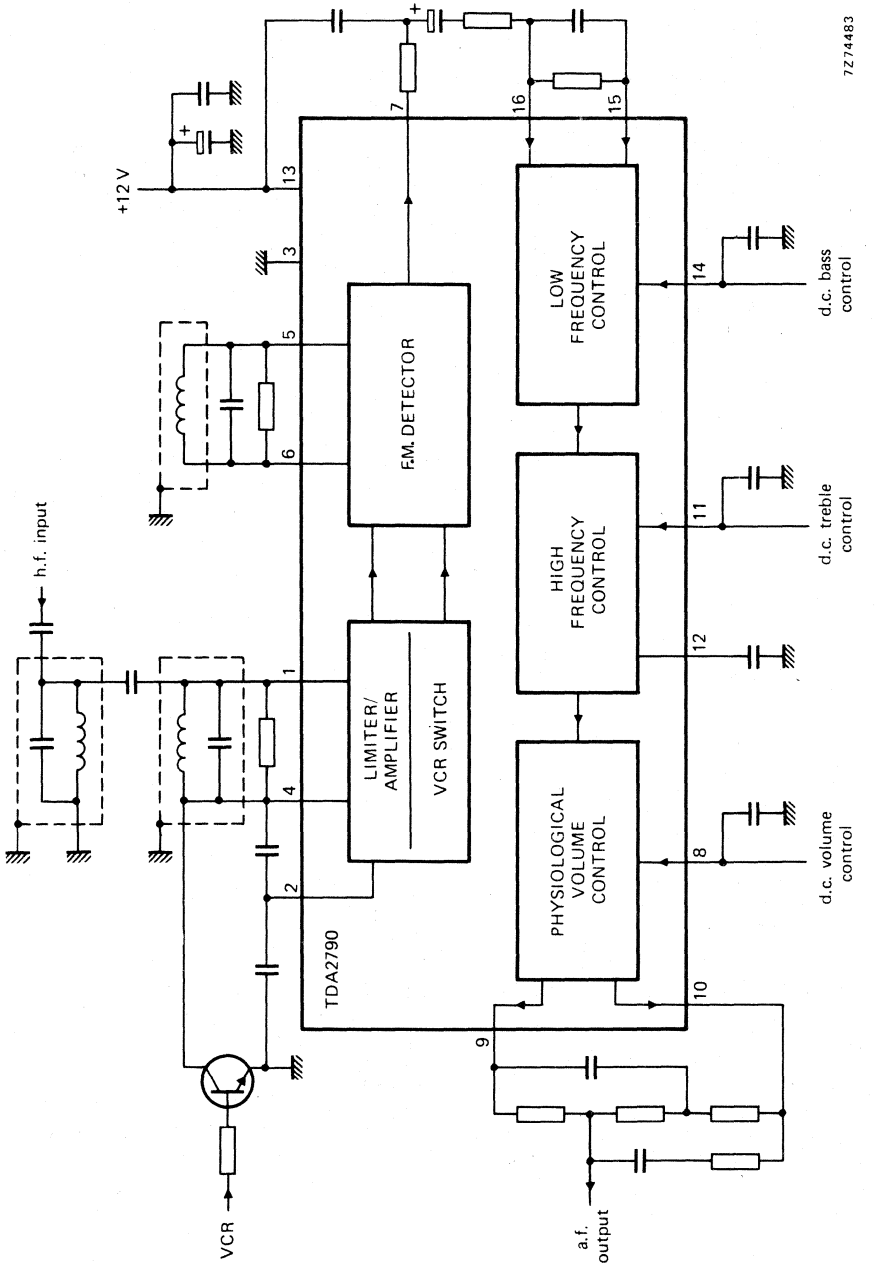
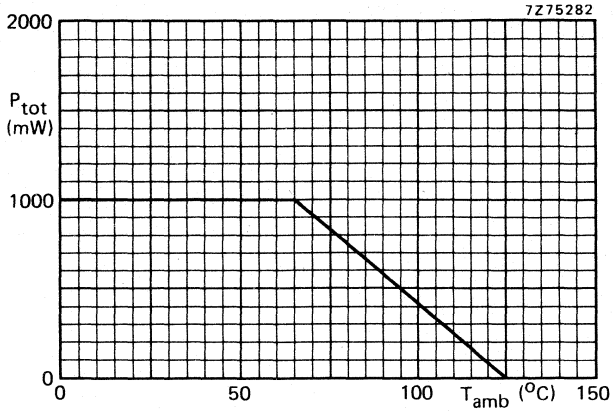
BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{13-3}	max.	14 V
Power dissipation			



Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +65	°C

CHARACTERISTICS

Measured in circuit on page 10, at T_{amb} = 25 °C; V_{13-3} = 12 V; f = 5,5 MHz (unless otherwise specified)

Supply voltage range	V_{13-3}		10,8 to 14	V
Total current drain, normal operation	I_{13}		37 to 64	mA
Total current drain, VCR operation	I_{13}		39 to 68	mA
Limiter/amplifier/demodulator (note 1)				
Input limiting voltage at V_{7-3} = −3 dB (r.m.s. value)	$V_{i(rms)}$	typ.	100	μV
Input impedance	$\lvert Z_{1-3} \rvert$	typ.	200	kΩ
A.M. rejection				
V_i = 0,5 mV (note 2)	α	typ.	45	dB
V_i = 1 mV (note 2)	α	typ.	45	dB
V_i = 10 mV (note 2)	α	typ.	50	dB
V_i = 100 mV (note 2)	α	typ.	55	dB
A.F. output voltage at f_m = 1 kHz; Δf = ±15 kHz; V_i = 10 mV; Q_{L3} = 25; pin 7	$V_{o(rms)}$	typ.	100	mV
Total harmonic distortion at pin 7 f_m = 1 kHz; Δf = ±40 kHz; V_i = 10 mV	d_{tot}	typ.	1,6	%
Zero-point stability at 30 μV to 10 mV; pin 7		typ.	2	kHz

Notes

1. At all measurements, the demodulator is controlled at minimum distortion.
2. See test set-up on page 7.

CHARACTERISTICS (continued)

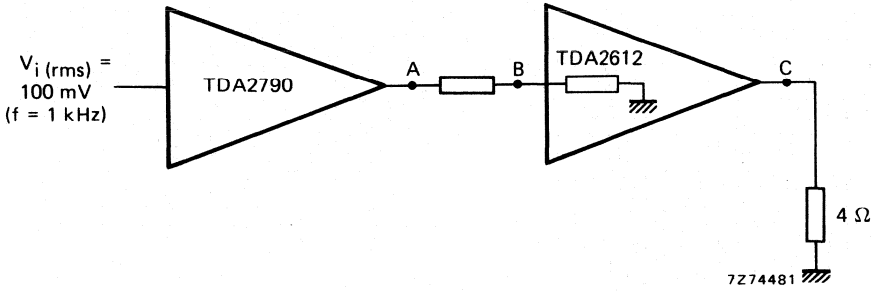
Signal-to-noise ratio at pin 7 f_m = 1 kHz; Δf = ±15 kHz; V_i = 10 mV (note 1)	S/N	typ. 70	dB
Demodulator output impedance, normal operation	$\lvert Z_{7-3} \rvert$	typ. 100	Ω
Demodulator output impedance, VCR operation	$\lvert Z_{7-3} \rvert$	typ. 10	kΩ
D.C. shift at demodulator output, when demodulator is switched to VCR condition	ΔV_{7-3}	typ. 50	mV
A.F. amplifier			
Bass control	see graph on page 8		
Input impedance	$\lvert Z_{14-3} \rvert$	typ. 500	kΩ
Treble control	see graph on page 8		
Input impedance	$\lvert Z_{11-3} \rvert$	typ. 500	kΩ
Control voltages for linear frequency characteristic	V_{11-3} V_{14-3}	typ. 2,9 typ. 3,1	V V
Volume control	see graph on page 8		
Input impedance	$\lvert Z_{8-3} \rvert$	typ. 200	kΩ
Bass and treble compensation	see graph on page 9		
Voltage gain (pin 16 to output) f = 1 kHz; V_{11-3} = 2,9 V; V_{14-3} = 3,1 V; V_{8-3} = 4 V	G_v	typ. 8	dB
D.C. volume control range		> −75	dB
Unweighted signal-to-noise ratio at an output voltage of 10,7 mV; V_i = 100 mV (note 2)	S/N	typ. 52	dB
Total harmonic distortion at output f = 1 kHz; V_{16-3} = 100 mV (related to max output; note 3) in the range: 0 to −20 dB −20 to −40 dB −40 to −60 dB	 d_{tot} d_{tot} d_{tot}	 typ. 0,2 typ. 0,5 typ. 0,7	 % % %

Notes

1. Unweighted signal-to-noise ratio, measured for a frequency range between 31,5 Hz and 20 kHz.
2. See test condition on page 7.
3. Measured at flat tone control characteristics.

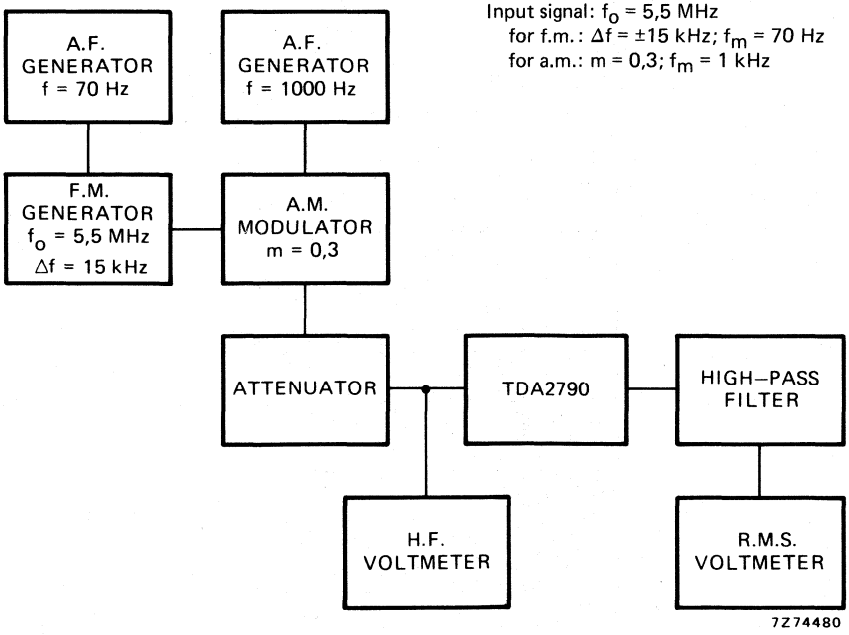
Test condition for S/N ratio

In combination with the TDA2612 (input impedance 36 kΩ), this output voltage corresponds to an audio output power of 100 mW (at 1 kHz) in accordance with DIN45 500. This figures are measured for a frequency range between 31,5 Hz and 20 kHz (unweighted).

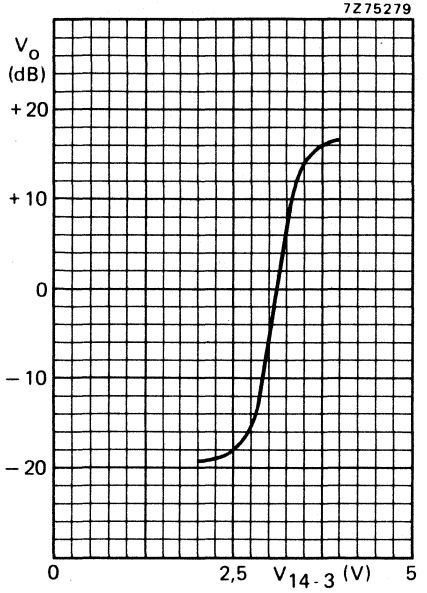


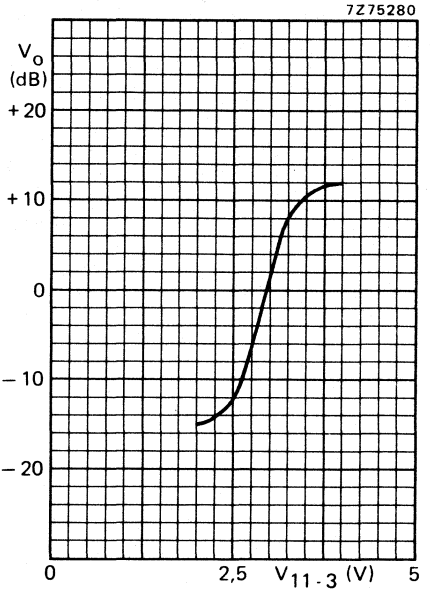
A		B	C	S/N ratio A
107 mV	max −7,5 dB	90 mV	10 W	–
10,7 mV	max −27,5 dB	9 mV	0,1 W	52 dB

TEST SET-UP

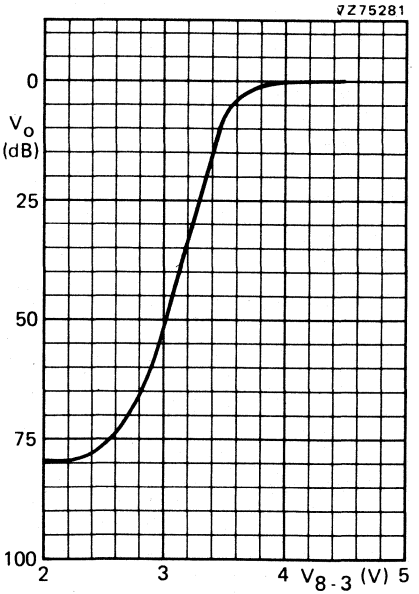


Input signal: f_o = 5,5 MHz
for f.m.: Δf = ±15 kHz; f_m = 70 Hz
for a.m.: m = 0,3; f_m = 1 kHz

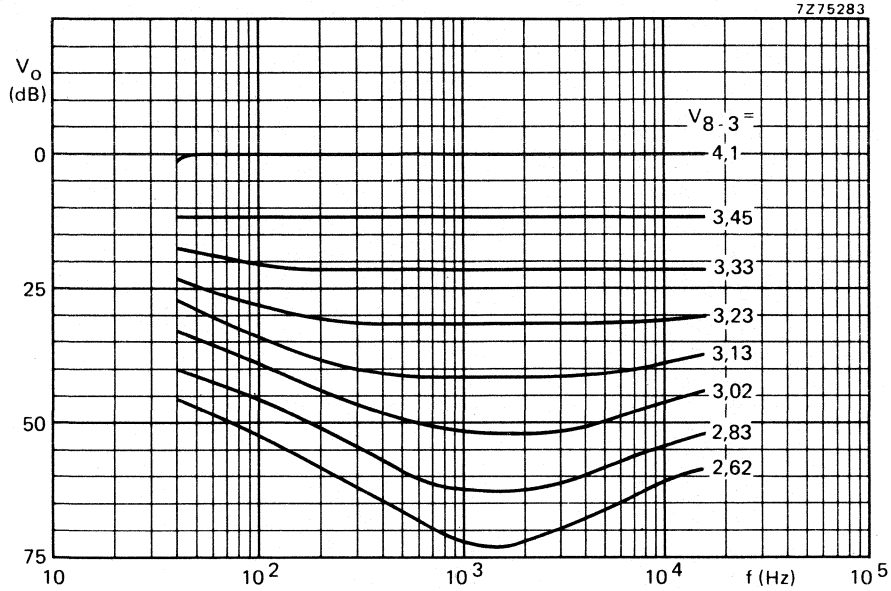




Bass control curve at f = 40 Hz; $V_{i(rms)}$ = 100 mV. Treble control curve at f = 15 kHz; $V_{i(rms)}$ = 100 mV.



Volume control curve at f = 1 kHz.



Bass and treble compensation measured at flat tone characteristic.

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Limiter input.
2. The decoupling capacitor for the internal limiter feedback is connected to this pin.
3. Negative supply (ground).
4. a. Limiter output for external feedback to pin 1.
   b. The demodulator will switch to VCR condition when pin 4 is grounded.

5 and 6. External tank circuit (demodulator reference signal).

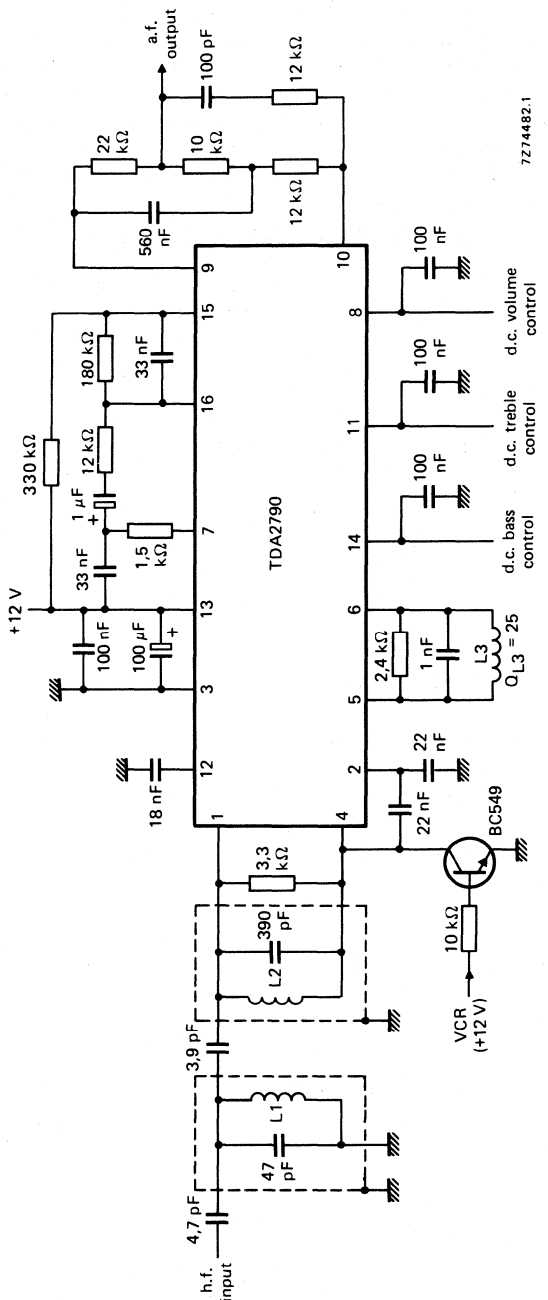
7. Demodulator output.
8. D.C. volume control.

9 and 10. External circuit for physiological volume control.

11. D.C. treble control.
12. External capacitor for treble control.
13. Positive supply.
14. D.C. bass control.

15 and 16. External circuit for bass control.

APPLICATION INFORMATION (continued)



TELEVISION SOUND COMBINATION

The TDA2791 contains the following functions:

- Limiter/amplifier
- F.M. detector.
- Physiological d.c. volume control.
- D.C. tone control.

The limiter/amplifier is designed as a four-stage differential amplifier, to obtain good noise and interference suppression. The detector is a balanced quadrature demodulator.

During VTR operation audio signals can be inserted before the tone and volume control circuits. The limiter amplifier and demodulator must be switched off by grounding pin 2. This switching action occurs without a d.c. shift, so that no transients will be noticed in the speaker. The circuit is very flexible in its application because the characteristics of the various controls can be adapted by changing external component values.

QUICK REFERENCE DATA

Supply voltage	V_{13-3}	typ.	12 V
Total current drain	I_{13}	typ.	61 mA
Frequency	f_o		5,5 MHz
Input voltage at start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	100 μV
A.M. rejection at V_i = 5 mV	α	typ.	60 dB
A.F. output voltage at $\Delta f = \pm 27$ kHz (r.m.s. value) (at pin 7 after de-emphasis)	$V_{o(rms)}$	typ.	700 mV
D.C. bass control range		$<$	$^{+16}_{-19}$ dB
D.C. treble control range		$<$	$^{+12}_{-15}$ dB
D.C. volume control range		$>$	−75 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

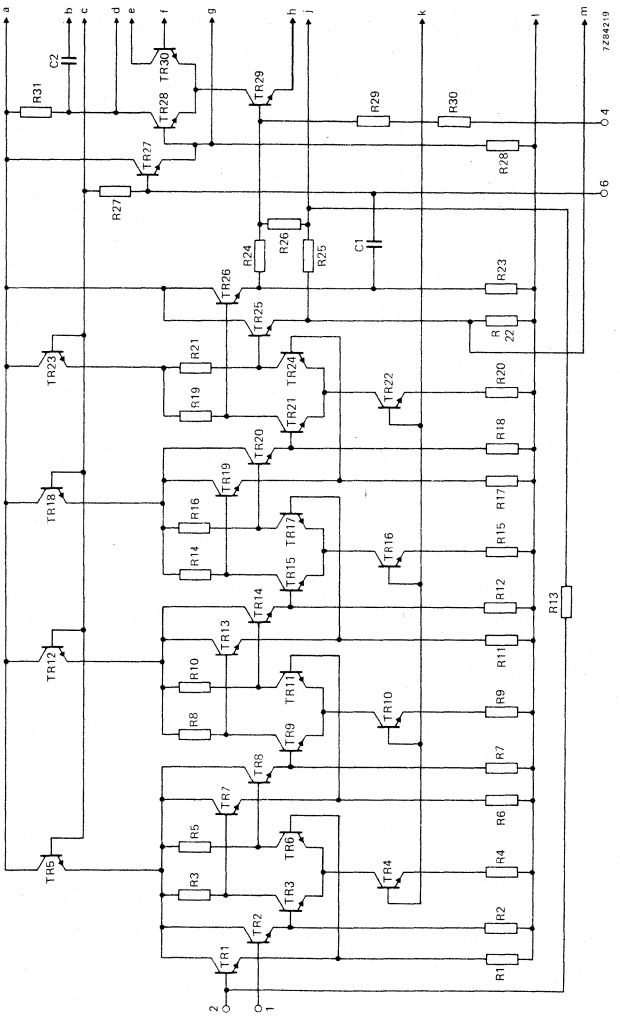


Fig. 1a Circuit diagram; continued in Fig. 1b.

DEVELOPMENT SAMPLE DATA

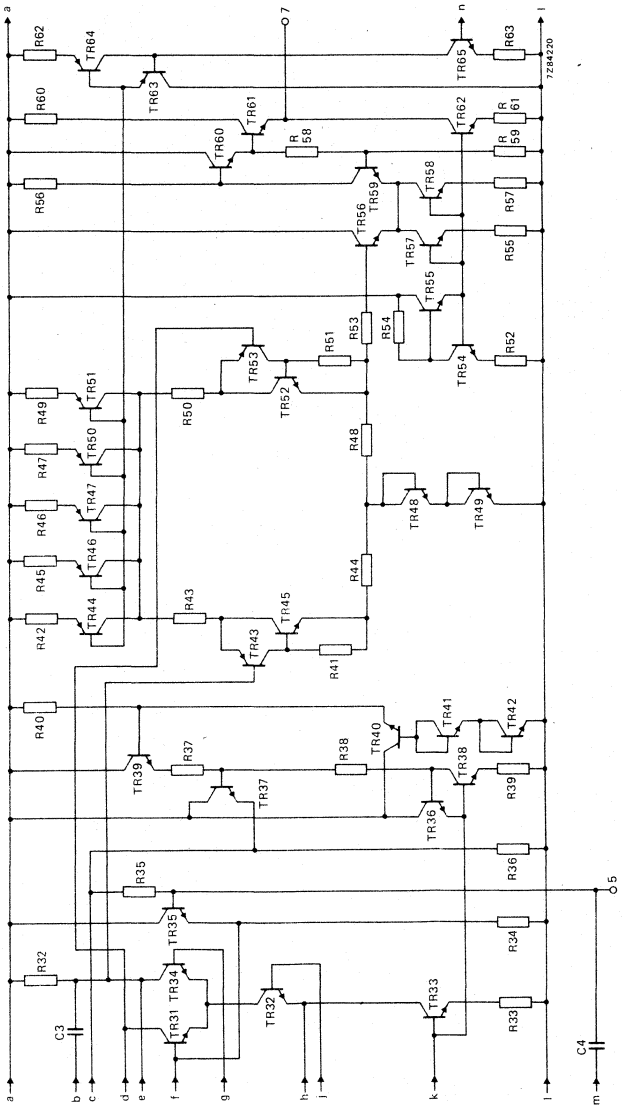


Fig. 1b Circuit diagram; continued from Fig. 1a; continued in Fig. 1c, for line 'n' see Fig. 1d.

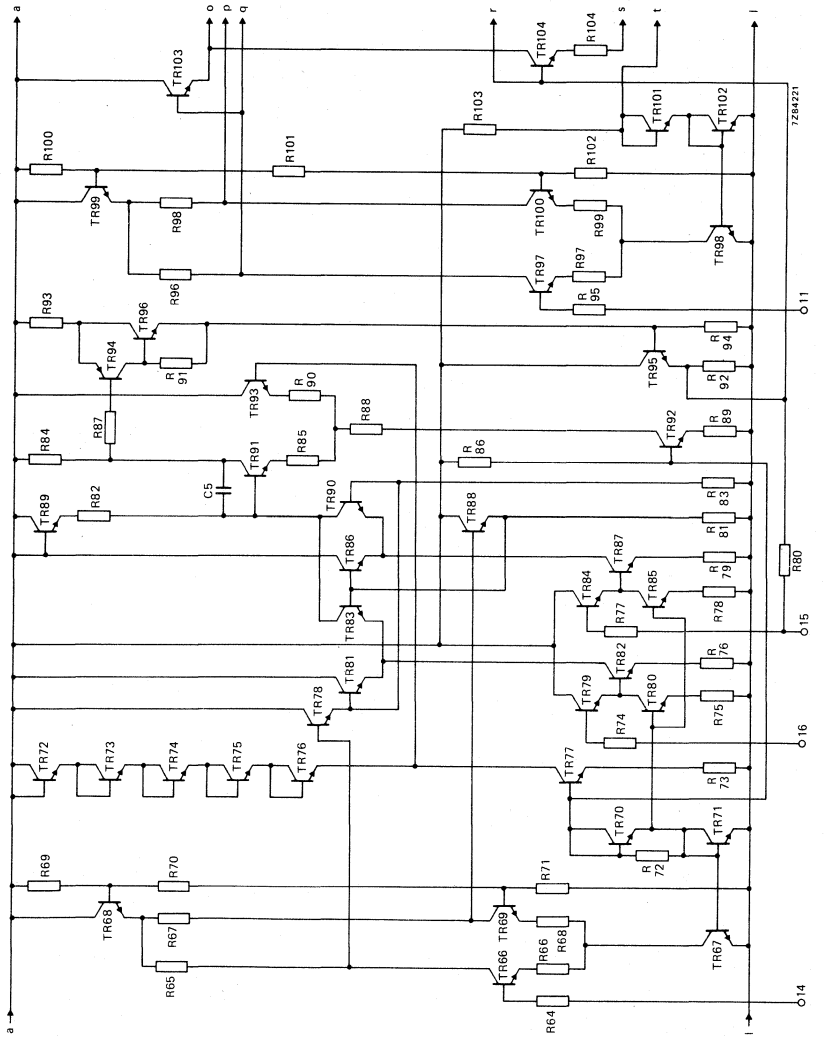


Fig. 1c Circuit diagram; continued from Fig. 1b; continued in Fig. 1d.

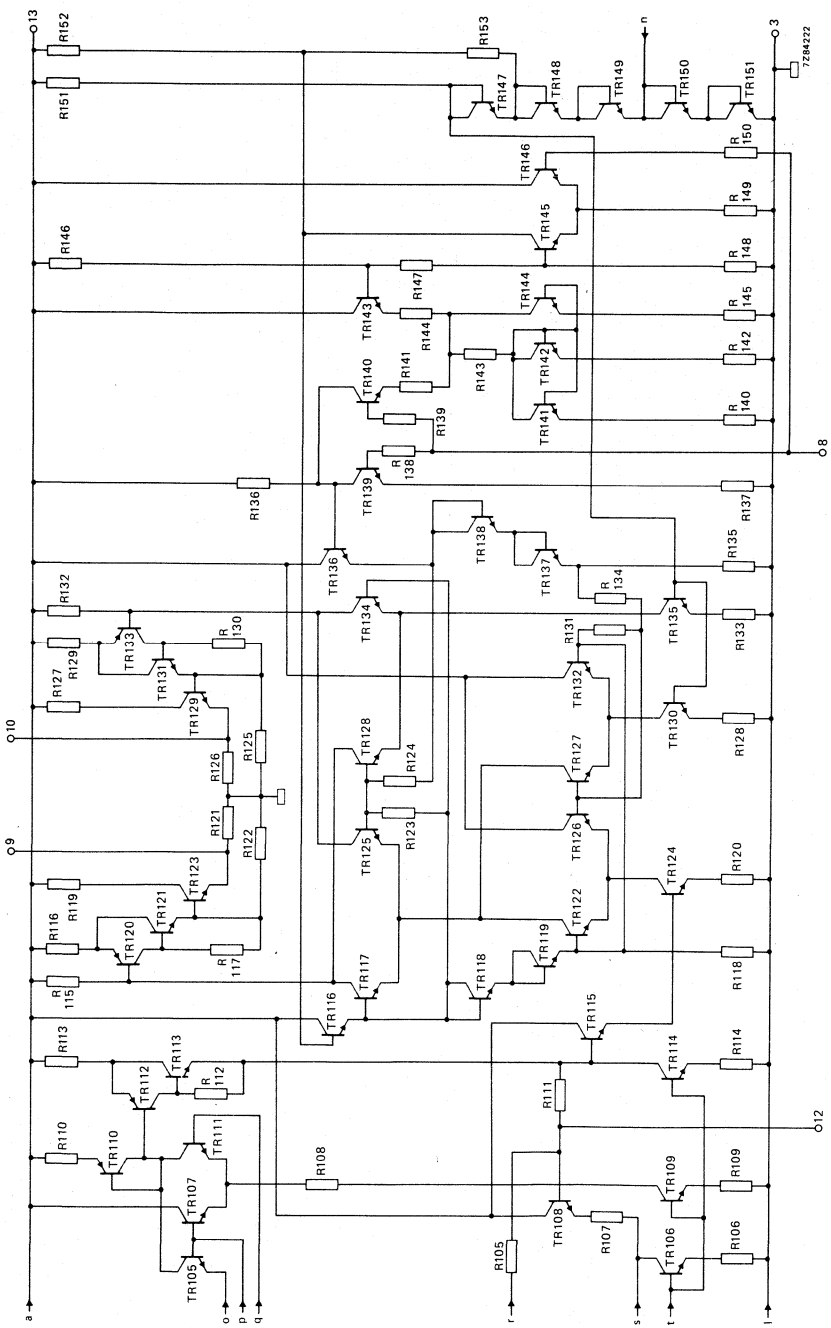


Fig. 1d Circuit diagram; continued from Fig. 1c and Fig. 1b.

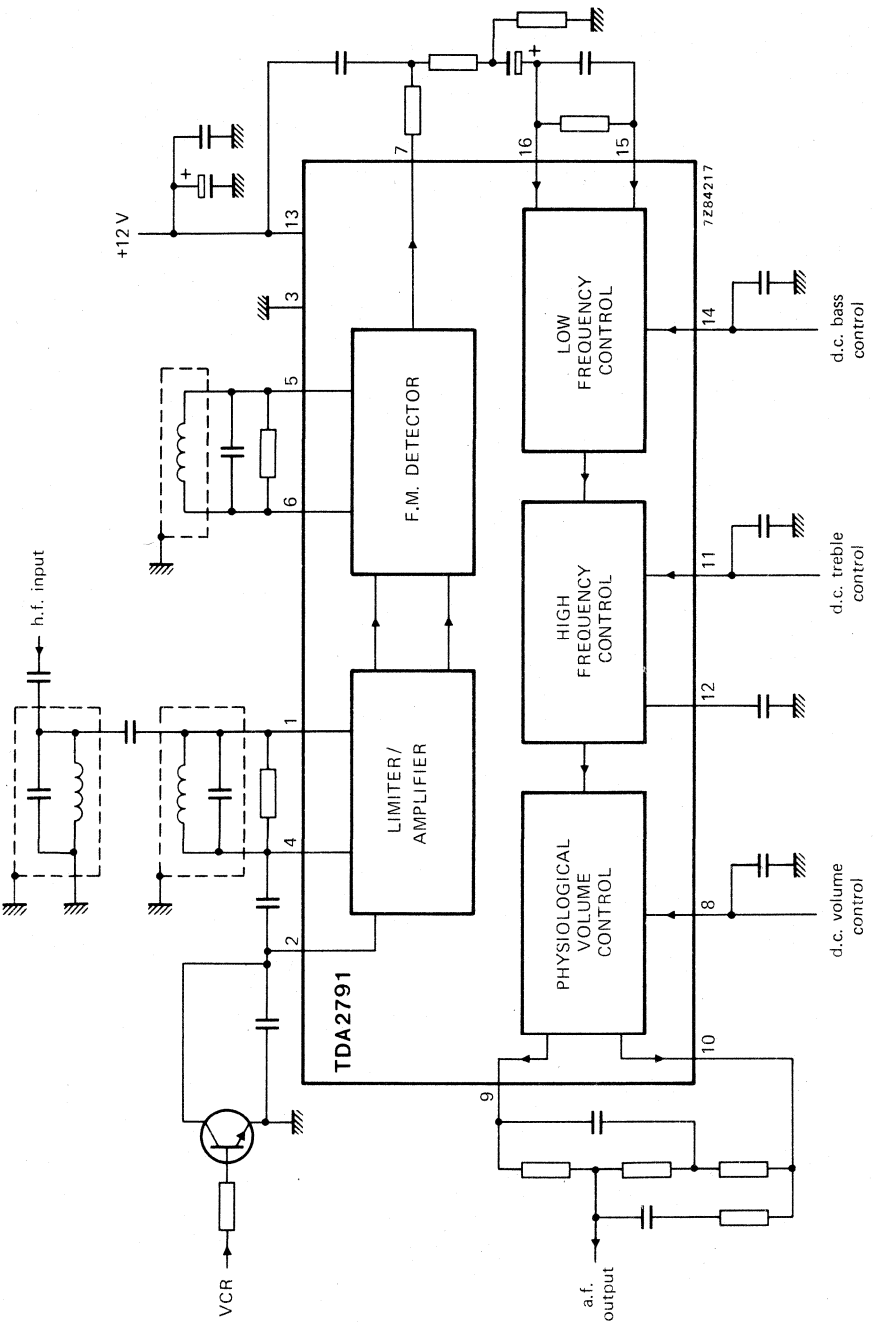


Fig. 2 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{13-3}	max.	13,2 V

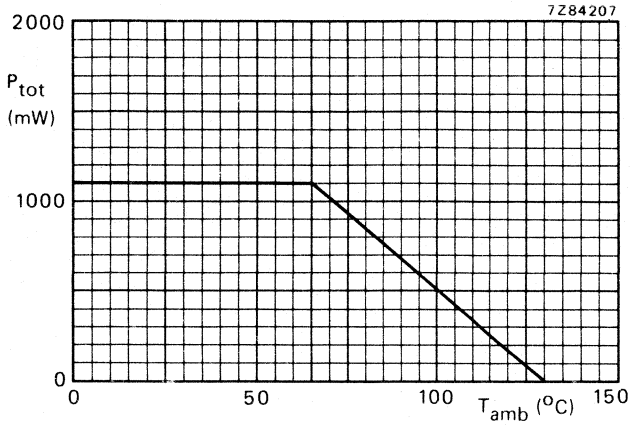


Fig. 3 Power derating curve.

Storage temperature	T_{stg}	−25 to + 130 °C
Operating ambient temperature	T_{amb}	−25 to + 65 °C

CHARACTERISTICS

Measured in Fig. 9 at T_{amb} = 25 °C; V_{13-3} = 12 V; f = 5,5 MHz (unless otherwise specified)

Supply voltage range	V_{13-3}		10,8 to 13,2 V
Total current drain	I_{13}		43 to 79 mA
Limiter/amplifier/demodulator (note 1)			
Input limiting voltage at V_{7-3} = −3 dB (r.m.s. value)	$V_{i(rms)}$	typ.	100 μV
Input impedance	$\lvert Z_{1-3} \rvert$	typ.	200 kΩ
A.M. rejection			
V_i = 0,5 mV }	α	typ.	50 dB
V_i = 1 mV } note 2	α	typ.	50 dB
V_i = 5 mV } note 2	α	typ.	60 dB
V_i = 50 mV } note 2	α	typ.	55 dB
A.F. output voltage at pin 7 (r.m.s. value)			
f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV; Q_{L3} = 12,5	$V_{o(rms)}$	typ.	700 mV

Notes

1. The quadrature reference circuit must be tuned in such a way that there is no difference in the demodulator d.c. output voltage when the limiter input is switched from signal to no signal.
2. See test set-up Fig. 4.

CHARACTERISTICS (continued)

Total harmonic distortion at pin 7			
f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV	d_{tot}	typ.	0,35 %
Zero-point stability at 30 μV to 10 mV; pin 7		typ.	2 kHz
Hum suppression; pin 7		typ.	20 dB
Signal-to-noise ratio at pin 7			
f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV (note 1)	S/N	typ.	63 dB
Demodulator output impedance	$\lvert Z_{7\text{-}3} \rvert$	typ.	25 Ω
A.F. amplifier			
Input voltage bass control circuit at pin 16 (r.m.s. value)			
at Δf = ± 27 kHz	$V_{i(rms)}$	typ.	215 mV
Bass control	see graph, Fig. 5		
Input impedance	$\lvert Z_{14\text{-}3} \rvert$	typ.	500 kΩ
Treble control	see graph, Fig. 6		
Input impedance	$\lvert Z_{11\text{-}3} \rvert$	typ.	500 kΩ
Control voltages for flat frequency characteristic	$V_{11\text{-}3}$	typ.	3,2 V
	$V_{14\text{-}3}$	typ.	3,2 V
Volume control	see graph, Fig. 7		
Input current at $V_{8\text{-}3}$ = 4 V	I_8	typ.	40 μA
Physiological volume control (bass and treble compensation)	see graph, Fig. 8		
Voltage gain of audio part			
f = 1 kHz; $V_{11\text{-}3}$ = 3,2 V; $V_{14\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V	G_v	typ.	4 dB
D.C. volume control range		>	−75 dB
Weighted signal-to-noise ratio			
$V_{i(rms)}$ = 215 mV; −24 dB volume control (notes 1 and 2)		typ.	56 dB
Total harmonic distortion at output			
f = 1 kHz; $V_{i(rms)}$ = 215 mV			
(related to max. output; note 2) at:			
0 dB	d_{tot}	typ.	0,2 %
−20 dB	d_{tot}	typ.	0,4 %

Notes
1. Specified according to DIN 45405; weighted noise (peak value).
2. Measured at flat-tone control characteristics.

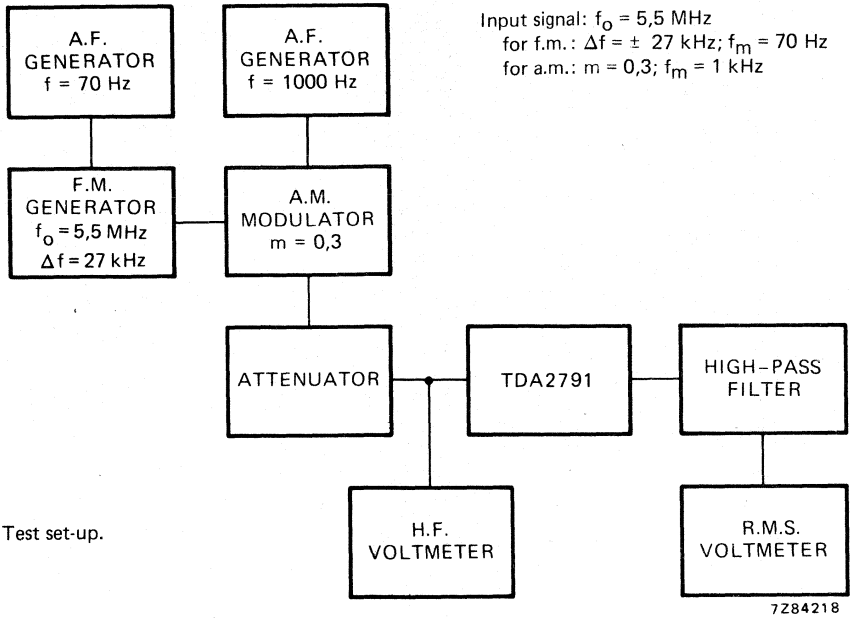


Fig. 4 Test set-up.

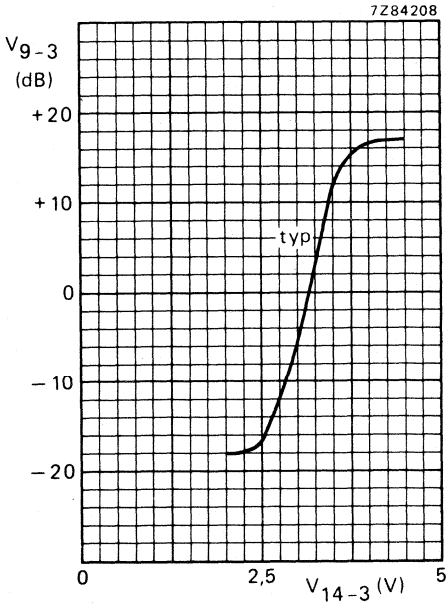


Fig. 5 Bass control curve; f = 40 Hz; V_{11-3} = 3,2 V; V_{8-3} = 4 V.

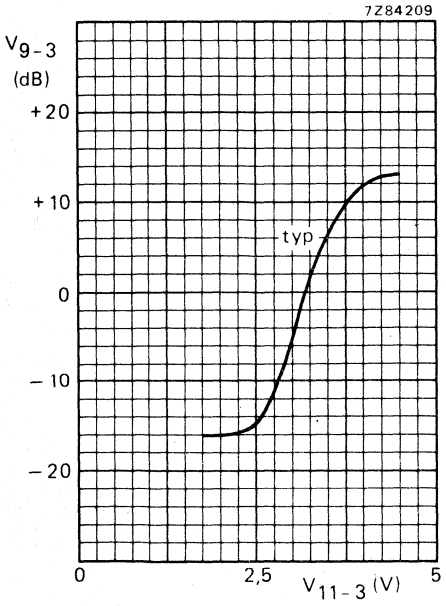


Fig. 6 Treble control curve; f = 15 kHz; V_{14-3} = 3,2 V; V_{8-3} = 4 V.

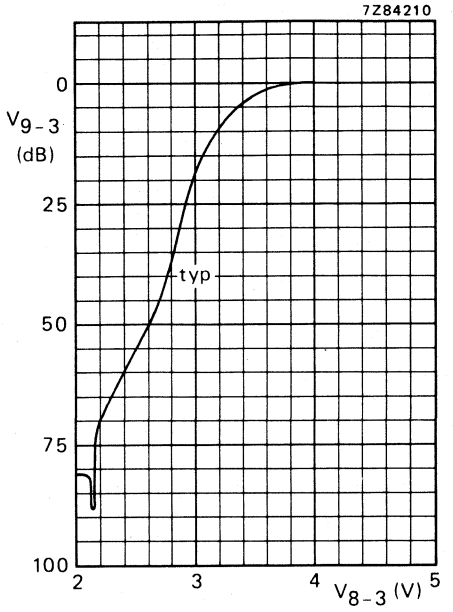


Fig. 7 Volume control curve; f = 1 kHz.
V_{14-3} = 3,2 V; V_{11-3} = 3,2 V.

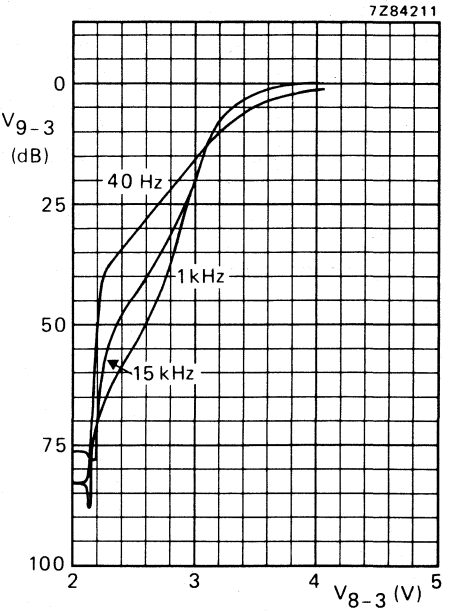


Fig. 8 Physiological volume control curves (typical values); V_{14-3} = 3,2 V; V_{11-3} = 3,2 V.

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Limiter input.
2. The decoupling capacitor for the internal limiter feedback is connected to this pin.
3. Negative supply (ground).
4. Limiter output for external feedback to pin 1.

5 and 6. External tank circuit (demodulator reference signal).

7. Demodulator output.
8. D.C. volume control.

9 and 10. External circuit for physiological volume control.

11. D.C. treble control.
12. External capacitor for treble control.
13. Positive supply.
14. D.C. bass control.

15 and 16. External circuit for bass control.

DEVELOPMENT SAMPLE DATA

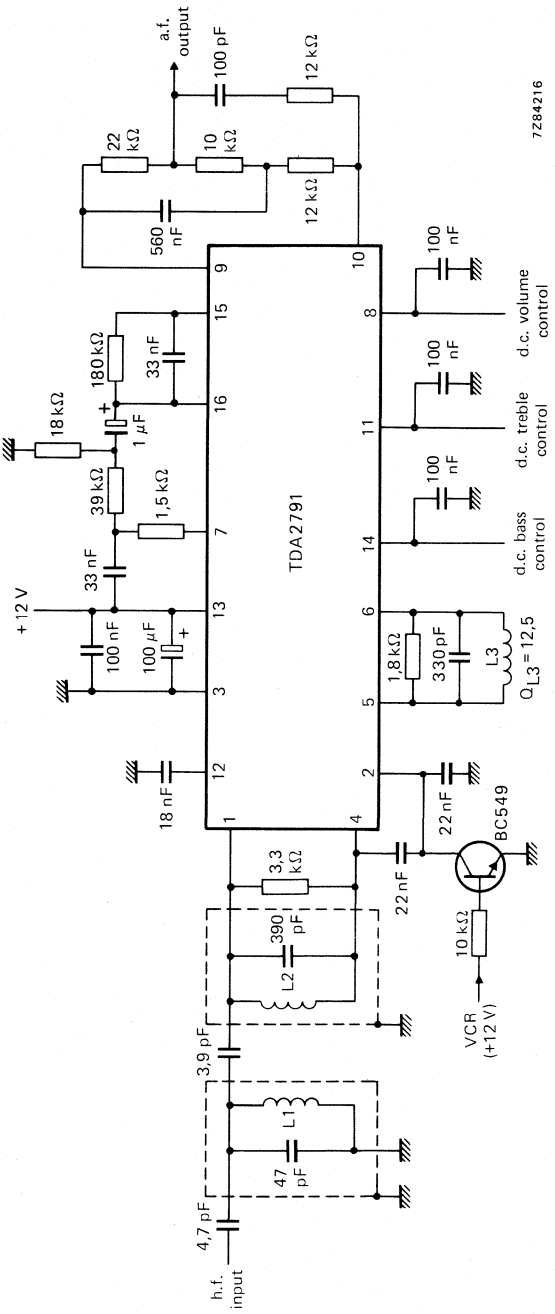


Fig. 9 Application circuit diagram.

VIDEO CONTROL COMBINATION

The TDA3500 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).
The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from an external source.
RGB signals are provided at the output to drive the video output stages.
The TDA3500 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 3 d.c. gain controls for the RGB output signals (white point adjustment)

QUICK REFERENCE DATA

Supply voltage	$V_{6\text{-}24}$	typ.	12 V
Supply current	I_6	typ.	100 mA
Luminance input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45 V
Luminance input resistance	$R_{15\text{-}24}$	typ.	12 kΩ
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18\text{-}24(p\text{-}p)}$	typ.	1,33 V
−(R-Y)	$V_{17\text{-}24(p\text{-}p)}$	typ.	1,05 V
Inserted RGB signals (peak-to-peak values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	typ.	1 V
Three-level sandcastle pulse detector	$V_{10\text{-}24}$	typ.	2,5/4,5/8,0 V
Control voltage ranges			
brightness	$V_{20\text{-}24}$		1 to 3 V
contrast	$V_{19\text{-}24}$		2 to 4 V
saturation	$V_{16\text{-}24}$		2,1 to 4 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

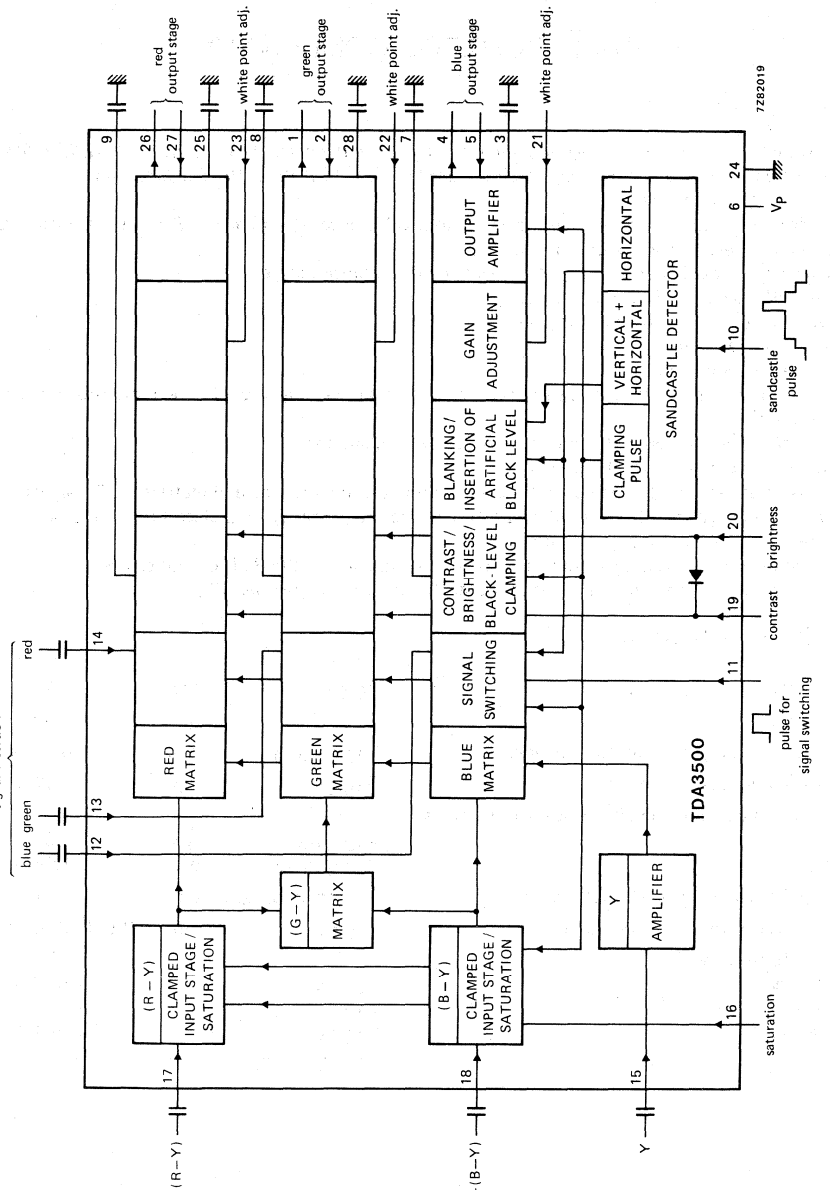


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	max.	
Supply voltage	$V_P = V_{6-24}$		–	13,2	V
Voltages with respect to pin 24					
pins 1,4,26	$V_{1,4,26-24}$		½V_P	V_P + 1	V
pins 2,5,27	$V_{2,5,27-24}$		0	V_P	V
pin 10	V_{10-24}		0	V_P	V
pin 11	V_{11-24}		–0,5	3	V
pins 16,19,20	$V_{16,19,20-24}$		0	½V_P	V
pins 21,22,23	$V_{21,22,23-24}$		0	V_P	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage				
Current at pin 20	I_{20}	max.		5	mA
Total power dissipation	P_{tot}	max.		1,7	W
Storage temperature	T_{stg}			–25 to + 125	°C
Operating ambient temperature	T_{amb}			–20 to + 70	°C

CHARACTERISTICS

Supply voltage range	V_P		10,8 to 13,2	V
The following characteristics are measured in Fig. 2; V_P = 12 V; T_{amb} = 25 °C; $V_{18-24(p-p)}$ = 1,33 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{12,13,14-24(p-p)}$ = 1 V; unless otherwise specified				
Current consumption	I_6	typ.	100	mA
Colour difference inputs				
–(B-Y) input signal (peak-to-peak value)*	$V_{18-24(p-p)}$		1,33	V
–(R-Y) input signal (peak-to-peak value)*	$V_{17-24(p-p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control				
control voltage range for a change of saturation from –20 dB to + 6 dB	V_{16-24}		2,1 to 4	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3	V
input current	I_{16}	<	20	μA

* For saturated colour bar with 75% of maximum amplitude.

CHARACTERISTICS (continued)

(G-Y) matrix

Matrixed according the equation	$V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$		

Luminance amplifier

Input signal (peak-to-peak)	$V_{15\text{-}24(p\text{-}p)}$		0,45 V
Input resistance	$R_{15\text{-}24}$	typ.	12 kΩ
Internal d.c. voltage	$V_{15\text{-}24}$	typ.	2,7 V

RGB channels

Signal switching input voltage for insertion			
on level	$V_{11\text{-}24}$		0,9 to 1,5 V
off level	$V_{11\text{-}24}$		−0,5 to 0,3 V
Input current	I_{11}		−100 to + 200 μA
Signal insertion			
external RGB input signal (peak-to-peak value)*	$V_{12,13,14\text{-}24(p\text{-}p)}$		1 V
internal d.c. voltage due to clamping	$V_{12,13,14\text{-}24}$	typ.	3,5 V
input current	$I_{12,13,14}$	<	5 μA
Contrast control			
control voltage range for a change of contrast from −17 dB to + 3 dB	$V_{19\text{-}24}$		2 to 4 V
nominal contrast (3 dB below max.)	$V_{19\text{-}24}$	typ.	3,4 V
control voltage for −6 dB	$V_{19\text{-}24}$	typ.	2,7 V
input current	I_{19}	<	10 μA
Brightness control			
control voltage range	$V_{20\text{-}24}$		1 to 3 V
nominal brightness voltage	$V_{20\text{-}24}$		2 V
input current	I_{20}	<	10 μA
control voltage for nominal black level which equals the inserted artificial black level	$V_{20\text{-}24}$	typ.	2 V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	± 50 %
Internal signal limiting **			
signal limiting for nominal luminance (black to white = 100%)			
black		typ.	−25 %
white		typ.	125 %

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

** Brightness, contrast and saturation control in nominal position.

White point adjustment

A.C. voltage gain*				
at $V_{21,22,23-24} = 6$ V				100 %
at $V_{21,22,23-24} = 0$ V			<	60 %
at $V_{21,22,23-24} = 12$ V			>	140 %
Input resistance		$R_{21,22,23-24}$	typ.	20 kΩ

Differential output amplifier

Feedback inputs (pins 2, 5, 27)				
d.c. voltage during clamping		$V_{2,5,27-24}$	typ.	6 V
voltage difference between the feedback inputs		ΔV	<	80 mV
input resistance		$R_{2,5,27-24}$	>	100 kΩ
Output amplifiers (pins 1, 4, 26) transconductance	$\frac{\Delta I_1}{\Delta V_{2-24}} = \frac{\Delta I_4}{\Delta V_{5-24}} = \frac{\Delta I_{26}}{\Delta V_{27-24}}$		typ.	20 mA/V
integrated load resistance		$R_{1,4,26-24}$	typ.	610 Ω
output current (peak value) at $V_{1,4,26-24} = 8{,}2$ V		$\pm I_{1,4,26\,m}$	typ.	5 mA

Gain data

At nominal contrast, saturation and white point adjustment				
Voltage gain between Y-input (pin 15) and feedback inputs (pins 2, 5, 27)		$G_{2,5,27-15}$	typ.	10 dB
Frequency response (0 to 5 MHz)		$d_{2,5,27-15}$	<	3 dB
Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pins 5 and 27)		$G_{5-18} = G_{27-17}$	typ.	0 dB
Frequency response (0 to 2 MHz)		$d_{5-18} = d_{27-17}$	<	3 dB
Voltage gain between signal display inputs (pins 12, 13, 14) and feedback inputs (pins 2, 5, 27)	$G_{2-13} = G_{5-12} = G_{27-14}$		<	0 dB
Frequency response (0 to 5 MHz)	$d_{2-13} = d_{5-12} = d_{27-14}$		<	3 dB

* With input pins 21, 22 and 23 not connected an internal bias voltage of 6 V is supplied.

CHARACTERISTICS (continued)

Sandcastle detector

There are 3 internal thresholds (proportional to V_P) the following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 1)	V_{10-24}	$>$	2 V
		$<$	3 V
horizontal pulse (note 2)	V_{10-24}	$>$	4 V
		$<$	5 V
clamping pulse (note 3)	V_{10-24}	$>$	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	V_{10-24}	$>$	7,5 V
no keying	V_{10-24}	$<$	1 V

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $>$ 3,5 μs.
4. This function will also be obtained by leaving pin 10 open.

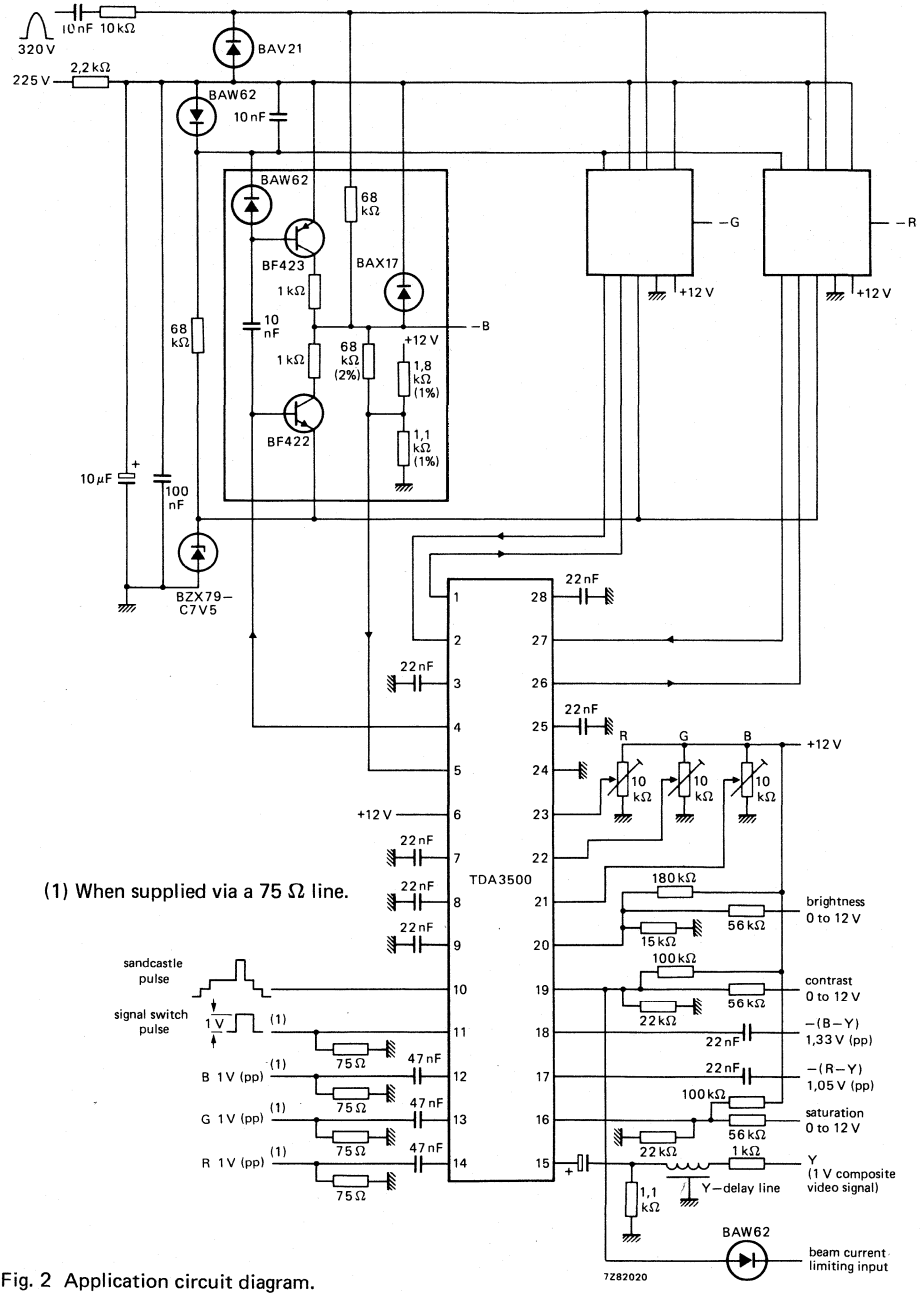


Fig. 2 Application circuit diagram.

VIDEO CONTROL COMBINATION

The TDA3501 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).
The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from an external source.
RGB signals are provided at the output to drive the video output stages.
The TDA3501 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 2 d.c. gain controls for the green and blue output signals (white point adjustment)
- beam current limiting possibility

QUICK REFERENCE DATA

Supply voltage	V_{6-24}	typ.	12 V
Supply current	I_6	typ.	100 mA
Luminance input signal (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Luminance input resistance	R_{15-24}	typ.	12 kΩ
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (peak-to-peak values)	$V_{12,13,14-24(p-p)}$	typ.	1 V
Three-level sandcastle pulse detector	V_{10-24}	typ.	2,5/4,5/8,0 V
Control voltage ranges			
brightness	V_{20-24}		1 to 3 V
contrast	V_{19-24}		2 to 4 V
saturation	V_{16-24}		2,1 to 4 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

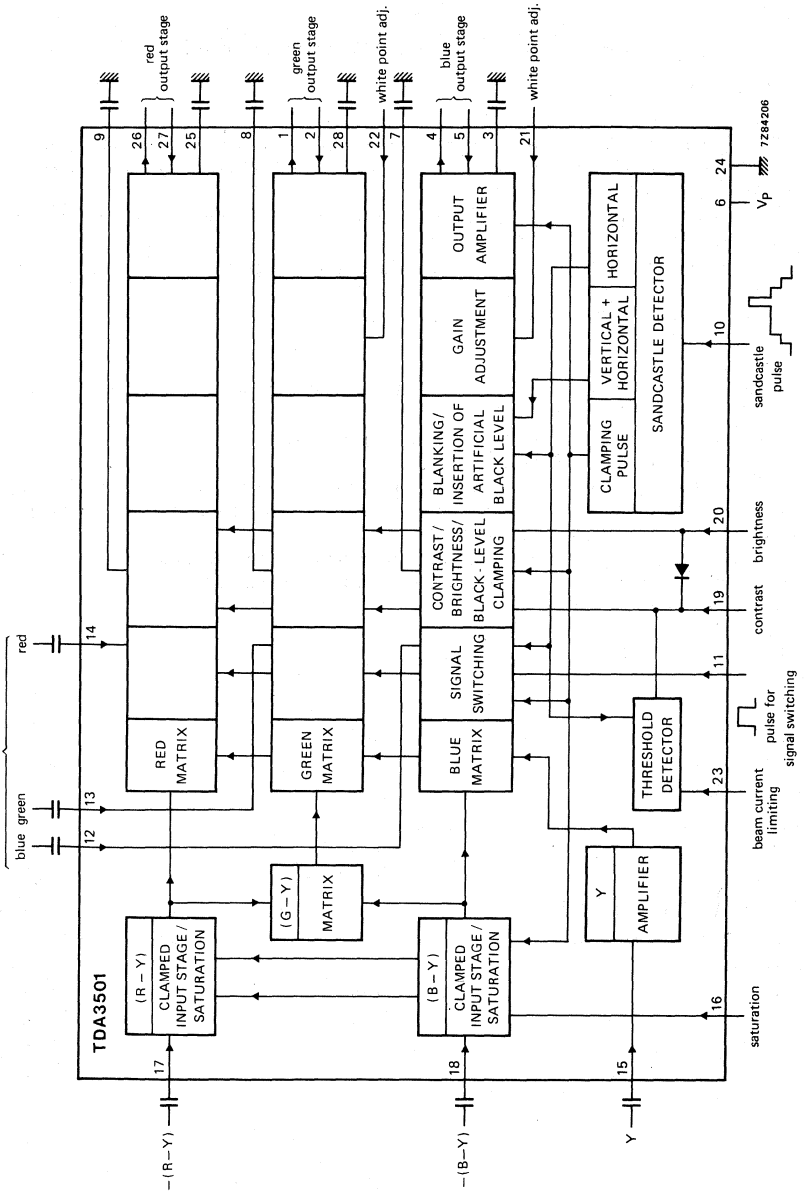


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	max.	
Supply voltage	$V_P = V_{6-24}$		–	13,2	V
Voltages with respect to pin 24					
pins 1,4,26	$V_{1,4,26-24}$		½V_P	V_P + 1	V
pins 2,5,27	$V_{2,5,27-24}$		0	V_P	V
pin 10	V_{10-24}		0	V_P	V
pin 11	V_{11-24}		–0,5	3	V
pins 16,19,20	$V_{16,19,20-24}$		0	½V_P	V
pins 21,22	$V_{21,22-24}$		0	V_P	V
pin 23	V_{23-24}		0	V_P	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage				
Current at pin 20	I_{20}	max.		5	mA
Total power dissipation	P_{tot}	max.		1,7	W
Storage temperature	T_{stg}		–25 to + 125		°C
Operating ambient temperature	T_{amb}		–20 to + 70		°C

CHARACTERISTICS

Supply voltage range	V_P		10,8 to 13,2	V
The following characteristics are measured in Fig. 2; V_P = 12 V; T_{amb} = 25 °C; $V_{18-24(p-p)}$ = 1,33 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{12,13,14-24(p-p)}$ = 1 V; unless otherwise specified				
Current consumption	I_6	typ.	100	mA
Colour difference inputs				
–(B-Y) input signal (peak-to-peak value)*	$V_{18-24(p-p)}$		1,33	V
–(R-Y) input signal (peak-to-peak value)*	$V_{17-24(p-p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control				
control voltage range for a change of saturation from –20 dB to + 6 dB	V_{16-24}		2,1 to 4	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3	V
input current	I_{16}	<	20	μA

* For saturated colour bar with 75% of maximum amplitude.

CHARACTERISTICS (continued)

(G-Y) matrix

Matrixed according the equation	$V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$		

Luminance amplifier

Input signal (peak-to-peak)	$V_{15\text{-}24(p\text{-}p)}$		0,45 V
Input resistance	$R_{15\text{-}24}$	typ.	12 kΩ
Internal d.c. voltage	$V_{15\text{-}24}$	typ.	2,7 V

RGB channels

Signal switching input voltage for insertion			
on level	$V_{11\text{-}24}$		0,9 to 1,5 V
off level	$V_{11\text{-}24}$		−0,5 to + 0,3 V
Input current	I_{11}		−100 to + 200 μA
Signal insertion			
external RGB input signal (peak-to-peak value)*	$V_{12,13,14\text{-}24(p\text{-}p)}$		1 V
internal d.c. voltage due to clamping	$V_{12,13,14\text{-}24}$	typ.	3,5 V
input current	$I_{12,13,14}$	<	5 μA
Contrast control			
control voltage range for a change of contrast from −17 dB to + 3 dB	$V_{19\text{-}24}$		2 to 4 V
nominal contrast (3 dB below max.)	$V_{19\text{-}24}$	typ.	3,4 V
control voltage for −6 dB	$V_{19\text{-}24}$	typ.	2,7 V
input current at $V_{23\text{-}24} \geqslant 6$ V	I_{19}	<	2,5 μA
Beam current limiting			
internal d.c. voltage	$V_{23\text{-}24}$	typ.	6 V
input resistance	$R_{23\text{-}24}$	typ.	10 kΩ
input current contrast control			
$V_{23\text{-}24} = 5{,}8$ V	I_{19}	typ.	0,7 mA
$V_{23\text{-}24} = 5{,}7$ V	I_{19}	typ.	10 mA
$V_{23\text{-}24} = 5{,}6$ V	I_{19}	typ.	16 mA
Brightness control			
control voltage range	$V_{20\text{-}24}$		1 to 3 V
nominal brightness voltage	$V_{20\text{-}24}$		2 V
input current	I_{20}	<	10 μA
control voltage for nominal black level which equals the inserted artificial black level	$V_{20\text{-}24}$	typ.	2 V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	± 50 %

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

Internal signal limiting*			
signal limiting for nominal luminance (black to white = 100%)			
black		typ.	−25 %
white		typ.	125 %
White point adjustment			
A.C. voltage gain **			
at $V_{21,22-24}$ = 6 V			100 %
at $V_{21,22-24}$ = 0 V		<	60 %
at $V_{21,22-24}$ = 12 V		>	140 %
Input resistance	$R_{21,22-24}$	typ.	20 kΩ
Differential output amplifier			
Feedback inputs (pins 2,5,27)			
d.c. voltage during clamping	$V_{2,5,27-24}$	5,79 to 5,95	V
voltage difference between the feedback inputs	ΔV	<	80 mV
input resistance	$R_{2,5,27-24}$	>	100 kΩ
Output amplifiers (pins 1,4,26) transconductance	$\frac{\Delta I_1}{\Delta V_{2-24}} = \frac{\Delta I_4}{\Delta V_{5-24}} = \frac{\Delta I_{26}}{\Delta V_{27-24}}$	typ.	20 mA/V
integrated load resistance	$R_{1,4,26-24}$	typ.	610 Ω
output current (peak value) at $V_{1,4,26-24}$ = 8,2 V	$\pm I_{1,4,26\ m}$	typ.	5 mA
Gain data			
At nominal contrast, saturation and white point adjustment			
Voltage gain between Y-input (pin 15) and feedback inputs (pins 2,5,27)	$G_{2,5,27-15}$	typ.	10 dB
Frequency response (0 to 5 MHz)	$d_{2,5,27-15}$	<	3 dB
Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pin 5 and 27)	$G_{5-18} = G_{27-17}$	typ.	0 dB
Frequency response (0 to 2 MHz)	$d_{5-18} = d_{27-17}$	<	3 dB
Voltage gain between signal display inputs (pins 12,13,14) and feedback inputs (pins 2,5,27)	$G_{2-13} = G_{5-12} = G_{27-14}$	typ.	0 dB
Frequency response (0 to 5 MHz)	$d_{2-13} = d_{5-12} = d_{27-14}$	<	3 dB

* Brightness, contrast and saturation control in nominal position.

** With input pins 21 and 22 not connected an internal bias voltage of 6 V is supplied.

CHARACTERISTICS (continued)

Sandcastle detector

There are 3 internal thresholds (proportional to V_P) the following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 1)	$V_{10\text{-}24}$	$>$	2 V
		$<$	3 V
horizontal pulse (note 2)	$V_{10\text{-}24}$	$>$	4 V
		$<$	5 V
clamping pulse (note 3)	$V_{10\text{-}24}$	$>$	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	$V_{10\text{-}24}$	$>$	7,5 V
no keying	$V_{10\text{-}24}$	$<$	1 V
Input current	$-I_{10}$	$<$	100 μA

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $>$ 3,5 μs.
4. This function will also be obtained by leaving pin 10 open.

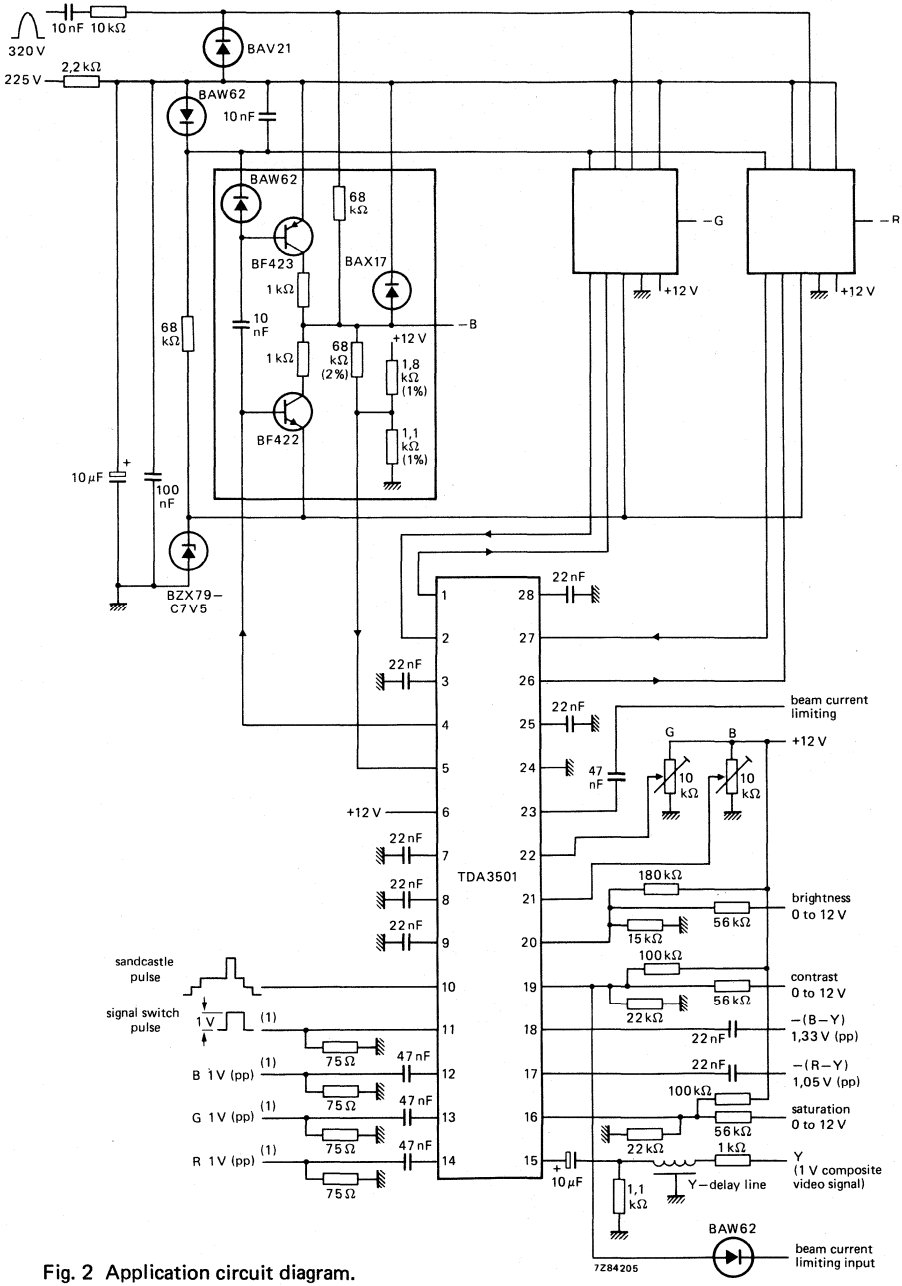


Fig. 2 Application circuit diagram.

PAL DECODER

The TDA3510 is a monolithic integrated colour decoder for the PAL standard.
The circuit incorporates the following functions:

Chrominance part

- Controlled chrominance amplifier
- Chrominance output stage with automatic standard switch for driving the 64 μs delay line
- Blanking circuit for the colour burst signal

Reference voltage and control voltage part

- 8,8 MHz reference oscillator with divider stage to obtain both the 4,4 MHz reference signals
- Gated phase comparison for an optimum noise ratio
- Circuit for obtaining the chrominance control voltage and a reference voltage
- Circuit for generating the colour killer signal and the identification signal

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Flyback blanking incorporated in the synchronous demodulators
- (R-Y) and (B-Y) signal output stages, which are controlled by the colour killer with switchable d.c. voltage levels

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{9-24}$	typ.	12 V
Supply current	I_9	typ.	58 mA
Chrominance input signal (peak-to-peak value)	$V_{1-24(p-p)}$		10 to 200 mV
Sandcastle pulse			
burst gating level	V_{20-24}	>	7,5 V
blanking level	V_{20-24}	>	1,8 V
Colour difference output signals			
peak-to-peak values			
−(R-Y) signal	$V_{11-24(p-p)}$	typ.	1,05 V ± 3 dB
−(B-Y) signal	$V_{10-24(p-p)}$	typ.	1,33 V ± 3 dB

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

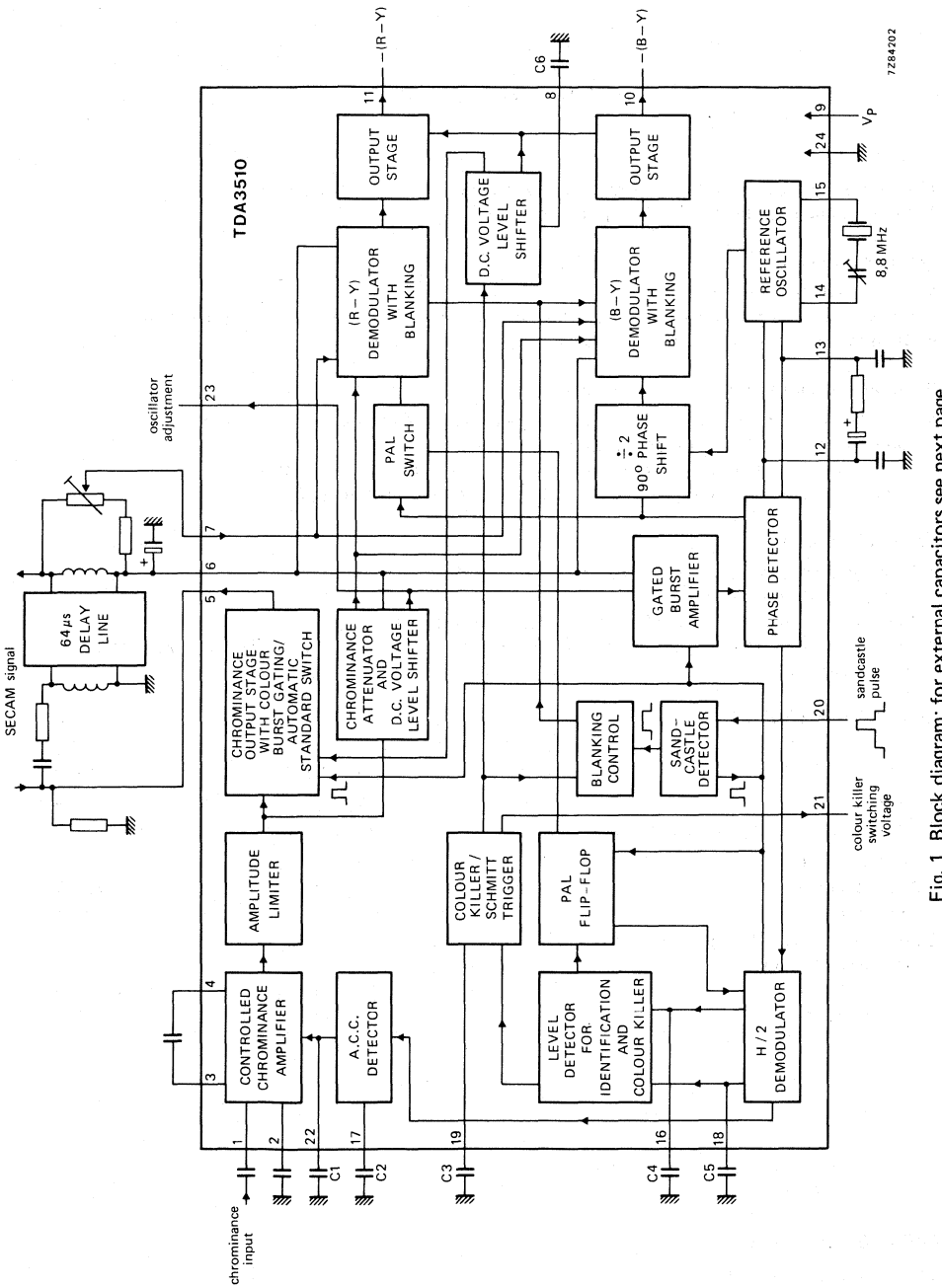


Fig. 1 Block diagram; for external capacitors see next page.

External capacitors in Fig. 1

capacitor	pins	
C1	22 – 24	filter capacitor for control voltage
C2	17 – 24	time constant for control voltage
C3	19 – 24	time constant for colour ON
C4	16 – 24	identification signal and colour OFF time constant
C5	18 – 24	load capacitor for the reference voltage
C6	8 – 24	time constant for the rise or fall time of the d.c. voltage level of the colour difference signal

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{9-24}$	10,8 to 13,2		V
Currents				
at pin 5	$-I_5$	max.	10	mA
at pins 10 and 11	$-I_{10}, -I_{11}$	max.	1	mA
at pin 21	I_{21}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature	T_{stg}	−20 to + 125		°C
Operating ambient temperature	T_{amb}	−20 to + 65		°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C

Supply current	I_9	typ.	58	mA
Chrominance part				
Chrominance signal is asymmetric (pins 1, 2)				
Input voltage range (peak-to-peak value)	$V_{1-24(p-p)}$	10 to 200		mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{1-24(p-p)}$	typ.	100	mV
Input impedance	$\lvert Z_i \rvert$	typ.	3,3	kΩ
Colour ON				
chrominance output voltage (peak-to-peak value) with 75% colour bar signal	$V_{5-24(p-p)}$	typ.	2	V
d.c. voltage at chrominance output	V_{5-24}	typ.	8	V
Colour OFF				
chrominance suppression		>	56	dB
d.c. voltage at chrominance output	V_{5-24}	typ.	4	V

CHARACTERISTICS (continued)

Reference voltage and control voltage part

Oscillator (8,8 MHz)				
Gain	$G_{14\text{-}15}$	>	8	dB
Input resistance	$R_{15\text{-}24}$	typ.	270	Ω
Output resistance	$R_{14\text{-}24}$	<	200	Ω
Catching range	Δf	typ.	500	Hz
Sandcastle pulse (pin 20)				
Burst gating level	$V_{20\text{-}24}$	>	7,5	V
Blanking level	$V_{20\text{-}24}$	>	1,8	V
Colour switching voltage (open collector)				
Maximum output current	I_{21max}	typ.	10	mA
Colour ON	$V_{21\text{-}24}$	typ.	V_P	
Colour OFF	$V_{21\text{-}24}$	<	0,5	V
Reference output voltage	$V_{18\text{-}24}$	typ.	5,5	V
Colour killer voltages				
colour OFF at	$V_{18\text{-}16}$	typ.	0	V
or at	$V_{19\text{-}24}$	>	6	V
colour ON at	$V_{18\text{-}16}$	typ.	1,5	V
or at	$V_{19\text{-}24}$	<	4	V
Colour unkill delay; depends on C3	t_d	typ.	20	ms/μF
Identification ON	$V_{16\text{-}18}$	<	200	mV

Demodulator part

Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{7\text{-}24(p\text{-}p)}$	typ.	250	mV
Colour difference output signals (peak-to-peak values)				
−(R-Y) signal	$V_{11\text{-}24(p\text{-}p)}$	typ.	1,05 V ± 3	dB
−(B-Y) signal	$V_{10\text{-}24(p\text{-}p)}$	typ.	1,33 V ± 3	dB
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{11\text{-}24}}{V_{10\text{-}24}}$	typ.	0,79 ± 10	%
D.C. voltage at colour difference outputs				
at colour ON	$V_{10;\,11\text{-}24}$	typ.	8	V
at colour OFF	$V_{10;\,11\text{-}24}$	typ.	4	V
Signal attenuation at colour OFF		>	60	dB
Residual 4,4 MHz signal	$V_{10;\,11\text{-}24}$	<	20	mV
H/2 ripple at (R-Y) output (peak-to-peak value) without input signal	$V_{11\text{-}24(p\text{-}p)}$	<	10	mV

SECAM DECODER

The TDA3520 is a monolithic integrated circuit which contains all the functions necessary for decoding the SECAM signal from the composite video and which offers the colour difference signals − (R−Y) and − (B−Y) to the video circuits TDA3500 or TDA 3501 in order to complete the SECAM decoding system.

By simply adding the PAL decoder circuit TDA3510, the SECAM system can be extended to receive SECAM/PAL signals as well. The 64 μs delay line is used in common and all system switching functions are performed automatically.

One of the main features of the TDA3520 is that only the clock filter has to be adjusted; all the other adjustments can be left out due to usage of PLL−type FM demodulators, the system of horizontal identification and the gain controlled chrominance amplifier.

The TDA3520 incorporates the following main functions:

- gain controlled chrominance amplifier
- delay line amplifier (fixed gain of nom. 8), controlled by the colour killer (black−white/colour and SECAM/PAL commutation)
- limiter stages for direct signals and delayed signals
- permutator
- horizontal identification system; in PAL/SECAM receivers automatic standard switching is obtained if only a fixed phase shift circuit is added
- internal clamping generator and identification (1 μs) triggered either by the sandcastle pulse or by the video signal via the internal sync separator together with the flyback pulse
- (B−Y) and (R−Y) demodulators (without control) with burst level memory by means of an external capacitor
- circuits for horizontal and vertical blanking, during which de-emphasizing and restoring of black levels in the (R−Y) and (B−Y) signals occurs
- low-impedance output stages controlled by the colour killer (black/white/colour and SECAM/PAL switches)
- possibility for vertical identification by adding a simple external circuit
- colour killer output with H/2 information is available to control the luminance suppression filter from line to line.

QUICK REFERENCE DATA

Supply voltage (pins 5, 14, 15)	V_P	typ.	12 V
Supply current ($I_5 + I_{14} + I_{15}$)	I_P	typ.	90 mA
Input voltage range (peak-to-peak value)	$V_{27\text{-}28\ (p\text{-}p)}$	10 to	200 mV
A.G.C. control range		>	26 dB
Colour killer output current (SECAM not identified)	I_8	<	5 mA
PLL demodulator catching range	Δf	>	1 MHz
−(R−Y) output voltage (peak-to-peak value)	$V_{16\text{-}24\ (p\text{-}p)}$	typ.	1,05 V
−(B−Y) output voltage (peak-to-peak value)	$V_{13\text{-}24\ (p\text{-}p)}$	typ.	1,33 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

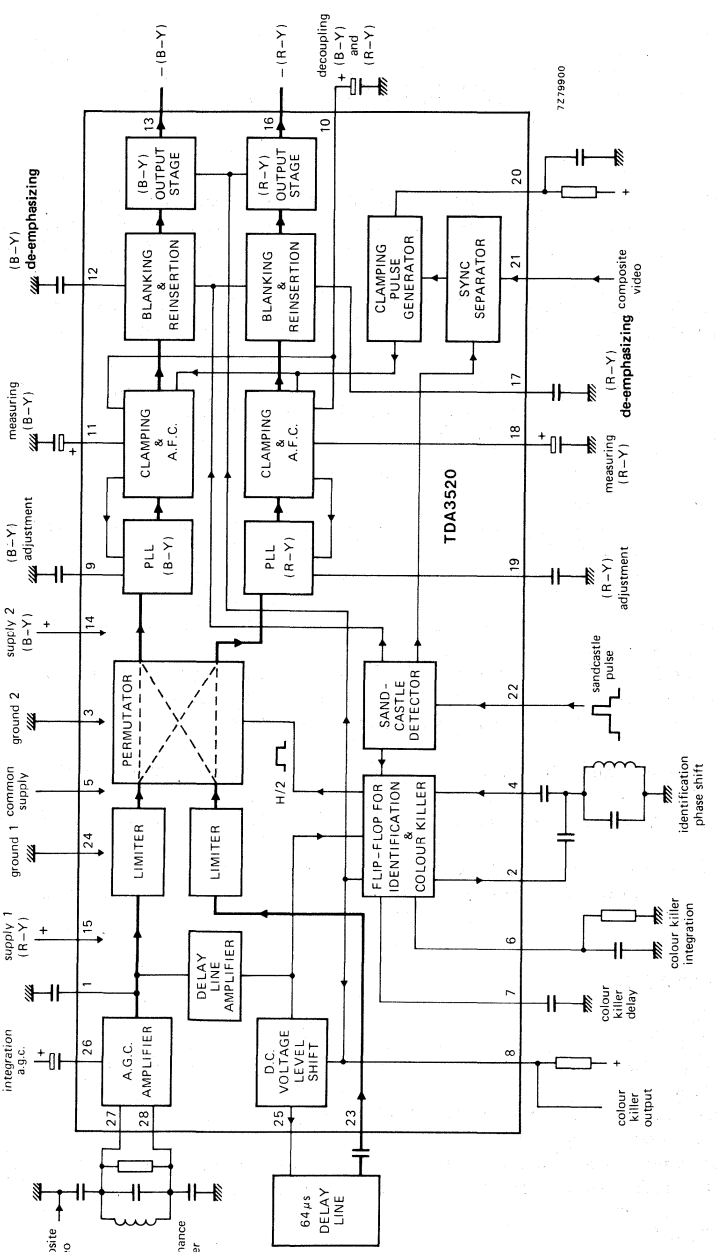


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 5 and 14)	$V_P = V_{5,14,15-3,24}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 70 °C

CHARACTERISTICS

Supply voltage range (pins 5,14 and 15)	V_P		10,8 to 13,2 V
The following characteristics are measured in Fig. 2; V_P = 12 V; T_{amb} = 25 °C			
Supply current	$I_P = I_5 + I_{14} + I_{15}$	typ.	90 mA
Chrominance amplifier (pins 27 and 28)			
Input voltage range (peak-to-peak value)	$V_{27-28\ (p-p)}$		10 to 200 mV
Input resistance	R_{27-28}	>	50 kΩ
A.G.C. control range at 3 dB output signal variation at pin 25		>	26 dB
Delay line amplifier (pin 25)			
Output voltage (peak-to-peak value)	$V_{25-24\ (p-p)}$	typ.	2,6 V
Output impedance	$\lvert Z_{25-24} \rvert$	<	100 Ω
D.C. output voltage			
SECAM identified	V_{25-24}	typ.	8 V
SECAM not identified	V_{25-24}	typ.	4,5 V
Attenuation (SECAM not identified)		typ.	60 dB
Delay line input (pin 23)			
Input voltage (peak-to-peak value) *	$V_{23-24\ (p-p)}$	typ.	325 mV
Input resistance	R_{23-24}	>	3 kΩ
Identification circuit (pins 2 and 4)			
Output voltage (phase-shift circuit input) (peak-to-peak value)	$V_{2-24\ (p-p)}$	typ.	2,8 V
Output resistance	R_{2-24}	<	200 Ω
Input voltage (phase-shift circuit output) (peak-to-peak value)	$V_{4-24\ (p-p)}$	typ.	300 mV
Input resistance	R_{4-24}	>	1 kΩ

* Corresponds with an attenuation of nom. 18 dB at pins 23 and 25 (delay line).

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

Colour killer output (pin 8; open collector)			
Saturation voltage (SECAM not identified)	$V_{8\text{-}24}$	typ.	300 mV
Output current (SECAM not identified)	$-I_8$	<	5 mA
Output current (SECAM identified; blue line)	$-I_8$	typ.	0 mA
Output current (SECAM identified; red line)	$-I_8$	typ.	0,5 mA
Sync separator (pin 21)			
Slicing level *	$V_{21\text{-}24}$	typ.	2,5 V
Video input voltage (peak-to-peak value) **	$V_{21\text{-}24\ (p\text{-}p)}$	typ.	1 V
Sandcastle input (or flyback pulse) (pin 22)			
Blanking level for driving the sync separator	$V_{22\text{-}24}$		1,0 to 2,0 V *
Flip-flop slicing level	$V_{22\text{-}24}$		3,0 to 4,0 V *
Maximum input current	$I_{22\ max}$	<	100 μA
Demodulators (pins 9 and 19)			
PLL demodulator catching range	Δf	>	1 MHz
Equivalent error at the reinserted reference levels	Δf_o	<	4 kHz
Colour difference output stages (pins 13 and 16)			
Output voltages (peak-to-peak values)			
−(R−Y) signal	$V_{16\text{-}24\ (p\text{-}p)}$	typ.	1,05 V
−(B−Y) signal	$V_{13\text{-}24\ (p\text{-}p)}$	typ.	1,33 V
D.C. output voltage	$V_{13,16\text{-}24}$	typ.	6 V *
Output resistance	$R_{13,16\text{-}24}$	<	100 Ω
Attenuation (SECAM not identified)		typ.	62 dB
H/Z ripple at the outputs (peak-to-peak value)	$V_{13,16\text{-}24\ (p\text{-}p)}$	<	10 mV

*Proportional to the supply voltage.

** Capacitive coupling; see Fig. 2.

DEVELOPMENT SAMPLE DATA

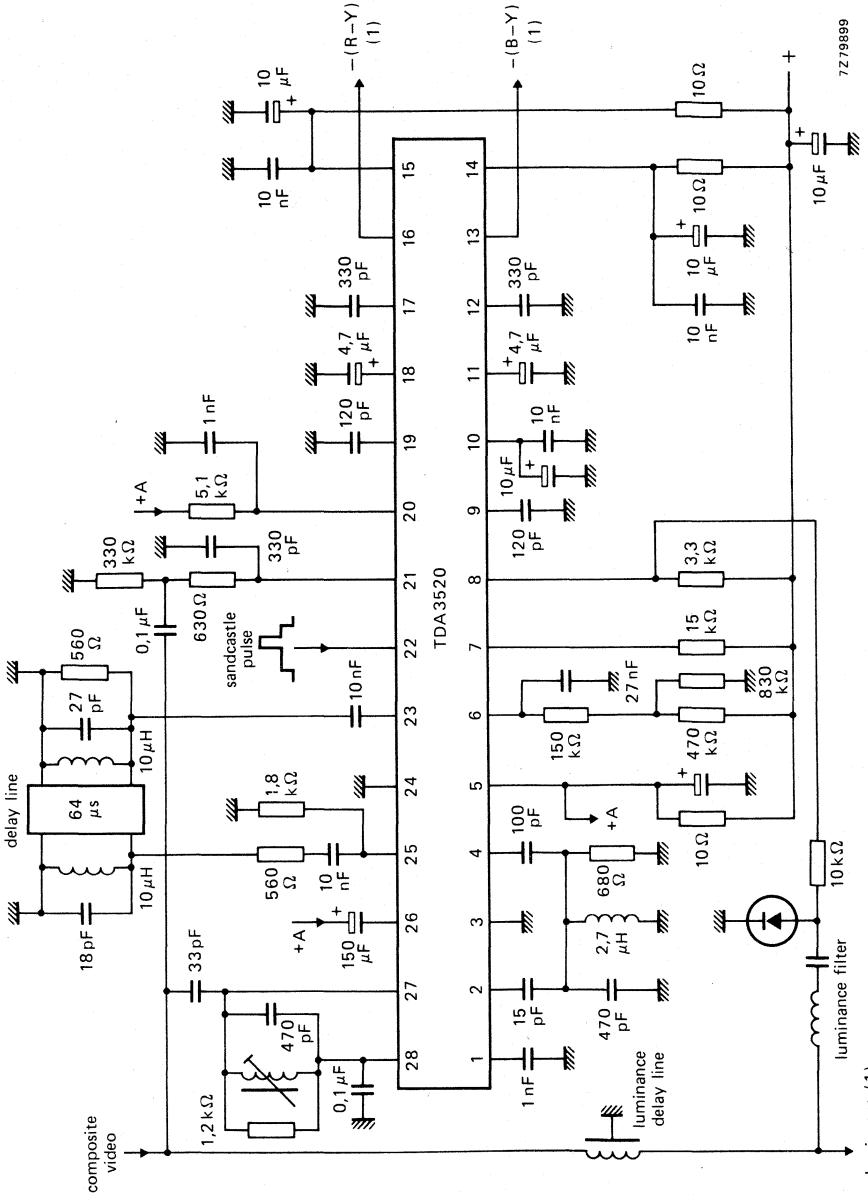


Fig. 2 Application diagram.

(1) To TDA3500 or TDA3501

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA3540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.
It incorporates the following functions:

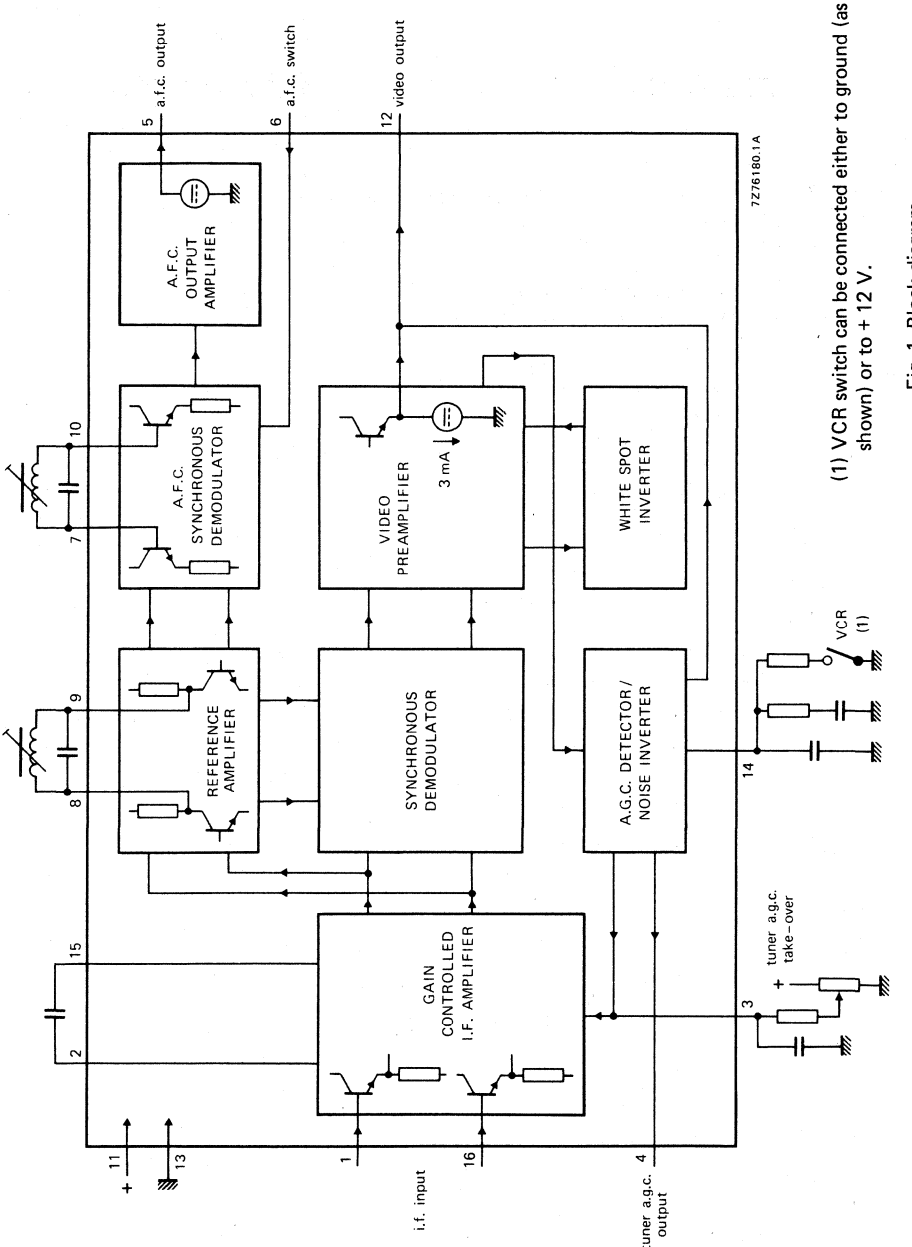
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator with excellent intermodulation
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with a.f.c. on/off switch
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- external video switch which switches off the video output; e.g. for insertion of a VCR playback signal, by either a high or a low level.

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12 V
Supply current	I_{11}	typ.	53 mA
I.F. input sensitivity (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	70 μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,7 V
I.F. voltage gain control range	G_v	typ.	65 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing for Δf = 70 kHz	$\Delta V_{5\text{-}13}$	typ.	10 V

PACKAGE OUTLINES

TDA3540 : 16-lead DIL; plastic (SOT-38).
TDA3540Q: 16-lead QIL; plastic (SOT-58).



(1) VCR switch can be connected either to ground (as shown) or to + 12 V.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13,2	V
Tuner a.g.c. voltage	V_{4-13}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 70	°C

CHARACTERISTICS (measured in Fig. 5)

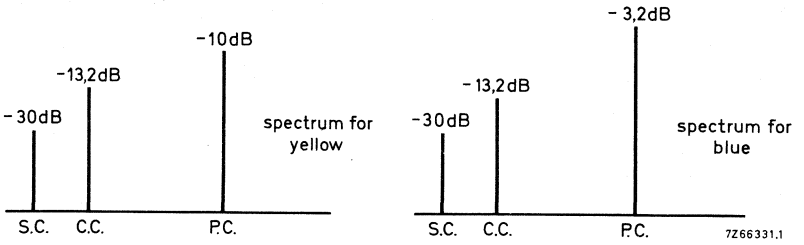
Supply voltage range	V_{11-13}	typ.	12 10,2 to 13,2	V V
The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V				
I.F. input voltage for onset of a.g.c. (r.m.s. value)				
at f = 38,9 or 45,75 MHz	$V_{1-16(rms)}$	typ.	70	μV
at f = 58,75 MHz	$V_{1-16(rms)}$	typ.	90	μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	10 kΩ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ.	6 ± 0,3	V*
Top sync output level	V_{12-13}	typ.	3,07 2,9 to 3,2	V V
I.F. voltage gain control range	G_v	typ.	65	dB
Bandwidth of video amplifier (3 dB)	B	typ.	9	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57	dB**
Differential gain	dG	typ. <	5 10	% %
Differential phase	dφ	typ. <	2° 10°	

* So-called 'projected zero point', e.g. with switched demodulator.

** $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*	>	60 dB
	typ.	65 dB
yellow*	>	54 dB
	typ.	58 dB
at 3,3 MHz**	>	60 dB
	typ.	70 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

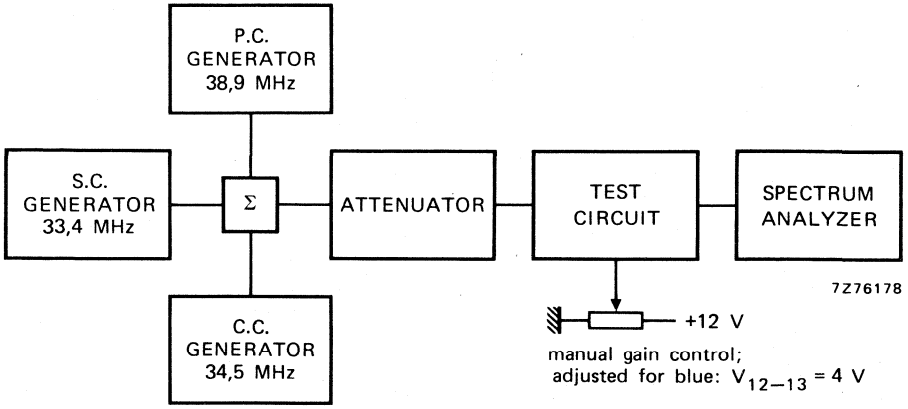


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6$ dB. ** $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$.

Carrier signal at video output		<	30 mV
2nd harmonic of carrier at video output		<	30 mV
White spot inverter threshold level (Fig. 4)		typ.	6,6 V
White spot insertion level (Fig. 4)		typ.	4,7 V
Noise inverter threshold level (Fig. 4)		typ.	1,8 V
Noise insertion level (Fig. 4)		typ.	3,8 V
External video switch (VCR) switches off the output at	V_{14-13}	<	1,5 V
		>	10,5 V

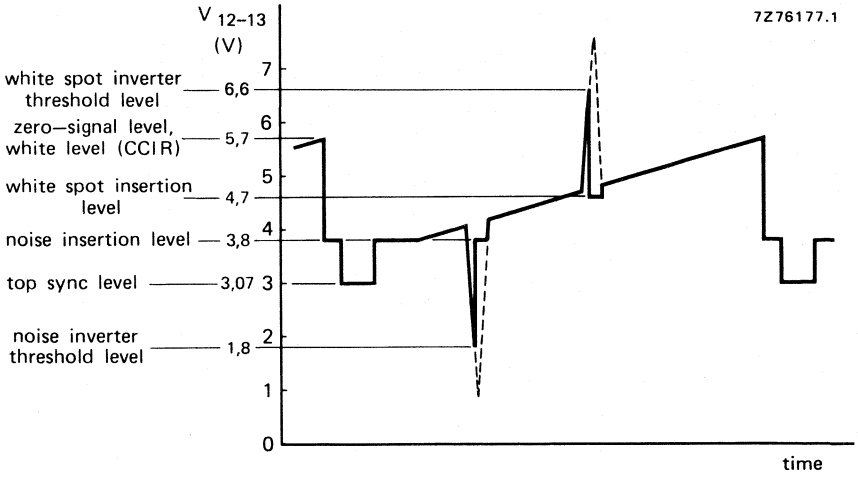


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		10 to 0 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 3 V; V_{4-13} = 12 V	I_4	<	10 μA
Lowest tuner a.g.c. take-over point	V_i	<	10 mV
Highest tuner a.g.c. take-over point	V_i	>	100 mV
Maximum a.f.c. output voltage swing	ΔV_{5-13}	>	10 V
		typ.	11 V
Detuning for a.f.c. output voltage swing of 10 V f = 38,9 MHz	Δf	typ.	70 kHz
		<	150 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V
			4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3,2 V
A.F.C. switches off at:	V_{6-13}	<	2,0 V

APPLICATION INFORMATION

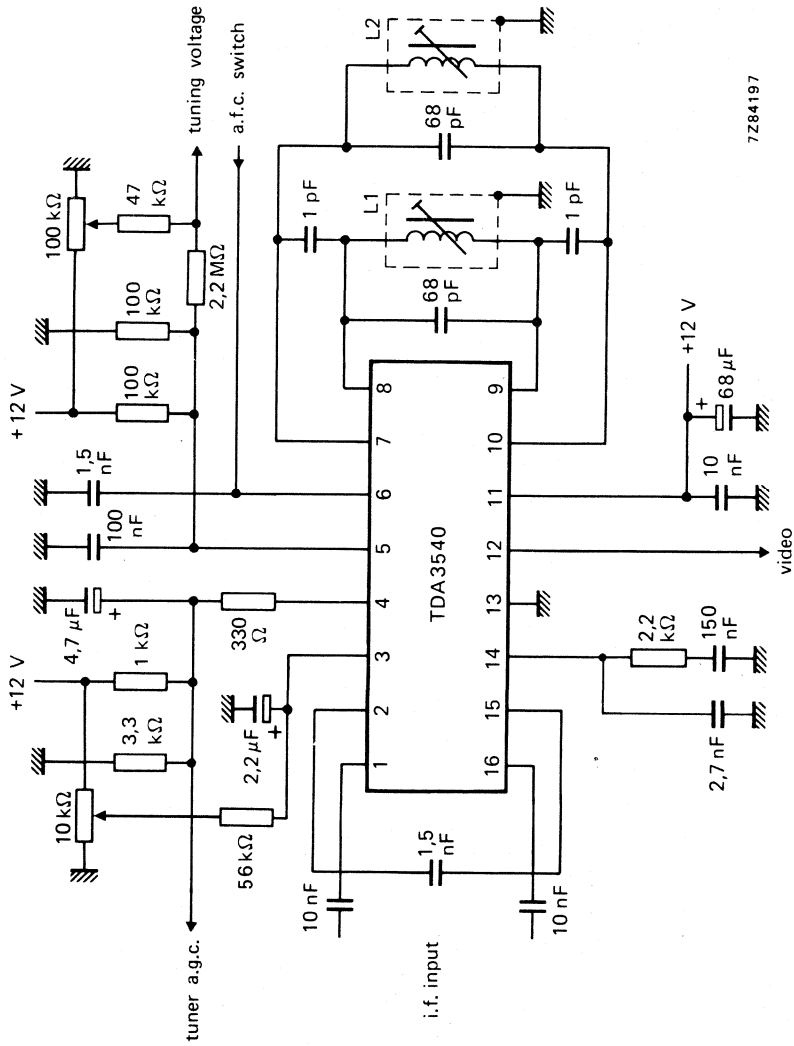
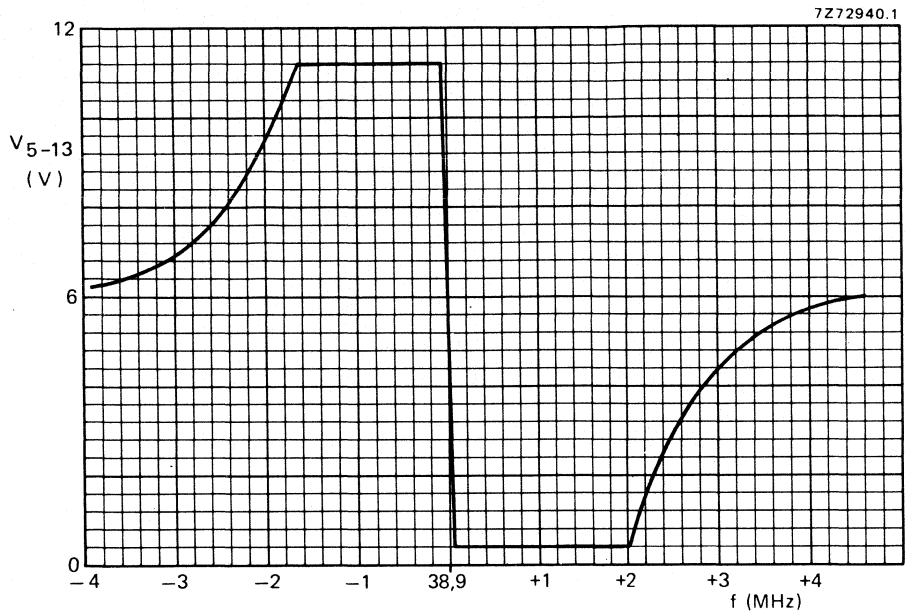


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f_o = 38,9 MHz.



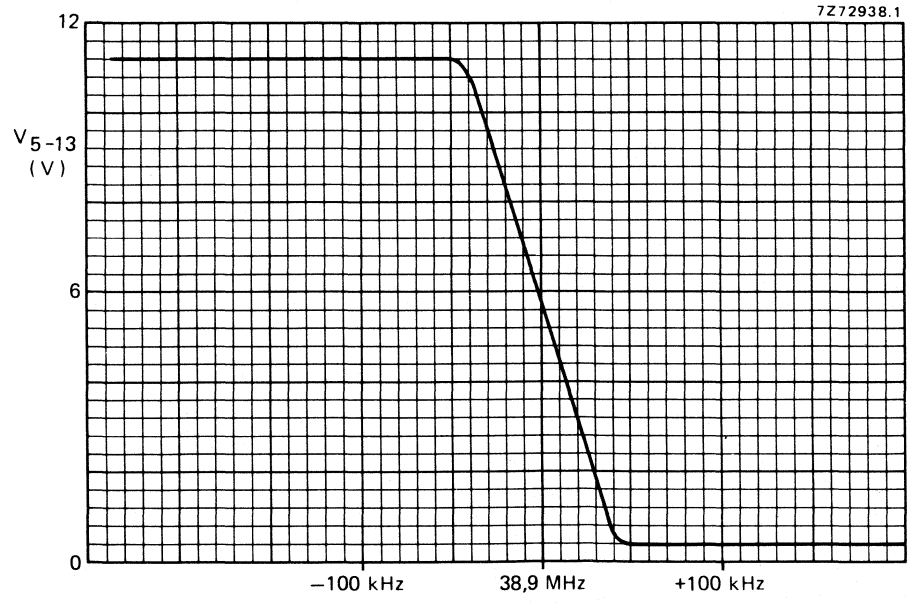


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

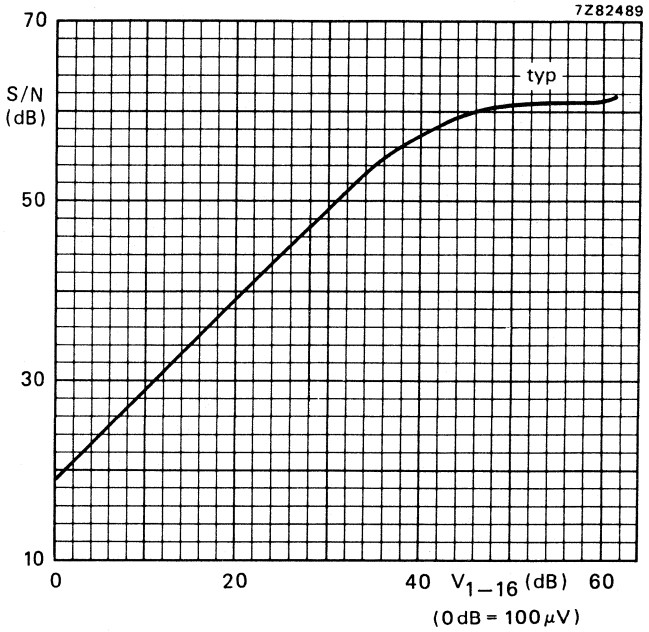


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA3541 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

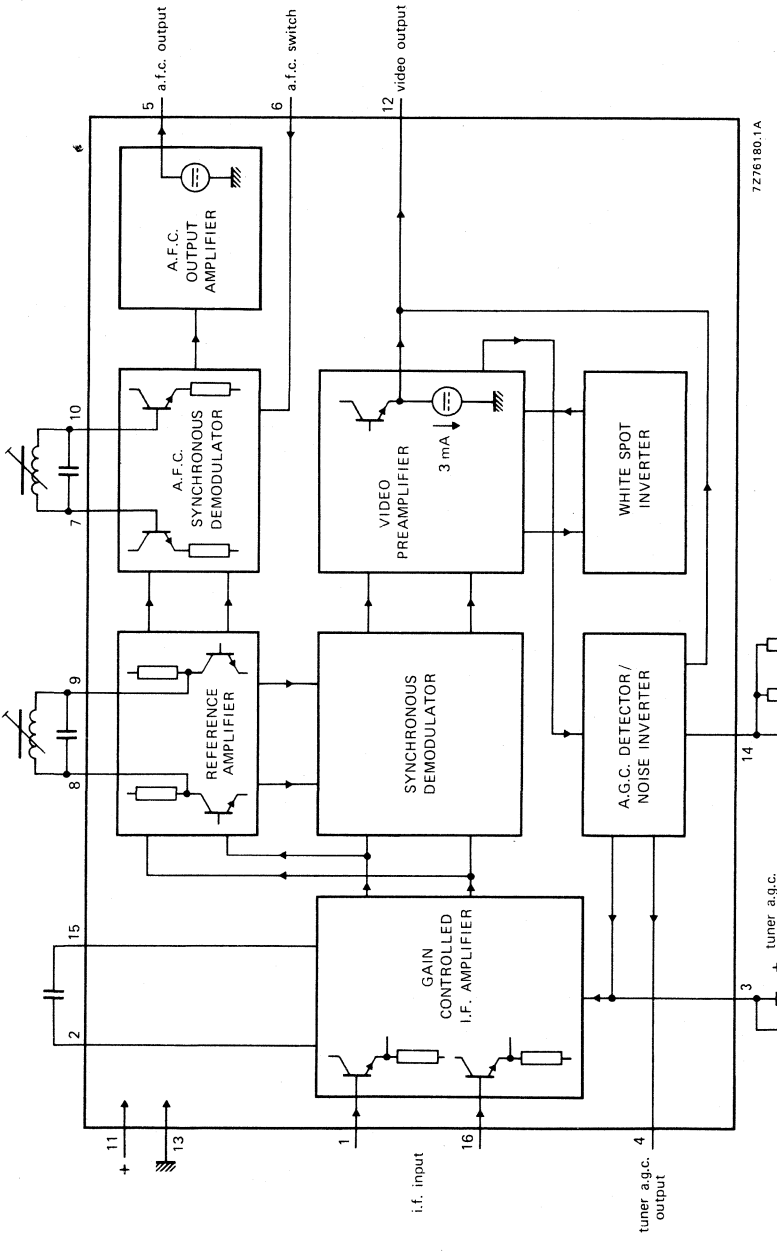
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator with excellent intermodulation
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with a.f.c. on/off switch
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- external video switch which switches off the video output; e.g. for insertion of a VCR playback signal, by either a high or a low level

QUICK REFERENCE DATA

Supply voltage	V_{11-13}	typ.	12 V
Supply current	I_{11}	typ.	53 mA
I.F. input sensitivity (r.m.s. value)	$V_{1-16(rms)}$	typ.	70 μV
Video output voltage (white at 10% of top sync)	$V_{12(p-p)}$	typ.	2,7 V
I.F. voltage gain control range	G_V	typ.	65 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing for Δf = 70 kHz	ΔV_{5-13}	typ.	10 V

PACKAGE OUTLINES

TDA3541 : 16-lead DIL; plastic (SOT-38).
TDA3541Q: 16-lead QIL; plastic (SOT-58).



(1) VCR switch can be connected either to ground (as shown) or to + 12 V.

Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2 V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,1 W
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 70 °C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ.	12 V
			10,2 to 13,2 V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V

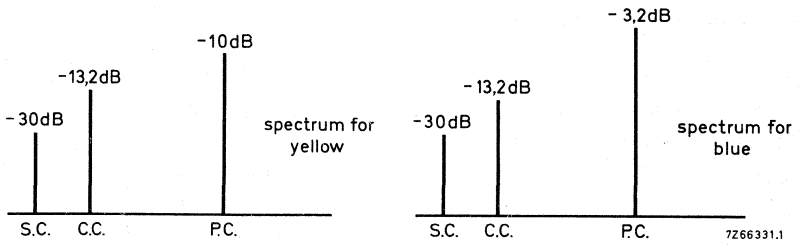
I.F. input voltage for onset of a.g.c. (r.m.s. value)			
at f = 38,9 or 45,75 MHz	$V_{1\text{-}16(rms)}$	typ.	70 μV
at f = 58,75 MHz	$V_{1\text{-}16(rms)}$	typ.	90 μV
Differential input impedance	$\lvert Z_{1\text{-}16} \rvert$	typ.	10 kΩ in parallel with 2 pF
Zero-signal output level	$V_{12\text{-}13}$	typ.	6 ± 0,3 V*
Top sync output level	$V_{12\text{-}13}$	typ.	3,07 V
			2,9 to 3,2 V
I.F. voltage gain control range	G_v	typ.	65 dB
Bandwidth of video amplifier (3 dB)	B	typ.	9 MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB**
Differential gain	dG	typ.	5 %
		<	10 %
Differential phase	$d\varphi$	typ.	2°
		<	10°

* So-called 'projected zero point', e.g. with switched demodulator.

** $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*	>	60 dB
	typ.	65 dB
yellow*	>	54 dB
	typ.	58 dB
at 3,3 MHz**	>	60 dB
	typ.	70 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

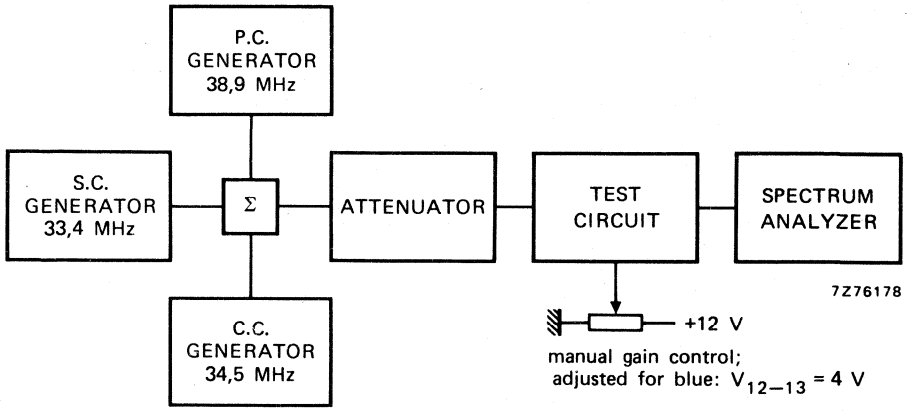


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB.

** $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

Carrier signal at video output		<	30 mV
2nd harmonic of carrier at video output		<	30 mV
White spot inverter threshold level (Fig. 4)		typ.	6,6 V
White spot insertion level (Fig. 4)		typ.	4,7 V
Noise inverter threshold level (Fig. 4)		typ.	1,8 V
Noise insertion level (Fig. 4)		typ.	3,8 V
External video switch (VCR) switches off the output at	V_{14-13}	<	1,5 V
		>	10,5 V

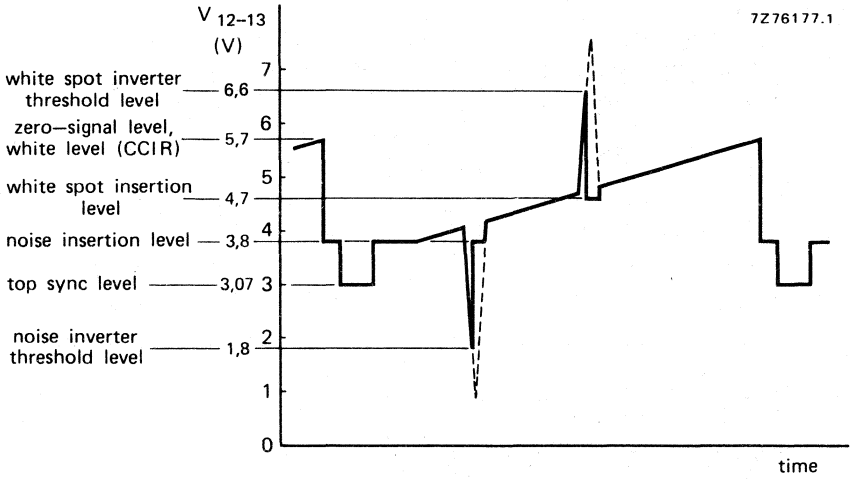


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 10 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3 V
Tuner a.g.c. output leakage current V_{14-13} = 11 V; V_{4-13} = 12 V	I_4	<	10 μA
Lowest tuner a.g.c. take-over point	V_i	<	10 mV
Highest tuner a.g.c. take-over point	V_i	>	100 mV
Maximum a.f.c. output voltage swing	ΔV_{5-13}	>	10 V
		typ.	11 V
Detuning for a.f.c. output voltage swing of 10 V f = 38,9 MHz	Δf	typ.	70 kHz
		<	150 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V
			4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3,2 V
A.F.C. switches off at:	V_{6-13}	<	2,0 V

DEVELOPMENT SAMPLE DATA

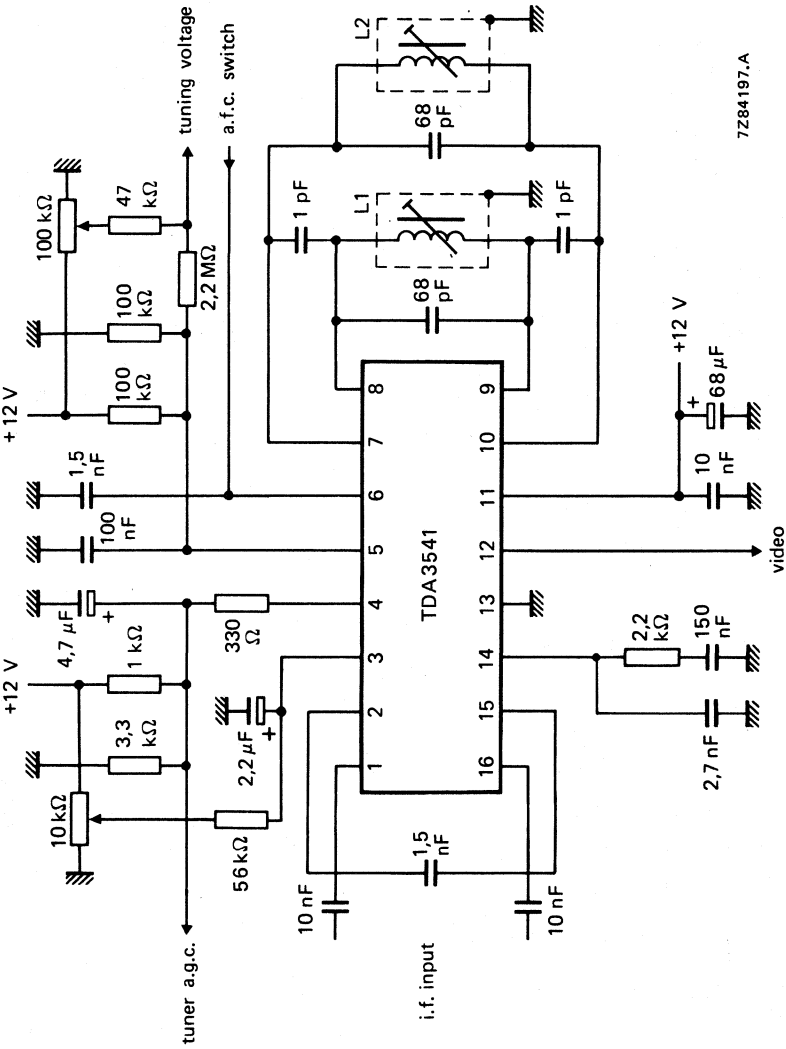


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f_o = 38,9 MHz.

APPLICATION INFORMATION

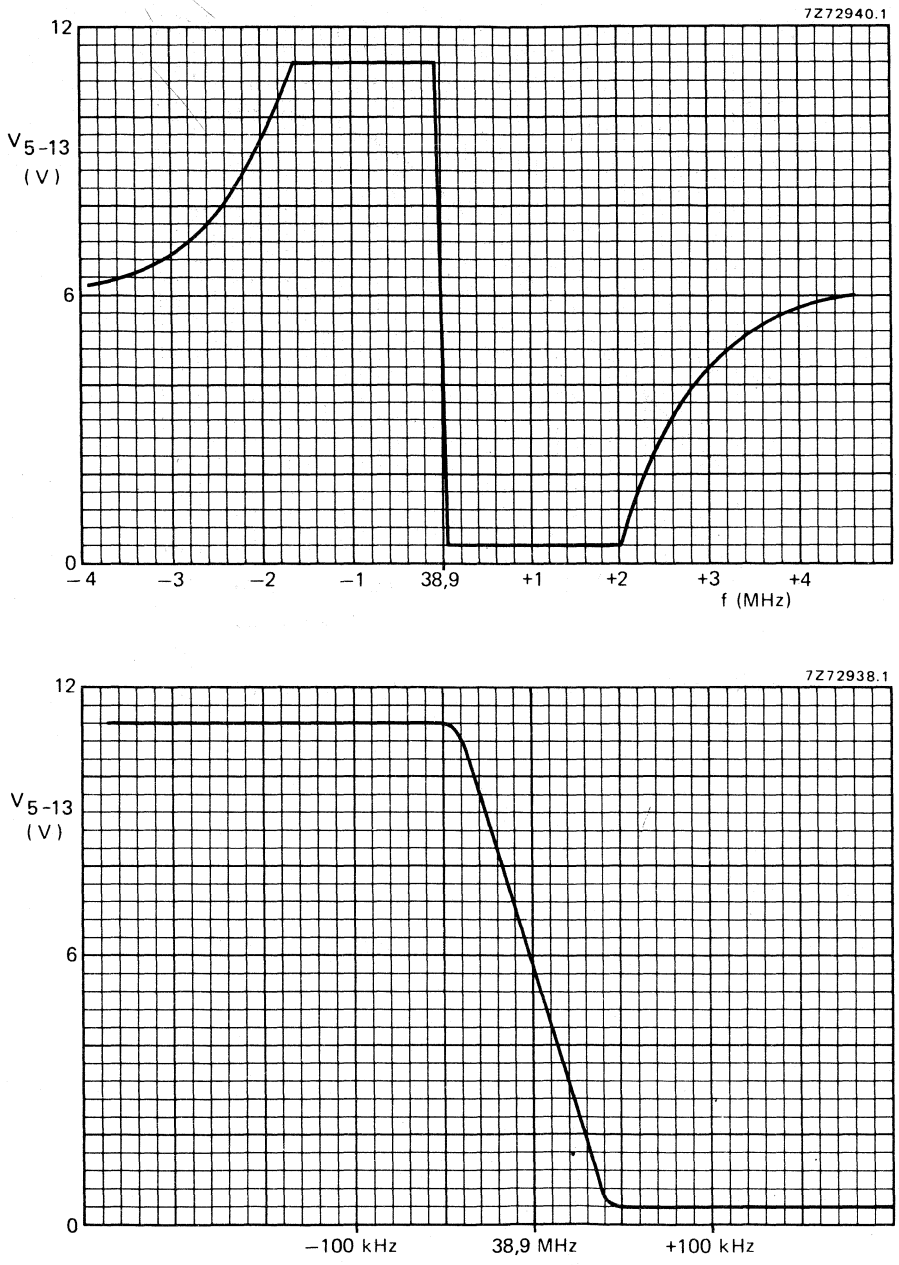


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

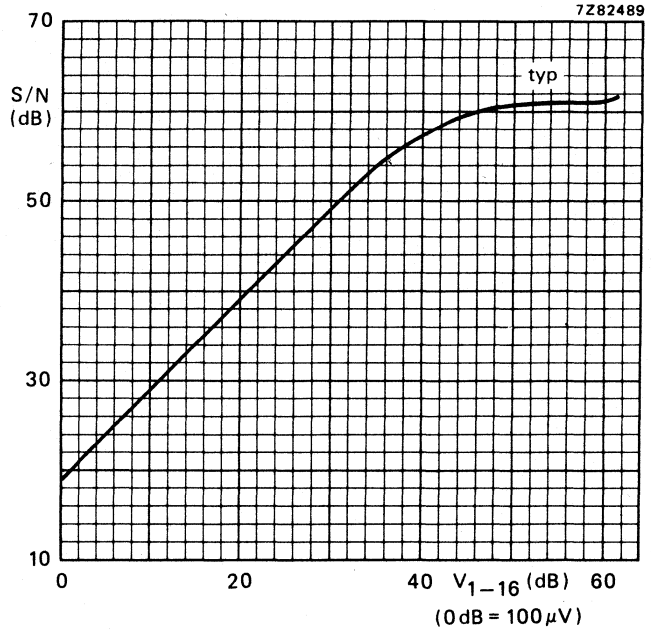


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

PAL DECODER

The TDA3560 is a monolithic integrated colour decoder for the PAL standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

QUICK REFERENCE DATA

Supply voltage	V_{1-27}	typ.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	5	V
Contrast control range		typ.	20	dB
Saturation control range		typ.	50	dB
Input for fast video-data signal switching	V_{9-27}	typ.	1	V
Blanking input voltage	V_{8-27}	typ.	1,5	V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

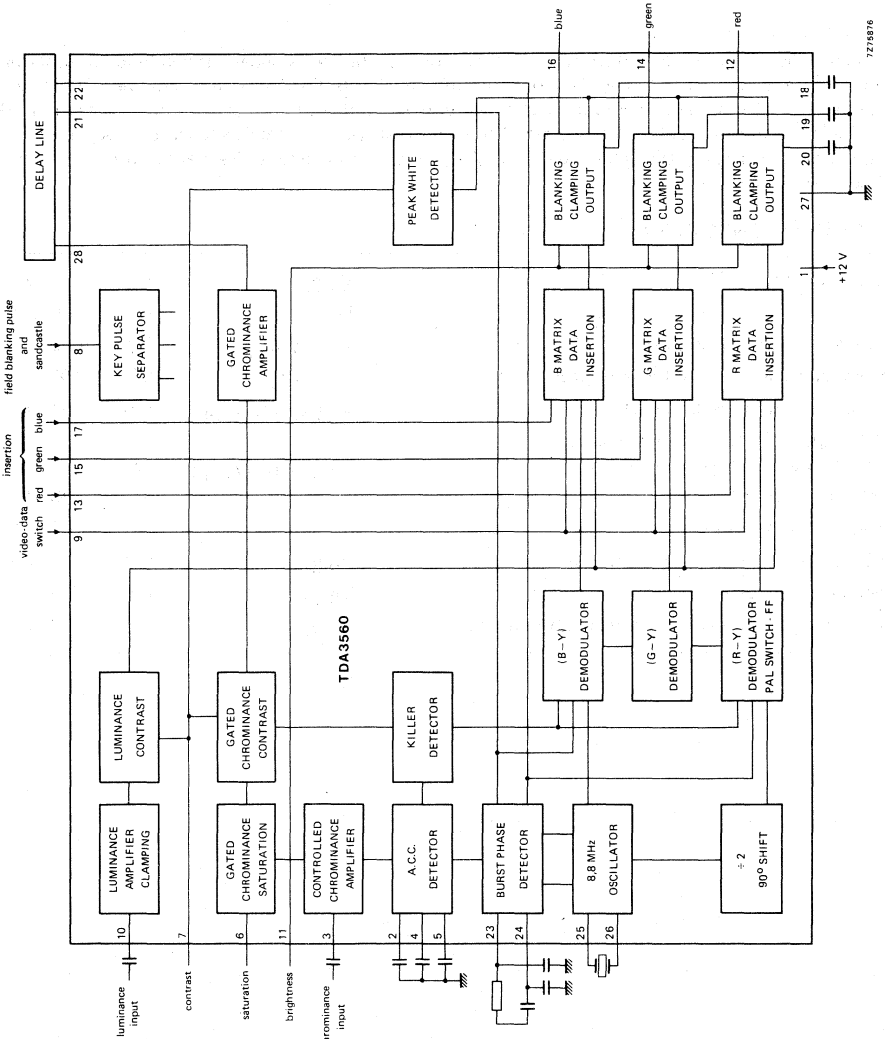


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{1-27}$	–	13,2	V
Input saturation voltage	V_{6-27}	0	V_P	V
Input contrast voltage	V_{7-27}	0	V_P	V
Input blanking pulse and sandcastle	V_{8-27}	0	V_P	V
Input video-data switch voltage	V_{9-27}	0	V_P	V
Input brightness voltage	V_{11-27}	0	V_P	V
Power dissipation	see Fig. 2			
Storage temperature	T_{stg}	−25 to	+ 150	°C
Operating ambient temperature	T_{amb}	−25 to	+ 65	°C

CHARACTERISTICS

V_{1-27} = 12 V; $V_{10-27(p-p)}$ = 0,45 V; $V_{3-27(p-p)}$ = 500 mV; T_{amb} = 25 °C; measured in Fig. 6; unless otherwise specified

Supply voltage range	V_P	typ.	12 8 to 13,2	V V
Supply current	I_1	typ.	85	mA
Luminance amplifier				
Input voltage (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Input current	I_{10}	<	1	μA
Contrast control range			−17 to + 3	dB
Contrast control voltage range	see Fig. 3			
Chrominance amplifier				
Input voltage (peak-to-peak value)	$V_{3-27(p-p)}$		55 to 1100	mV
A.C.C. control range		>	30	dB
Output signal (peak-to-peak value) * burst signal (peak-to-peak value) = 0,5 V	$V_{28-27(p-p)}$	typ.	1,7	V
Saturation control range		>	50	dB
Saturation control voltage range	see Fig. 4			
Phase shift between burst and chrominance *		<	5°	
Tracking between luminance and chrominance with contrast control over a range of 10 dB, starting at maximum contrast		typ.	1	dB

* At nominal contrast and saturation setting. Nominal setting = maximum contrast −3 dB; maximum saturation −6 dB.

CHARACTERISTICS (continued)

Reference oscillator

Phase locked loop:			
– catching range (note 1)		>	500 Hz
– phase shift (note 2)		<	5°
Oscillator:			
– input resistance	$R_{26\text{-}27}$	typ.	300 Ω
– input capacitance	$C_{26\text{-}27}$	<	10 pF
– output resistance	$R_{25\text{-}27}$	typ.	200 Ω
A.C.C. generation:			
– reference voltage	$V_{4\text{-}27}$	typ.	4,6 V
– control voltage at nominal input signal	$V_{2\text{-}27}$	typ.	4,7 V
– control voltage without burst	$V_{2\text{-}27}$	typ.	2,4 V

Demodulator circuit

Input burst signal amplitude (peak-to-peak value)	$V_{21,22\text{-}27(p\text{-}p)}$	typ.	60 mV
Ratio of demodulated signals without luminance input signal			
(B-Y)/(R-Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78
(G-Y)/(R-Y)	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	–0,51
(G-Y)/(B-Y)	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	–0,19

RGB matrix and amplifiers

Output voltage (peak-to-peak value) (note 3)	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5 V
Maximum white level		typ.	9,3 V
Birghtness control voltage range	see Fig. 5		
Relative spread between R, G and B output signals		<	10 %
Variation of black level with contrast control	ΔV	<	200 mV
Relative black-level variation between the three stages during variation of contrast saturation, brightness and supply voltage		<	20 mV
Differential black-level drift over a temperature range of 40 °C		<	20 mV
Blanking level at RGB outputs		typ.	2,1 V
Signal-to-noise ratio of output signals (note 4)	S/N	>	62 dB

Notes
1. Frequency referred to 4,4 MHz carrier frequency.
2. For ± 400 Hz deviation of the oscillator frequency.
3. For nominal setting of the controls.
4. The signal-to-noise ratio is specified as the nominal peak-to-peak output signal with respect to r.m.s. noise.

Residual 8,8 MHz and higher harmonics on RGB-outputs (peak-to-peak value)		<	150 mV
Output impedance RGB outputs	$\lvert Z_o \rvert$	typ.	50 Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3 dB
Signal insertion			
Input signals for an RGB output voltage of 5 V (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1 V
Difference between the black levels of the RGB signals and the inserted signals at the output	ΔV	<	60 mV
Output rise time	t_r	typ.	50 ns
Differential delay time for the three channels	t_d	<	40 ns
Video-data switching			
Input voltage for switching from video to inserted signals	V_{9-27}		0,9 to 2 V
Input voltage for no data insertion	V_{9-27}	<	0,3 V
Delay between signal switching at the output and the signal switching input pulse at pin 9	t_d	<	20 ns
Sandcastle and field blanking input (pin 8)			
Burst gate and clamping pulse	V_{8-27}	>	7,5 V
RGB blanking level			
on	V_{8-27}		2 to 6,5 V
off	V_{8-27}	<	0,8 V

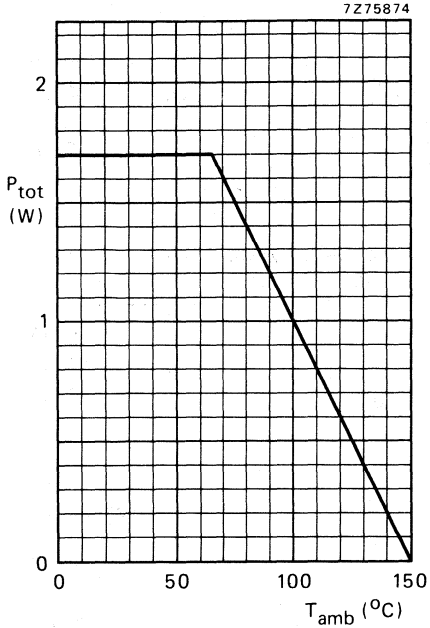


Fig. 2 Power derating curve.

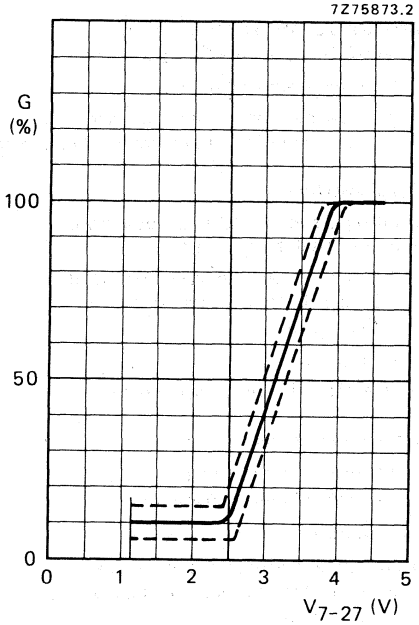


Fig. 3 Contrast control voltage range.

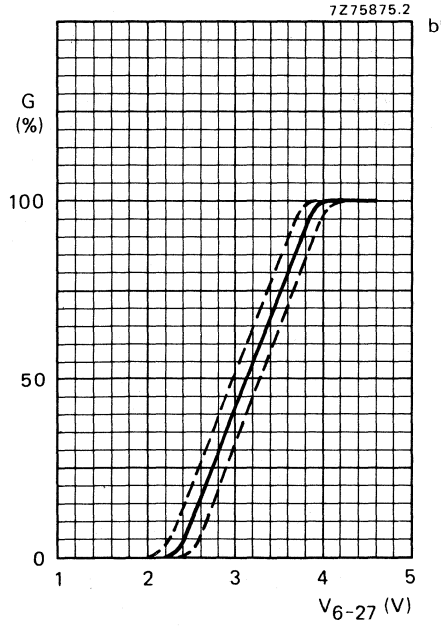


Fig. 4 Saturation control voltage range.

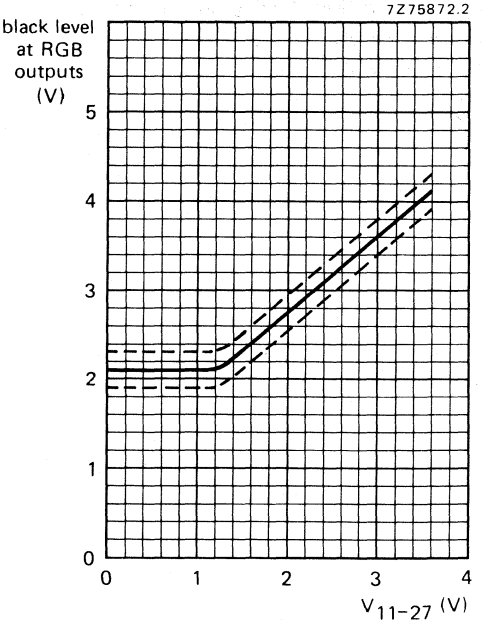


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

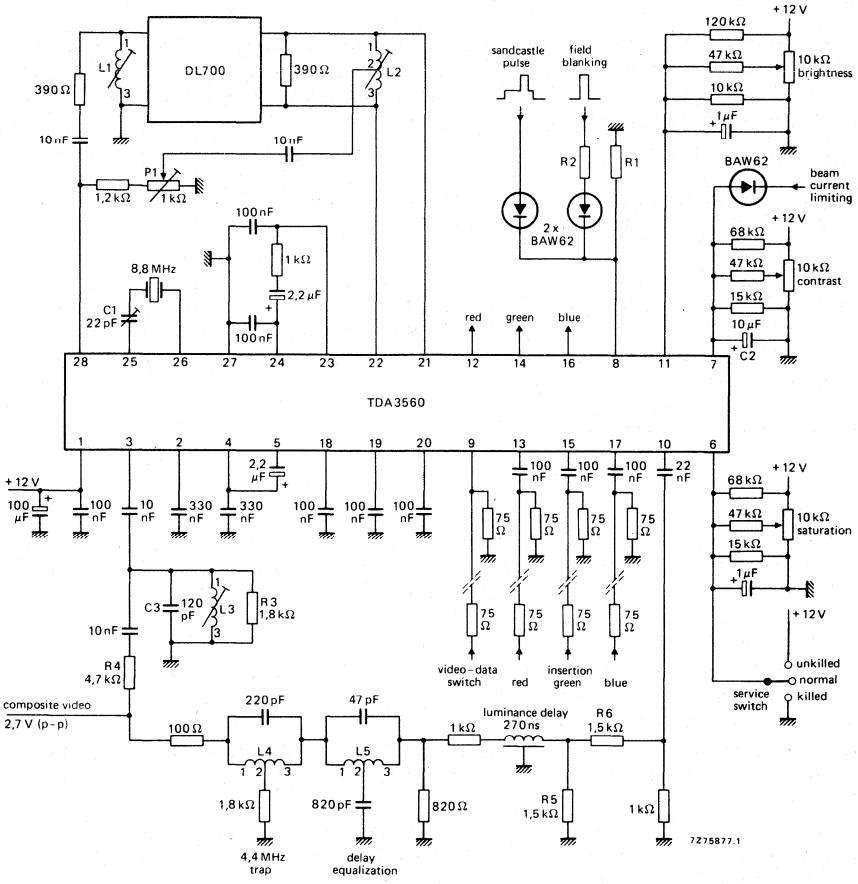


Fig. 6 Application circuit.

For adjustments see page 10.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3560. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,6 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short ($<$ 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2 V. The peak white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to this pin and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 23 and pin 24. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 μH
L2	nominal value	= 10,7 μH
L3	4,4 MHz chrominance input filter	= 10,7 μH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 μH
L5	delay equalization	= 66,1 μH
P1	amplitude of direct chroma signal	
R1 R2	field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R4 = 1 kΩ; R3, R5 and R6 can be omitted.

NTSC DECODER

The TDA3570 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. The amplifier supplies output signals up to 3,5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains an automatic picture setting switch to preset positions of both saturation and tint controls.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}14}$	typ.	12	V
Supply current	I_1	typ.	43	mA
Luminance input signal (peak-to-peak value)	$V_{5\text{-}14(p\text{-}p)}$	typ.	1	V
RGB output signals (peak-to-peak value)	$V_{26,27,28\text{-}14(p\text{-}p)}$	typ.	3,5	V
Contrast control range		typ.	13	dB
Blanking pulse and black level gating input voltage	$V_{24,20\text{-}14}$	$\geqslant$	2	V
Chrominance input voltage (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$		10 to 300	mV
Saturation control range		$\geqslant$	40	dB
Tint control range		typ.	$\pm 45^{o}$	

PACKAGE OUTLINE

28-lead DIL; plastic

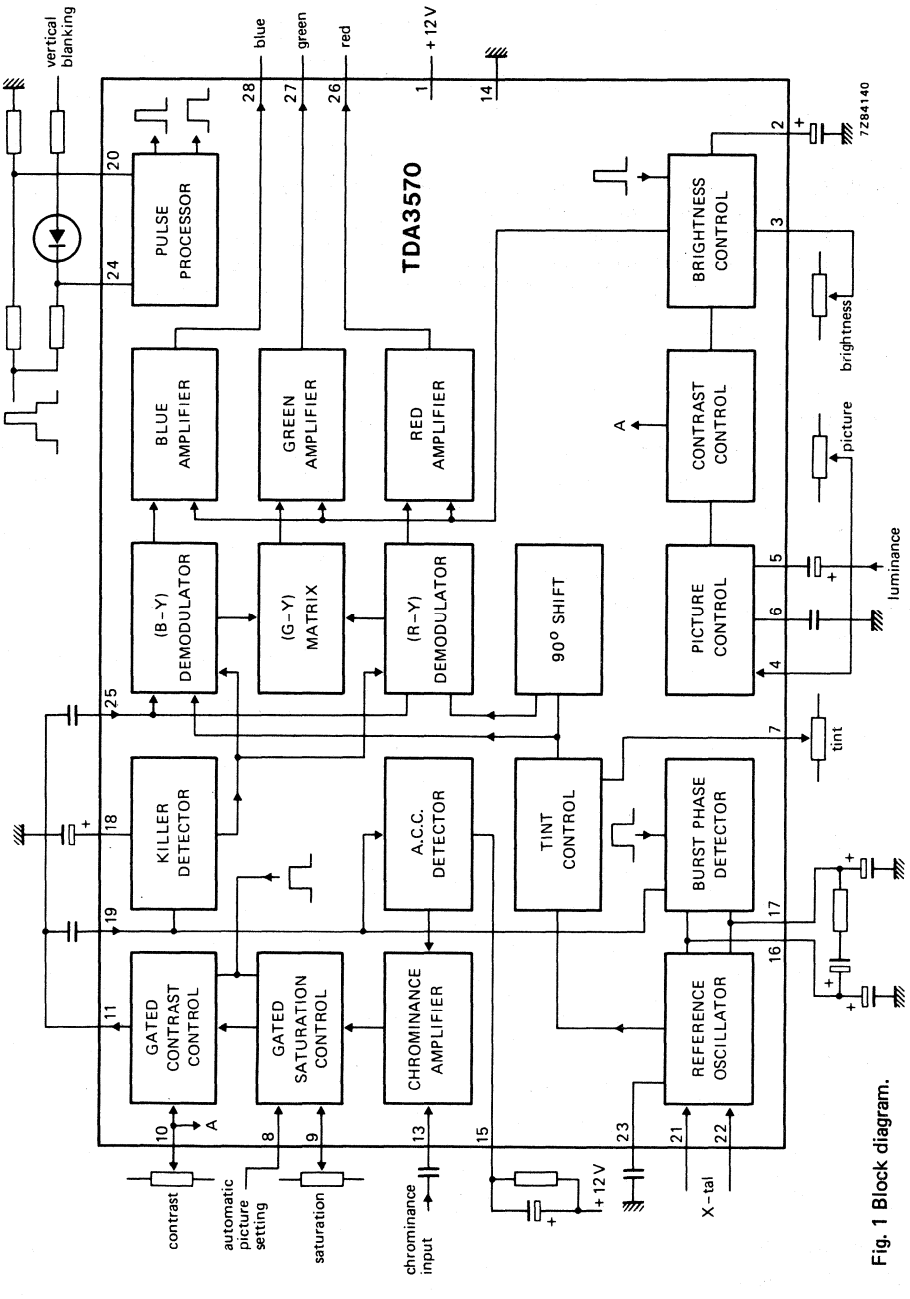


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{1-14}$	0	14,4	V
Input saturation voltage	V_{9-14}	0	V_P	V
Input contrast voltage	V_{10-14}	0	V_P	V
Input tint voltage	V_{7-14}	0	V_P	V
Input picture voltage	V_{4-14}	0	V_P	V
Input brightness voltage	V_{3-14}	0	V_P	V
Input sandcastle current	I_{20}	−30	−	mA
Input blanking pulse voltage	V_{24-14}	−6	V_P	V
Power dissipation at T_{amb} = 70 °C			750	mW
Storage temperature	T_{stg}	−40 to + 125		°C
Operating ambient temperature	T_{amb}	−20 to + 70		°C

CHARACTERISTICS

V_{1-14} = 12 V; $V_{5-14(p-p)}$ = 1 V; $V_{13-14(p-p)}$ = 150 mV;
T_{amb} = 25 °C; measured in Fig. 2

Supply voltage	V_{1-14}	typ.	12	V
Supply current	I_1	typ.	43	mA
Luminance				
Input voltage (positive-going sync pulse; peak-to-peak value)	$V_{5-14(p-p)}$	typ.	1	V
Video gain	G_v	typ.	5	
Contrast control voltage range	V_{10-14}		0 to 12	V
Contrast control range		typ.	13	dB
Brightness control voltage range	V_{3-14}		8 to 10	V
Black level range	$V_{26,27,28-14}$		0 to 7	V*
Max. output voltage	$V_{26,27,28-14}$	typ.	7	V
Blanking and gating pulse	V_{24-14}	typ.	⩾ 2	V
Input impedance (pin 24)	$\lvert Z_{24-14} \rvert$	typ.	1,5	kΩ
Black level clamp and burst gating pulse	V_{20-14}	typ.	⩾ 2	V
Input impedance (pin 20)	$\lvert Z_{20-14} \rvert$	typ.	3	kΩ
Input circuit: 3 pF in parallel with 9 kΩ				
Output circuit: emitter followers with internal R_E = 2,2 kΩ				
Picture control voltage	V_{4-14}		0 to 12	V

* Usable range depends on the output signal amplitude.

Chrominance

Input voltage (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$	typ.	150 mV
A.C.C. control range		typ.	30 dB
Colour kill level (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$	typ.	5 mV
Saturation control voltage range	$V_{9\text{-}14}$		1 to 6 V
Saturation control range		typ.	40 dB
Saturation control range in position AUTO*		typ.	6 dB
Tint control voltage range	$V_{7\text{-}14}$		1 to 6 V
Tint control range		typ.	± 45°
Tint control range in position AUTO*		typ.	± 17°
Pull in range of oscillator		typ.	± 600 Hz
Phase difference for 100 Hz change of burst		typ.	± 1,5°

Input circuit: 6 pF in parallel with 3 kΩ

* Depends on the ratio of R1/R2 in Fig. 2; position AUTO: switch closed.

APPLICATION INFORMATION

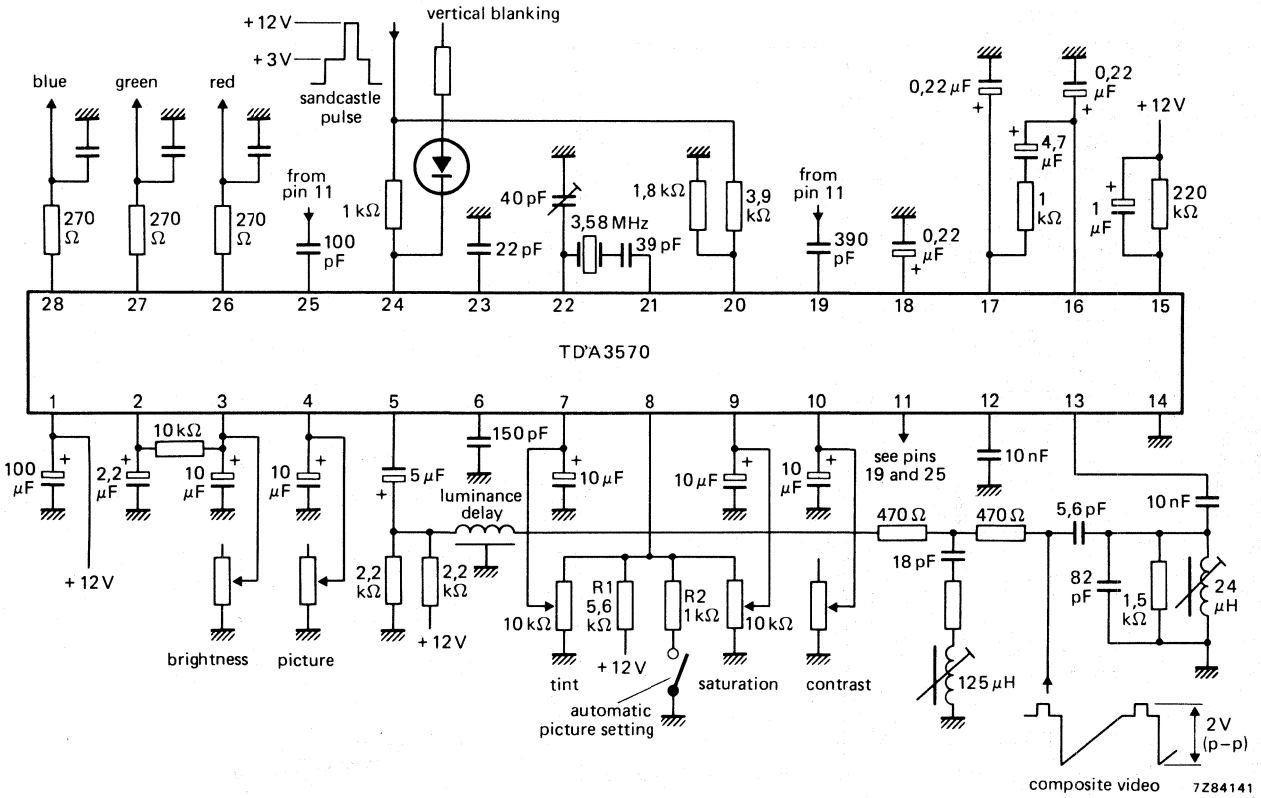
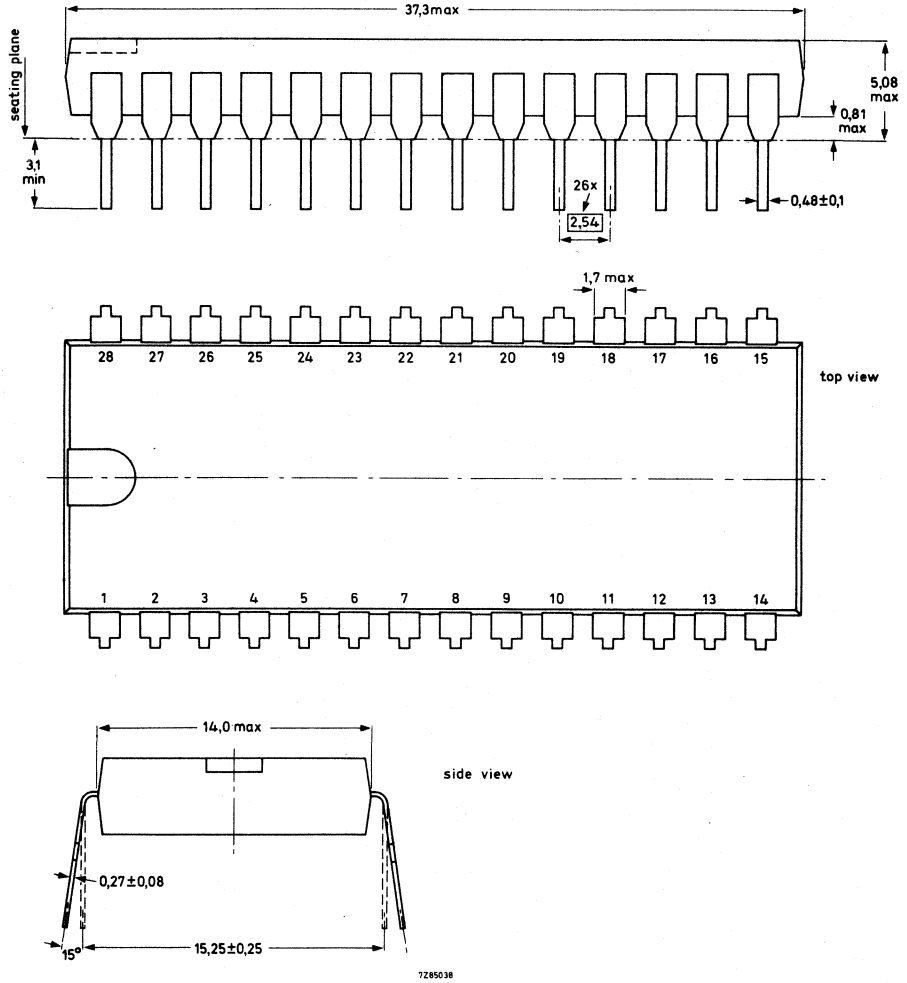


Fig. 2 Application circuit.

28-LEAD DUAL IN-LINE; PLASTIC



VERTICAL DEFLECTION CIRCUIT

The TDA3650 is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity control
- Comparator and drive circuit
- Output stage
- Flyback generator
- Voltage stabilizer
- Thermal protection circuit
- Guard circuit
- Output stage protection

QUICK REFERENCE DATA

Supply voltage range (pin 13)	V_P		10 to 50 V
Output current (peak-to-peak value)	$I_{3(p-p)}$	typ.	3 A
Operating junction temperature	T_j	max.	150 °C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\ j\text{-}mb}$	=	4 K/W

PACKAGE OUTLINE

13-lead DIL; plastic power (SOT-141).

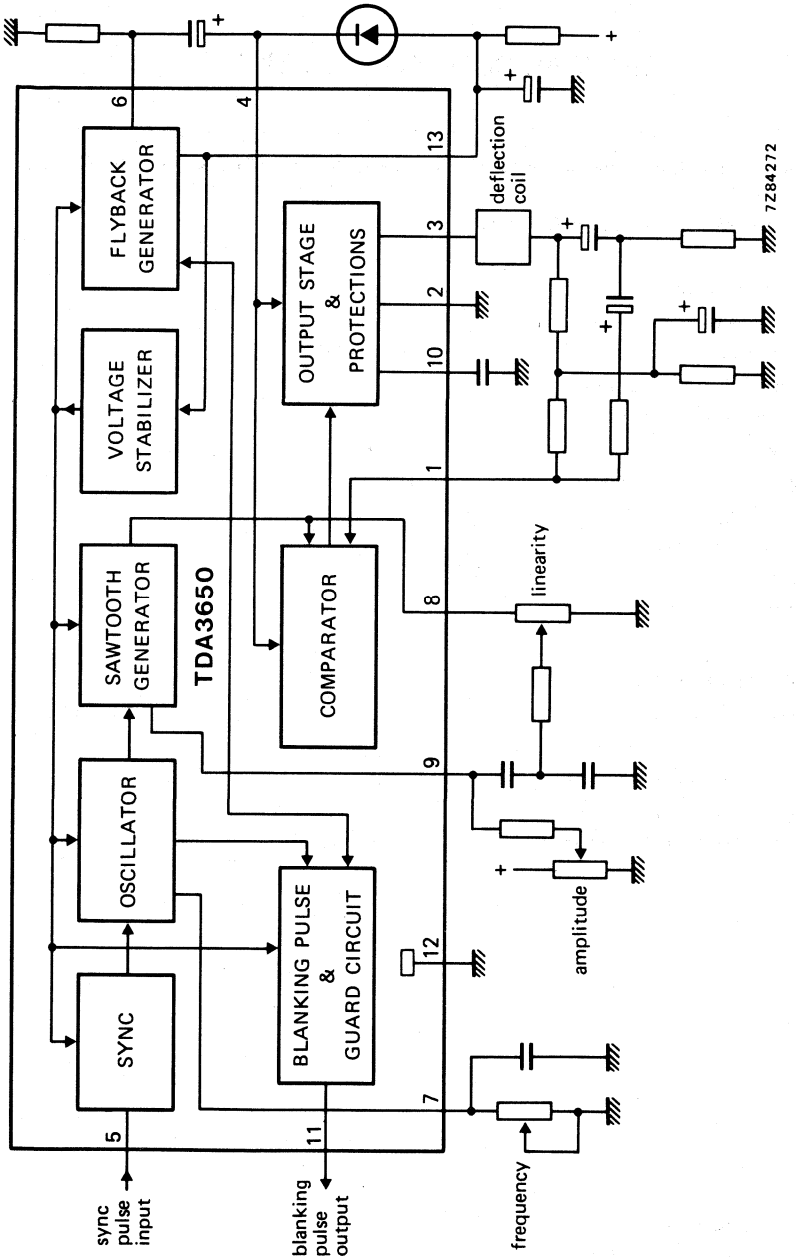


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages			
Pin 1; feedback voltage	V_{1-12}	max.	8 V
Pin 3; output voltage	V_{3-12}	max.	50 V
Pin 4; supply voltage output stage	V_{4-12}	max.	50 V
Pin 5; sync voltage	V_{5-12}	max.	8 V
Pin 13; supply voltage	V_{13-12} (V_P)	max.	50 V
Currents			
Pin 3; repetitive peak output current	$\pm I_{3RM}$	max	4 A
Pin 3; non-repetitive peak output current	$\pm I_{3SM}$	max.	6 A
Pin 6; flyback generator	I_6	max.	2 A
Pin 11; blanking pulse	I_{11}	max.	10 mA
Total power dissipation internally limited by the thermal protection circuit (see also Fig. 2)			
Storage temperature	T_{stg}		−25 to + 150 °C
Operating junction temperature	T_j	max.	150 °C

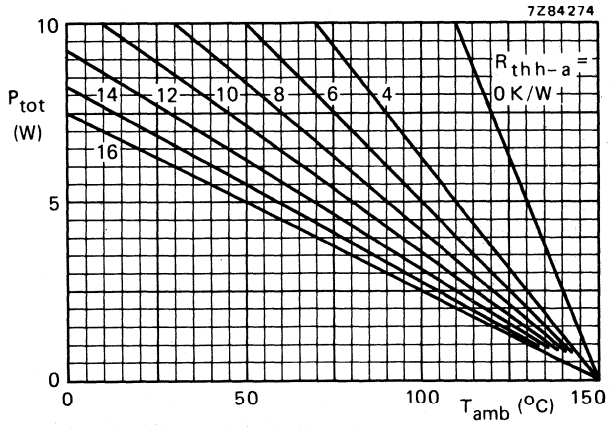


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heatsink compound is used. $R_{th\ j-mb}$ = 4 K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Supply voltage	$V_P = V_{13-2}$		10 to 50 V *
Supply voltage output stage	V_{4-2}		10 to 50 V
Maximum flyback generator output voltage	V_{6-2}	typ.	V_P–2 V
Comparator input voltage	V_{1-12}	typ.	3,8 V
Comparator input current	I_1	<	1 μA
Synchronization input voltage	V_{5-12}		1 to 8 V
Synchronization input impedance	$\lvert Z_{5-12} \rvert$	typ.	2 kΩ
Oscillator input current during scan period	I_7		1 to 5 μA
Sawtooth generator input current during scan period	I_9		1,5 to 5 μA
Sawtooth generator discharge current during flyback	I_9	typ.	4,7 mA
Minimum sawtooth voltage level	V_{9-12}	typ.	1,1 V
Supply current (without load)	I_{13}	typ.	55 mA
Output voltage			
minimum	V_{3-2}		2 to 3 V **
maximum	V_{3-2}		$V_{4-2} - 3$ to $V_{4-2} - 2$ V **
Output current (peak-to-peak value)	$I_{3(p-p)}$	<	4 A
Blanking pulse generator output voltage; $I_{11} = 0$	V_{11-12}	typ.	6,5 V
Blanking pulse duration	t_b		1,4 ± 0,1 ms
Blanking pulse output current	I_{11}	<	10 mA
Blanking pulse output impedance	$\lvert Z_{11-12} \rvert$	typ.	400 Ω
Tracking range oscillator		typ.	18 %
Oscillator temperature dependency		typ.	0,02 Hz/K
Oscillator voltage dependency		typ.	0,03 Hz/V
Junction temperature switching point thermal protection	T_j	typ.	170 °C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\ j-mb}$	typ.	4 K/W

* When the flyback generator is used, the maximum supply voltage must be chosen such that during flyback the voltage at pin 4 (supply voltage output stage) does not exceed 50 V.

** These values are obtained at an output current of 2,1A p-p (knee voltages of the output transistors). For an output current of 4A p-p the maximum knee voltage is 3 V.

PINNING

1. Comparator input
2. Negative supply (ground) for output stage
3. Output
4. Positive supply of output stage
5. Synchronization input
6. Flyback generator output
7. Tuning of oscillator (frequency control)
8. Buffered sawtooth signal
9. Tuning of sawtooth generator
10. Decoupling of output driver stage
11. Blanking output
12. Negative supply (ground)
13. Positive supply

APPLICATION INFORMATION

The function is described against the corresponding pin number

1. Comparator input

   The d.c. and a.c. feedback, which are measured at the output of the class-B amplifier, are fed into pin 1 via an external circuitry. Pin 1 is one of the two comparator inputs, the other is fed internally with the sawtooth signal.

2. Negative supply (ground) for output stage.

3. Output of class-B power stage.

   The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

4. Positive supply of output stage

   This supply is obtained from the flyback generator. An electrolytic capacitor between pins 4 and 6, a diode between pins 4 and 13, and a resistor between pins 6 and ground have to be connected for proper operation of the flyback generator.

5. Synchronization input

   The oscillator has to be synchronized by a positive-going synchronization pulse of between 1 and 8 V.

6. Flyback generator output.

   An electrolytic capacitor between pins 6 and 4 and a resistor between pins 6 and 12 (ground) have to be connected to complete the flyback generator.

7. Tuning of oscillator

   The oscillator frequency is determined by the values of the resistor and capacitor connected in parallel to pin 7.

8. Buffered sawtooth signal

   The sawtooth signal is applied via a buffer stage to pin 8. This signal is applied via an external circuit to the mid-point of the sawtooth generator tuning capacitors to obtain linearity and part of S-correction.

9. Tuning of sawtooth generator

   The timing of the sawtooth generator is defined by the potentiometer setting and the capacitors connected to pin 9. This capacitance is divided to realize linearity control and part of the S-shape.

APPLICATION INFORMATION (continued)

10. Decoupling of output driver stage

    A capacitor with a low value has to be connected to pin 10 for decoupling of the output driver stage.

11. Blanking output

    The maximum pulse amplitude without load is 6,5 V. The maximum available current is 10 mA.

12. Negative supply (ground) of small-signal part.

13. Positive supply

    The supply voltage at this pin is used to supply the flyback generator, the voltage stabilizer and the protection circuits.

The following application data are measured in a typical 30 AX system (Fig. 3).

Supply voltage	$V_P = V_{13-12}$	typ.	26 V
Output voltage (d.c. value)	V_{3-2}	typ.	14 V
Output voltage (peak value)	V_{3-2}	typ.	42 V
Supply current	$I_4 + I_{13}$	typ.	300 mA
Output current (peak-to-peak value)	$I_{3\ (p-p)}$	typ.	2,1 A
Flyback time	t_{fl}	typ.	1,2 ms
Blanking time	t_b	typ.	1,4 ms
Total power dissipation in IC	P_{tot}	typ.	4 W
Total power consumption	P	typ.	8 W
Non-linearity		<	3 %
Thermal resistance of heatsink	$R_{th\ h-a}$	typ.	10 K/W

EVELOPMENT SAMPLE DATA

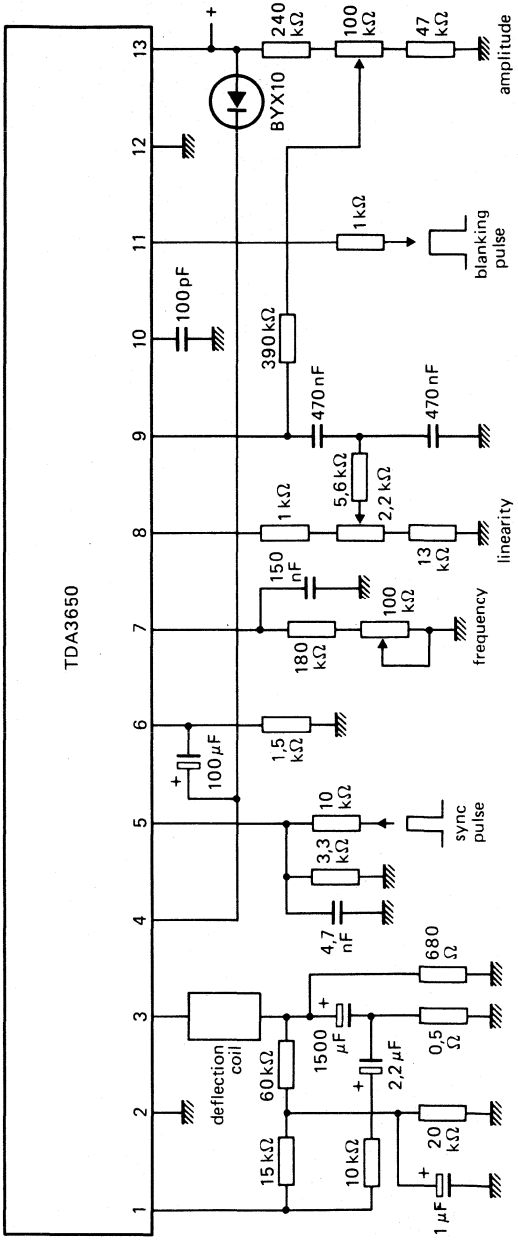


Fig. 3 Complete vertical deflection circuit for 30 AX.

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